Microprocessor Compatible 16-Bit D/A Converters

AD1147/AD1148

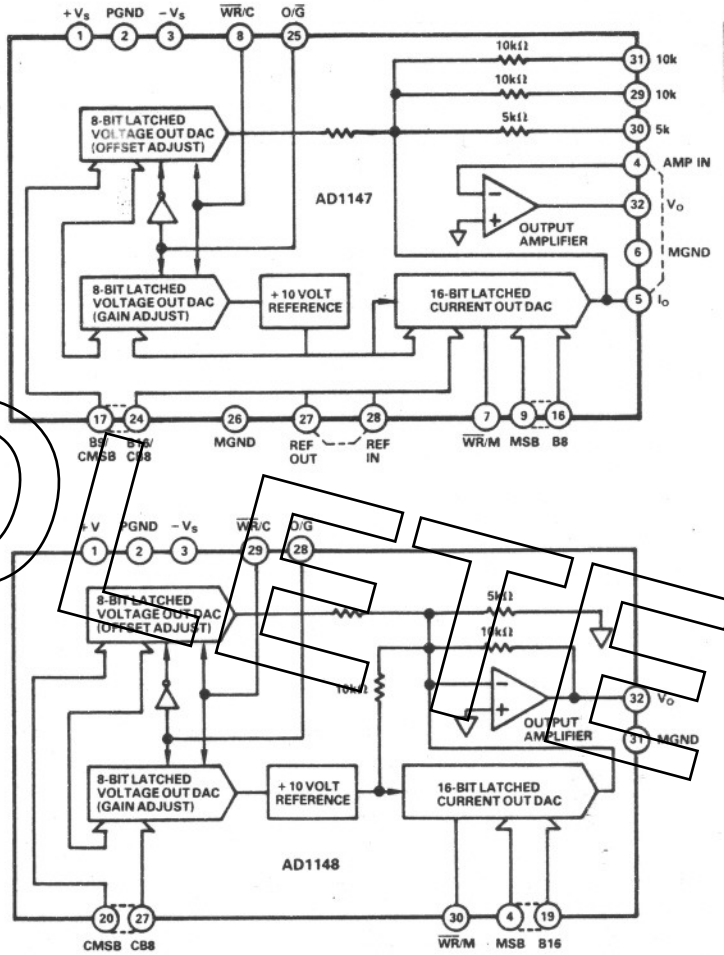
FEATURES

- Low Nonlinearity
  - Differential: ±0.00076% max
  - Integral: ±0.00076% max
  - Differential TC: ±1ppm/°C max
- Fast Settling
  - Full Scale: 20µs to ±0.00076%
  - LSB: 3µs to ±0.00076%
- Low Power: 375mW Including Reference
- Functionally Complete
  - Internal Reference, Output Voltage Amplifier, Input Latches and 8-Bit Latched Input DACs for Offset and Gain Correction.
- Full Four Quadrant Multiplying
- Low Cost

APPLICATIONS

- Automatic Test Equipment
- Scientific Instrumentation
- Beam Positioners
- Robotics
- Graphics Displays

AD1147/AD1148 FUNCTIONAL BLOCK DIAGRAMS



GENERAL DESCRIPTION

The AD1147 and AD1148 are 16-bit resolution, hybrid, latched input, digital-to-analog converters. Their two 8-bit latched input DACs allow direct offset and gain correction via microprocessor interface.

The AD1147 and AD1148 are constructed as hybrids in a compact 32-pin, triple wide dual-in-line package. Precision CMOS switches and a laser-trimmed thin-film resistor network are used to provide 16-bit accuracy and excellent temperature stability.

The Main (16-bit) DAC is loaded as a 16-bit word. The offset and gain correction DACs are each loaded as 8-bit words. The AD1147 multiplexes both correction DACs' inputs with the Main DAC's eight LSBs. This pin sharing allows for additional pin connections providing: external reference input, a current output and feedback resistors for voltage output ranges of 0 to +5V, 0 to +10V, ±5V and ±10V.

The AD1148 correction DACs' inputs are separate from the Main DAC's. The gain correction DAC's inputs are multiplexed with the offset DAC's 8-bit inputs. This allows for a separate 8-bit bus interface with the correction DACs – common in applications such as Automatic Test Equipment.

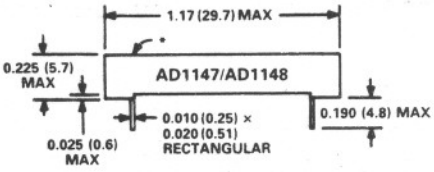
SPECIFICATIONS (typical @ +25°C and rated supplies unless otherwise specified)

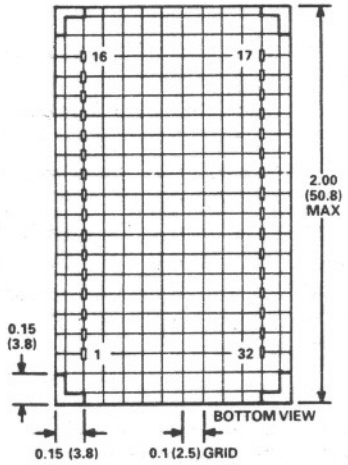
MODEL	AD1147	AD1148
RESOLUTION	16 Bits	*
ACCURACY		
Differential Nonlinearity	±0.00076% FSR[1] (max)	±0.00076% FSR[1] (typ), ±0.0015% FSR[1] (max)
Integral Nonlinearity	±0.00076% FSR[1] (max)	±0.00076% FSR[1] (typ), ±0.0015% FSR[1] (max)
Monotonic (16 Bits)	Guaranteed	*
Offset	Adjustable to Zero	*
Gain	Adjustable to Full Scale	*
STABILITY		
Differential Nonlinearity	±1ppm/°C (max)	*
Offset	±20µV/°C (max)	**
Bipolar Offset	±6ppm/°C (max)	*
Gain (Includes Int. Ref.)	±10ppm/°C (max)	*
STABILITY, Long-Term (ppm/1000 hr.)		
Differential Nonlinearity	±1ppm	*
Offset	±3ppm	**
Bipolar Offset	±3ppm	*
Gain	±12ppm	*
REFERENCE VOLTAGE		
Output Voltage	+10.00V, ±0.3% (max)	**
Output Current	2mA (max)	**
Ext. Ref Voltage Range[2]	−12V to +12V	**
Input Resistance	12kΩ	**
DYNAMIC PERFORMANCE		
Settling Time to ±0.00076%		
Voltage, Full-Scale Step	20µs	*
Voltage, LSB Step	3µs	*
Current	2µs	**
DIGITAL INPUT CODES	5 Volt CMOS/TTL Compatible	
Main DAC		
Unipolar	Binary (BIN)	**
Bipolar	Offset Binary (OBN)	*
Correction DACs	Binary (BIN)	*
ANALOG OUTPUT		
Voltage	+5V, +10V, ±5V, ±10V	±10V
Current	−2mA, ±1mA	**
Voltage Compliance	±500mV	**
Noise (100kHz BW)	60µV rms	*
POWER REQUIREMENTS		
Voltage (Rated Performance)	±15V (±5%)	*
Voltage (Operating)	±12.5V to ±17V	*
Supply Current Drain	±15mA (max)	*
Total Power @V_S = ±15V	375mW typ, 500mW max	*
POWER SUPPLY SENSITIVITY		
Offset	±10ppm/V	*
Gain	±10ppm/V	*
OFFSET ADJUSTMENT		
Range	±0.05% FSR	*
Resolution (@±10V)	1/4LSB	*
GAIN ADJUSTMENT		
Range (Unipolar/Bipolar)	±0.2% FSR[1]/±0.1% FSR[1]	NA/*
Resolution (Unipolar/Bipolar)	1LSB/1/2LSB	NA/*
TEMPERATURE RANGE		
Rated Performance	−25°C to +85°C	*
Storage Temperature	−40°C to +100°C	*
SIZE	2.00" × 1.17" × 0.225" (all maximums) (50.8 × 29.7 × 5.7mm)	

NOTES
*Specifications same as AD1147.
**AD1148 does not provide pin connections to current output, reference input, reference output or the internal feedback resistors. Output voltage range is fixed at ±10V.
[1]FSR means Full-Scale Range.
[2]Rated performance is specified with +10V reference.
Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).





* PIN 1 LOCATION IS IDENTIFIED BY A WHITE DOT ON THE TOP SURFACE.

AD1147 PIN DESIGNATIONS

PIN	FUNCTION	PIN	FUNCTION
1	$+V_S$	32	V_O
2	PGND	31	10k
3	$-V_S$	30	5k
4	AMP IN	29	10k
5	I_O	28	REF IN
6	MGND	27	REF OUT
7	$\overline{WR}$/M	26	MGND
8	$\overline{WR}$/C	25	O/$\overline{G}$
9	MSB	24	B16/CB8
10	B2	23	B15/CB7
11	B3	22	B14/CB6
12	B4	21	B13/CB5
13	B5	20	B12/CB4
14	B6	19	B11/CB3
15	B7	18	B10/CB2
16	B8	17	B9/CMSB

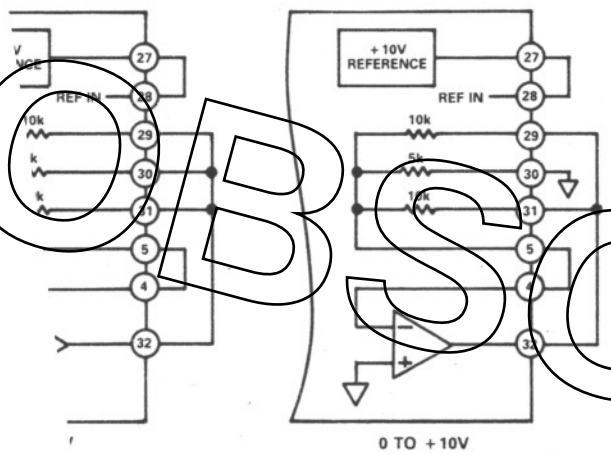
AD1148 PIN DESIGNATIONS

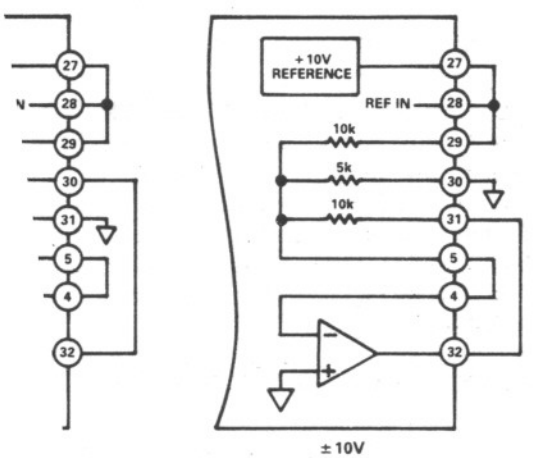
PIN	FUNCTION	PIN	FUNCTION
1	$+V_S$	32	V_O
2	PGND	31	MGND
3	$-V_S$	30	$\overline{WR}$/M
4	MSB	29	$\overline{WR}$/C
5	B2	28	O/$\overline{G}$
6	B3	27	CB8
7	B4	26	CB7
8	B5	25	CB6
9	B6	24	CB5
10	B7	23	CB4
11	B8	22	CB3
12	B9	21	CB2
13	B10	20	CMSB
14	B11	19	B16
15	B12	18	B15
16	B13	17	B14

LOG OUTPUT RANGE

AD1148 is internally connected for ±10 volts output

D1147 is pin programmable to provide a variety of analog
, either current or voltage. A unipolar output current of
2mA is available at pin 5, and can be offset by 1mA (by
ing pin 28 to pin 29) for a bipolar output of ±1mA.
voltage ranges (+5V, +10V, ±5V and ±10V) are
at pin 32 by connecting the current output (pin 5) to
fier input (pin 4) and the appropriate internal feedback
o the amplifier output (pin 32) as shown in Figure 1.





alog Output Range Pin Programming

s for the models AD1147 and AD1148
ıe timing diagrams for the MAIN 16-bit
ction DACs are shown in Figure 2.
erate as follows:

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: line is low, and latched when the

the correction DACs. Operation is

et correction DAC and the gain
l on this pin selects the offset DAC.
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SYMBOL	PARAMETER	RE(
Main DAC		
t_{DS}	Data Setup Time	140n
t_{DH}	Data Hold Time	120n
t_{WR}	Write Pulse Width	250ns
Correction DACs		
t_{CS}	O/$\overline{G}$ To Write Setup Time	200ns
t_{CH}	O/$\overline{G}$ To Write Hold Time	20ns m
t_{DS}	Data Valid To Write Setup Time	110ns n
t_{DH}	Data Valid To Write Hold	0ns min
t_{WR}	Write Pulse Width	100ns mi

Table I. Timing Requirements

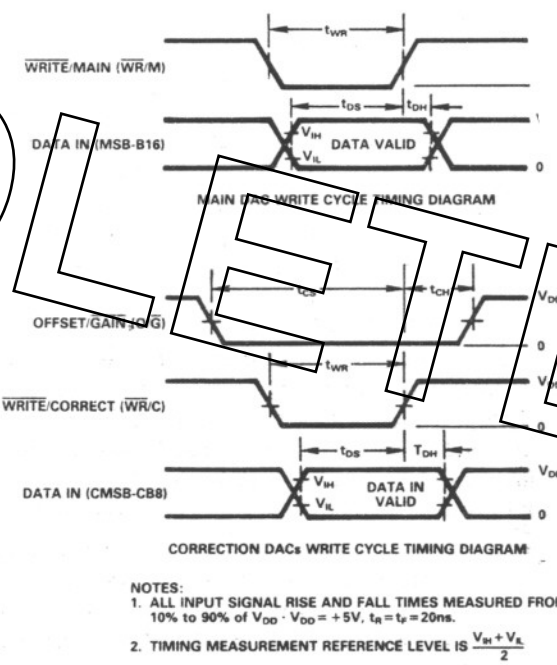

Figure 2. AD1147 and AD1148 Timing Diagrams

OFFSET AND GAIN CALIBRATION

Initial offset and gain errors can be adjusted to zero using the two internal 8-bit calibration DAC's. There are three control lines used in the calibration sequence: $\overline{WR}$/M is the write line for the Main (16-bit) DAC – the latches are transparent when the write line is low, and latched when the write line goes high; $\overline{WR}$/C is the write line for the correction DACs and operates the same as $\overline{WR}$/M; O/$\overline{G}$ selects between the offset correction DAC and the gain correction DAC – a high level on this pin selects the offset DAC and a low level selects the gain DAC.

Offset and Gain calibrations are performed as follows:

1. With $\overline{WR}$/M low, set the digital inputs of the Main DAC to "000....00" (in unipolar mode) or "100....00" (in bipolar mode).
2. Set $\overline{WR}$/M high to latch the digital input into the Main DAC.
3. With $\overline{WR}$/C low and O/$\overline{G}$ [illegible] the offset

voltage (pin V_O) is as close to 0.000000 volts as possible. Note that incrementing the digital input produces a more negative voltage output.

4. Set $\overline{WR}$/C high to latch the digital input into the offset correction DAC.
5. With $\overline{WR}$/M low, set the digital input of the Main DAC to "111....11".
6. Set $\overline{WR}$/M high to latch the digital input into the Main DAC.
7. With $\overline{WR}$/C low and O/$\overline{G}$ low, adjust the digital inputs of the gain correction DAC until the Main DAC's output voltage (pin V_O) is as close as possible to the positive full-scale voltage shown below in Table II. Note that incrementing the digital input produces a more negative voltage output.
8. Set $\overline{WR}$/C high to latch the digital input into the gain correction DAC.
9. Calibration is complete. Set $\overline{WR}$/M low and begin/resume normal digital-to-analog conversion via the Main DAC.

Output Voltage Range	Positive Full-Scale Voltage
0 to +5 volts	+4.999924 volts
0 to +10 volts	+9.999847 volts
±5 volts	+4.999847 volts
±10 volts	+9.999695 volts

Table II. Gain Calibration

GROUNDING AND GUARDING

The current from the measurement ground pin (MGND) is constant, independent of digital input, for ease of making measurements. This is the high quality ground for the AD1147 and AD1148. It should be connected to the high quality ground in the application. Power ground (PGND) should be connected to measurement ground (MGND) at the measurement point.

The current output pin (I_O) of the AD1147 is sensitive to interference from the digital input lines. It should be surrounded by a grounded guard at all times. When using the AD1147 in the voltage output mode, both the "I_O" and "AMP IN" pins should be guarded (see Figure 3).

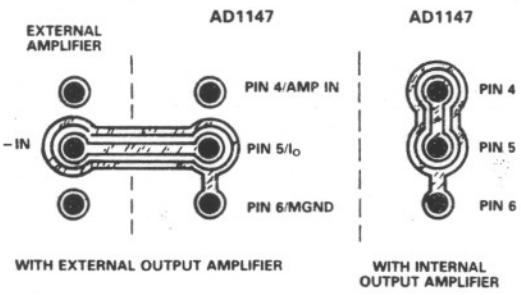

Figure 3. Typical Guarding Techniques

EXTERNAL AMPLIFIER FOR LOW DRIFT VOLTAGE OUTPUT OR HIGH OUTPUT CURRENT

The internal output amplifier of the AD1147 is designed for high-speed applications that require fast settling times. An external precision operational amplifier like the AD OP-07C can be applied when lower offset (less than 20μV/°C) is important (see Figure 4). Simply connect the current output (Pin 5) to the inverting input of the amplifier and connect the proper feedback resistors as shown in Figure 1. Be certain to keep the current output-amplifier's input connection short and surrounded by a grounded guard. To avoid degrading the gain drift performance of the DAC, always use the internal feedback resistors, since they are matched to the internal current weighting resistors of the DAC. It is also good practice to connect the negative input (Pin 4, AMP IN) of the unused internal output amplifier to its output (Pin 32, V_O).

The current drift of the AD1147 is typically 350pA/°C from +15°C to +35°C. When using the AD OP-07, the total offset drift of the output signal will typically be less than 2μV/°C.

As a second example, a high output current amplifier can be connected to the AD1147 to create a programmable power supply. The configuration is the same as shown for the AD OP-07C in Figure 4.

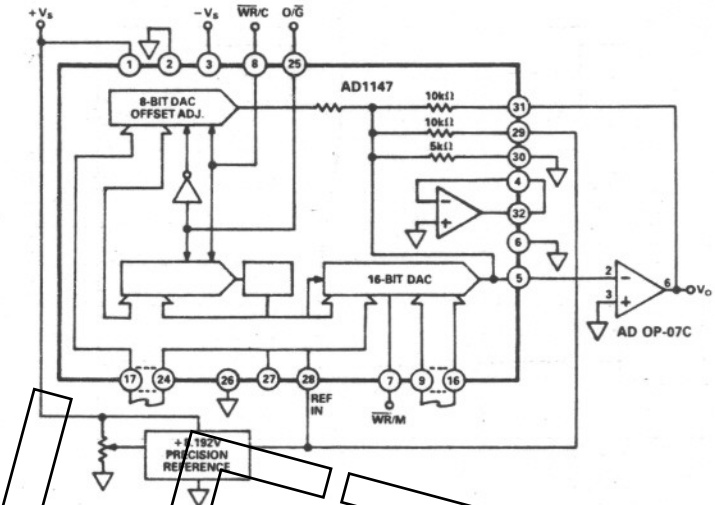

Figure 4. Precision DAC with ±8.192V F.S. Output Voltage

FULL FOUR-QUADRANT MULTIPLYING DAC

The AD1147 is a full four-quadrant multiplying DAC and can be used with references varying between +12 and −12 volts. Typical linearity vs. external reference voltage is shown in Figure 5. Output voltage ranges other than those provided can be obtained by connecting the appropriate reference voltage to "REF IN" (Pin 28), (see Figure 4). The DAC output voltage can be calculated as follows:

$$\text{UNIPOLAR } V_O = \frac{\text{DIGITAL INPUT}}{2^{16}} \times \frac{V_{REF}}{5k} \times R_{fb}$$

$$\text{BIPOLAR } V_O = \frac{\text{DIGITAL INPUT}}{2^{16}} \times \frac{V_{REF}}{5k} \times R_{fb} - \frac{V_{REF}}{10k}$$

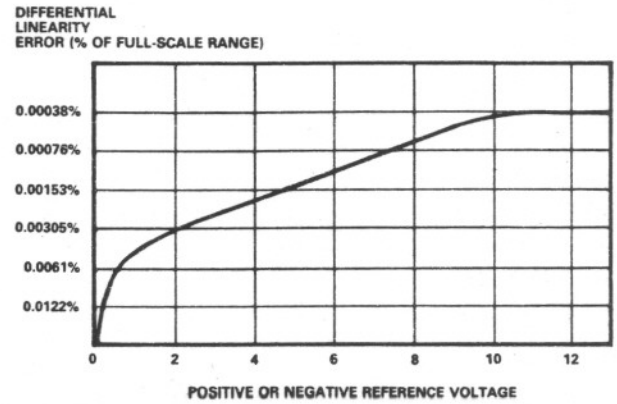

Figure 5. Typical Differential Linearity vs. External Reference Voltage

8-BIT MICROPROCESSOR INTERFACE

The AD1147/AD1148 can easily be operated with an 8-bit bus by the addition of an octal latch. The 16-bit Main DAC is loaded from the 8-bit bus as two 8-bit bytes. Figure 6 shows the configuration when using a 74HC573 octal latch.

The eight most significant bits are latched into the 74HC573 by setting the "latch enable" control line low. The eight least significant bits are then placed on the bus. Now all sixteen bits can be simultaneously latched into the Main DAC by setting $\overline{WR}$/M high.

The offset and gain correction DAC's are calibrated as they were for 16-bit microprocessor applications. See the "OFFSET AND GAIN CALIBRATION" section of this data sheet.

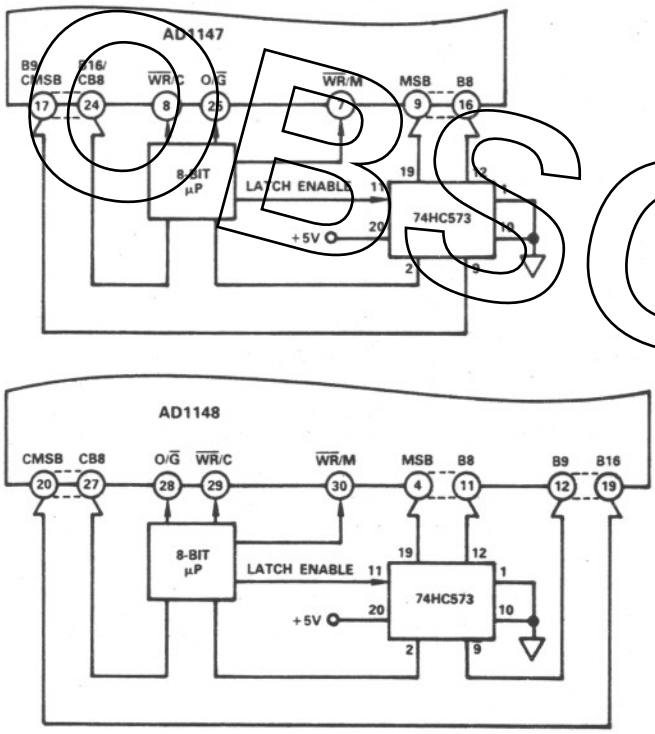

Figure 6. Connections for 8-Bit Bus Interface

AUTOMATIC TESTING OF 12-BIT ADC'S AND DAC'S

The AD1147 and AD1148 can be used as a reference DAC to automatically test the integral and differential linearity of 12-bit ADCs and DACs. An ideal reference DAC should be an order of magnitude more accurate than the devices to be tested. The AD1147 and AD1148 are sixteen times more accurate than the devices to be tested and therefore can be considered ideal.

The general test procedures for ADCs and DACs are shown below. Before actual testing proceeds, calibrate the offset and gain of the AD1147 or AD1148 (see "OFFSET AND GAIN CALIBRATION" section of this data sheet).

ADC TESTING (refer to Figures 7 and 8).

The differential nonlinearity of ADC's is the difference between the actual code widths of the analog input voltage vs. the ideal, one LSB, code widths of a perfect converter. A code width is the range of analog input voltage which produces the desired digital output word.

A code width can be measured by determining the analog input voltage at which the transition occurs from the code under test to its next lower digital output code and then differencing that analog value with the same determined for the transition from the code under test to its next higher digital output code.

Virtually all converters exhibit a degree of noise. This will necessitate an averaging technique to determine the analog input value for a code transition – where a reduction in analog input voltage produces a majority of the lower digital code decisions and an analog input increase produces a majority of the higher digital code decisions.

Begin testing by calibrating the offset and gain of the ADC under test per the manufacturer's instructions. Set the digital inputs of the reference DAC to the nominal value of the desired transition edge (produces an analog input to the device under test that is either 1/2LSB below or 1/2LSB above the ideal analog input for the code under test). Increment or decrement this digital input until the Device Under Test (D.U.T.) outputs the digital code below the transition 50% of the time and the digital code above the transition 50% of the time. Record this digital input and repeat the procedure for the next transition of the nominal code to be measured. Compare this second digital input with the recorded input. The difference between these two digital values is the width of the code being measured. A perfect code width is 16 counts of the reference DAC. Each count more, or less than 16, corresponds to a differential linearity error of 1/16LSB for the D.U.T. The arithmetic average of the two digital input values is the center of the code being tested. Each count of difference between this actual code center and the ideal, nominal code center represents an integral linearity error of 1/16LSB.

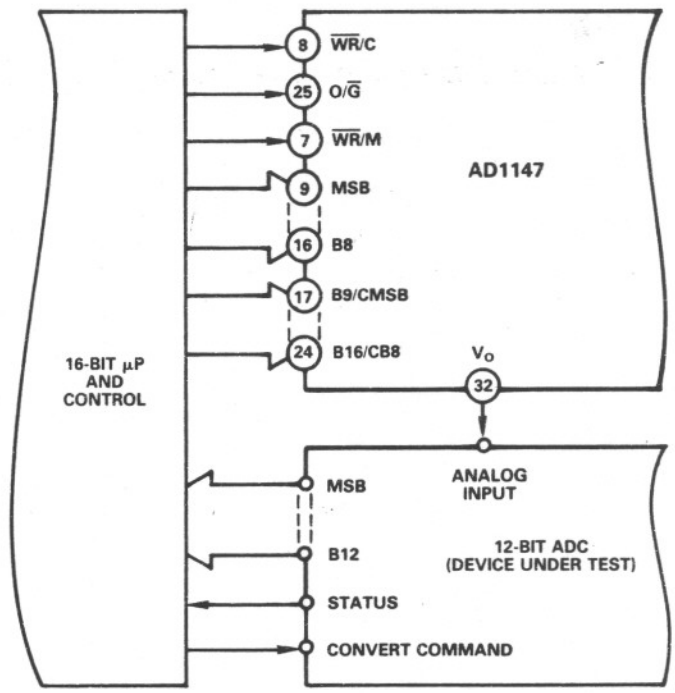

Figure 7. ADC Testing

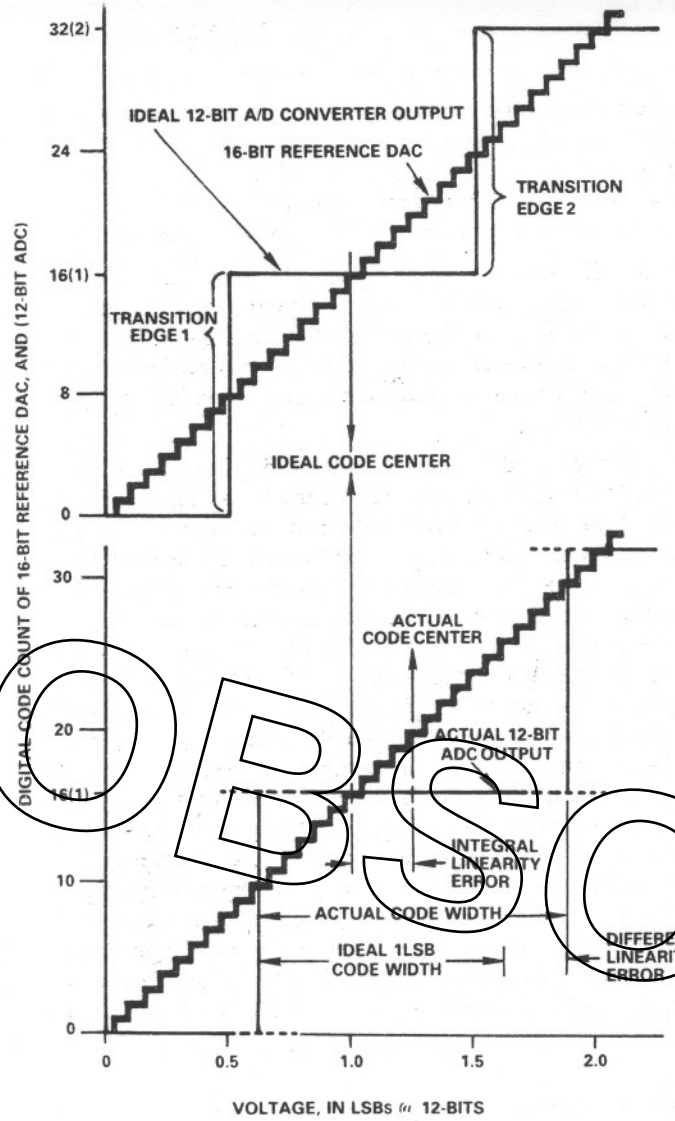

Figure 8. 12-Bit ADC Linearity Testing

DAC TESTING (refer to Figure 9).

To test 12-bit DACs begin with offset and gain calibration of the DAC under test per the manufacturer's instructions. Set the digital inputs of the reference DAC and the D.U.T. to the desired code. Latch this digital input into the reference DAC. The DACs' outputs are differenced and amplified by an AD524A instrumentation amplifier. The voltage error between the DACs is the integral linearity error.

Now null the meter and then increment or decrement the digital input to the D.U.T. only, by one LSB. The meter reading will correspond to the code width of the new digital input word. The deviation of this voltage from the ideal value of one LSB is the differential linearity error of the D.U.T.

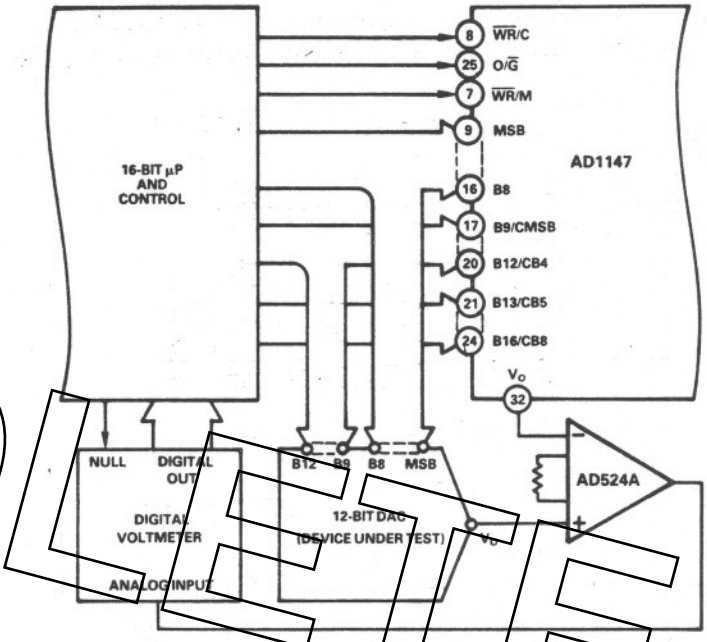

Figure 9. DAC Testing