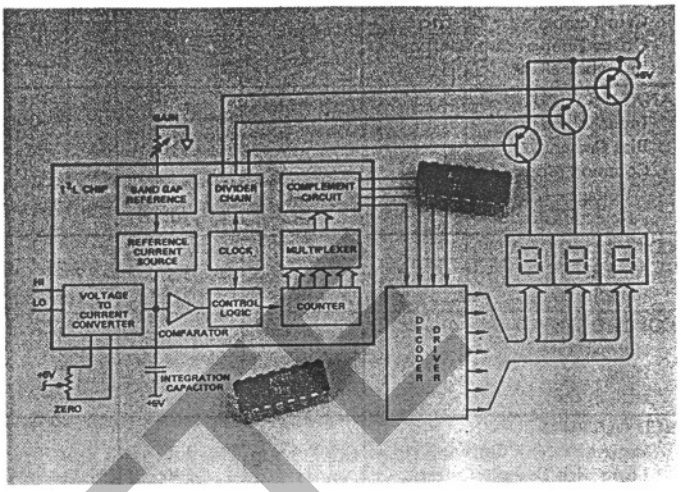
ANALOG DEVICES

I^2L 3 Digit A/D Converter

AD2020

FEATURES

- Low Cost
- I^2L LSI Design
- Multiplexed Character Serial BCD Output
- Support Components Required — 10 (including displays)
- Single +5V Power Supply Required
- Balanced Differential Input
- Internal Reference
- Low Power Consumption (50mW typical)
- Small Size: 16 Pin Dual-in-Line
- Wide Temperature Range: Operating 0 to +75°C
  Storage -55°C to +150°C
- Extended Temperature Range Available Upon Special Request



GENERAL DESCRIPTION

The AD2020 is a low cost 3 digit A/D Converter, needing only 10 additional support components to make a complete 3 digit DPM/DVM. The small total component count, the low cost, and high reliability allow for a wide variation in display applications, especially those previously utilizing APM's (Analog Panel Meters).

The technology utilized in the AD2020 is Integrated Injection Logic (I^2L), an extension of the long proven, high yield bipolar process. This technique offers a significantly higher circuit packing density. The input amplifier, comparator, band-gap reference, counters, clock, control logic, multiplexer and drivers needed to implement the dual slope conversion, are all included on a single die.

The AD2020, although it has an internal reference, consumes only 50mW of power and is operated from a single +5V supply, unlike most DPM chips requiring two (2) supplies.

The DPM chip is packaged in a standard size 16 pin-dual-in-line package. Utilizing a unique double passivation and noble-metal interconnect scheme, this plastic package offers essentially hermetic performance over a wide temperature range. The chip is available in two versions with differing guaranteed operating temperature ranges. The standard AD2020 is specified from 0 to +75°C and because of the special packaging technique, an extended temperature version is also available upon request.

EXCELLENT PERFORMANCE

The AD2020 measures inputs from -99mV to +999mV with an accuracy of 0.1% of reading ±1 digit. The balanced differential input rejects common mode voltages up to 200mV dc, enough to eliminate most ground loop problems. Polarity detection is automatic and "+" and "–" Overload conditions are indicated through BCD coding, i.e., BCD code for "+" Overload is 1011 and 1010 for "–" Overload. Zero shift is ±0.5mV over the full operating temperature range resulting in the same performance as a chip with Auto-Zero.

The benefits in manufacturing labor, inventory and reliability are self-evident. The only external components required for a complete digital display product are: 1 capacitor, 3 transistors, 1 decoder driver, 2 potentiometers and 3 displays, all operated from a single 5 volt supply.

WHAT IS I^2L?

MOS and bipolar are the two basic LSI semiconductor processes. MOS produces very dense — therefore low-cost — logic circuits, but has difficulty achieving precision analog circuitry. Before I^2L, bipolar could offer stable high-quality devices suitable for precision analog circuits, but logic consumed much expensive chip area.

Integrated Injection Logic (I^2L) now allows the design of single-chip devices containing both analog and digital functions, without calling for the compromises required in the past. I^2L has a logic density that equals or exceeds that of MOS, while employing a bipolar process suitable for precision analog circuitry.

I^2L eliminates the complexity of conventional bipolar logic by using inverted transistors (collectors and emitters are interchanged). Figure 1 shows a conventional transistor, with its wraparound P+ isolation region, which is needed to separate the collectors of adjacent transistors. When the transistors are inverted, the collectors are automatically isolated, and the emitters are grounded, at the same time.

SPECIFICATIONS (@ +25°C, V_{CC} = +5V)

PARAMETER	SPECIFICATIONS MIN	TYP	MAX	UNITS	CONDITIONS
ACCURACY					
Range	-99		+999	mV	
Accuracy		0.05	0.1	%RDG	±1 Digit
Unadjusted Gain	0.94	1.0	1.06		Gain Pot @ 2.4kΩ
Unadjusted Zero Offset	-12		+12	mV	Zero Pot Centered
Zero Width		1		Count	
Gain Temperature Coefficient		50		ppm/°C	Gain Adjusted[1]
Offset Temperature Coefficient		10.0		μv/°C	Offset Adjusted[1]
Intercode Noise		0.1		Counts	
ANALOG INPUT					
Input Impedance		100		mΩ	
Bias Current		110		nA	
Common Mode					
Voltage			±0.2	V dc	
Rejection Ratio		50		dB	
CONVERSION RATE					
Normal	2	3.5	7	Conv./sec	Hold Pin @ 0V
High Speed	48	72	168	Conv./sec	Hold Pin ≥3.2V
CONTROL INPUT (PIN 6)					
Normal Rate			0.4V	V	Pin May Be Left Open
Hold	0.8		1.6V	V	
High Speed	3.2			V	
BCD OUTPUTS					
Logic Low Sink Current	0.4	3.2		mA	V_o = ≤0.5V
Logic High Leakage Current		500		pA	V_o = 4.0V (open collector output)
DIGIT SELECT OUTPUTS					
Digit "On" Sink Current	1.6	3.2		mA	V_o = 4.0V
Digit "Off" Leakage Current		500		pA	V_o = 4.0V (open collector output)
POWER SUPPLY					
Operating Range	4.5	5.0	5.5	V	
Supply Current		10.0	17.0	mA	V_{CC} = 5.0V
Power Supply Rejection		60		dB	

ABSOLUTE MAXIMUM RATINGS @ +25°C[2]

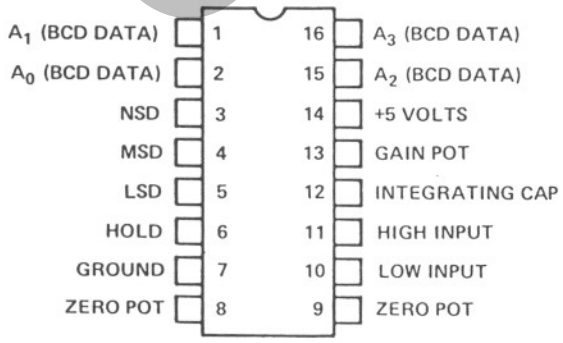
- Analog Input Voltage (pins 10 or 11 to pin 7) ..... ±15V
- V_{CC} to GND (pin 14 to pin 7) ..... +7V; -0V
- Operating Temperature Range ..... 0 to +75°C
- Storage Temperature Range ..... -55°C to +150°C
- Power Dissipation (package) up to T_A = +55°C 750mW
- Derates Above +55°C by ..... 6.7mW/°C
- Lead Temperature ..... +265°C for 10sec (max) at distance of 1/16" ±1/32" from case to solder

OVERLOAD DECODING

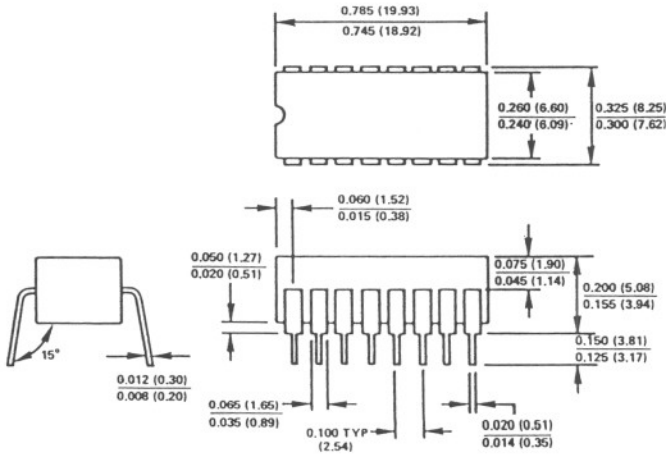
Positive Overload: 1011 (decodes as "EEE" on display via 9374 decoder driver).
Negative Overload: 1010 (decodes as "- - -" on display via 9374 decoder driver).
Negative Indication: 1010 during MSD (decodes as "-88" on display via 9374 decoder driver).

[1] Unadjusted gain and zero result in additional T.C. of 3.3μV/°C per unadjusted bit.
[2] Beyond which damage may occur.
Specifications subject to change without notice.

PIN CONFIGURATION
TOP VIEW



OUTLINE DIMENSIONS
Dimensions shown in inches and (mm).



HOLD, NORMAL, HIGH SPEED CONVERSIONS

Hold, normal and high speed conversion rates are controlled via voltage levels applied to the Hold pin (pin 6) of the AD2020. The circuit in Figure 7 shows how the three conditions are controlled by a single pin.

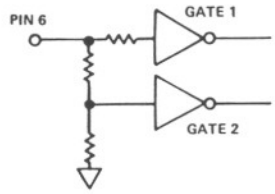


Figure 7.

- Normal Conversion
  A voltage less than 0.4V (or an open circuit) will keep both gate 1 and gate 2 off. The AD2020 in this state will convert at its normal rate.
- Hold
  A voltage greater than 0.8V but less than 1.6V will cause gate 1 to turn on but gate 2 will remain off. In this state the AD2020 will "hold" the last valid conversion.
- High Speed
  A voltage greater than 3.2V will cause both gates to turn on allowing the AD2020 to convert at its maximum rate.

Logic Compatibility

A typical circuit for making the AD2020 hold function logic compatible is shown in Figure 8. A Logic "1" applied to the base of the transistor will allow normal operation. A Logic "0" will cause the AD2020 to "hold".

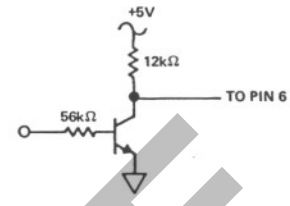
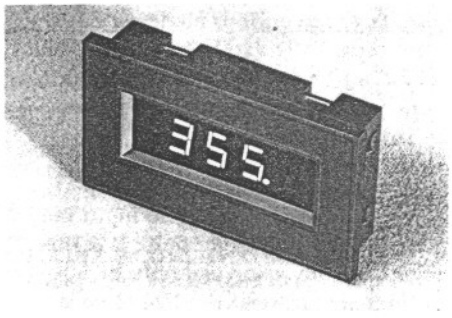
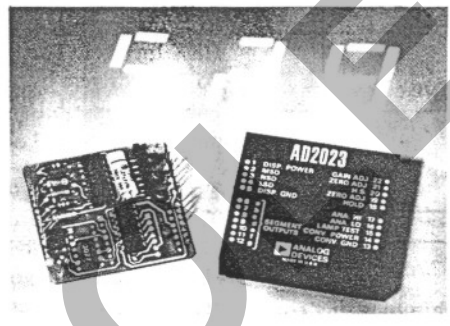
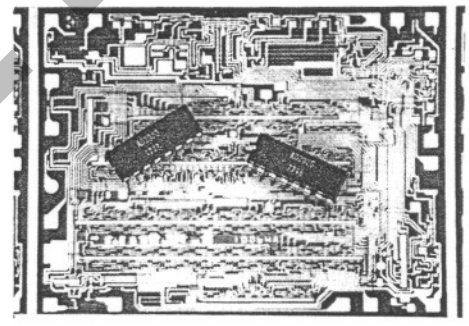


Figure 8.

"3RD GENERATION I^2L"







THE AD2026

The AD2026 was specifically designed to provide a digital alternative to analog panel meters. The complete DPM is mounted on a single 3″ by 1 5/8″ PCB. A unique case design utilizes molded-in fingers, both to capture the PCB and to provide snap-in mounting of the DPM in a standard panel cutout. No mounting hardware of any kind is used. The DPM occupies less than 1″ of space behind the panel. Only 13 components (including 3 decimal point resistors) in addition to the AD2020 make up the AD2026. Reliability is assured by the low component count, low internal heat rise (5°C), and extensive factory testing. MTBF is 260,000 hours at +25°C (for further information on the AD2026 consult factory).

THE AD2023

The AD2023 is a 3 digit DPM module containing all the circuitry, except gain adjust pot, to drive three external display digits. The AD2023 with 7-segment output and the AD2023/B, with character serial BCD output, enables the user to drive most any type of display. Like the AD2026, the AD2023 is based on the AD2020. Packaged in a small 2″ x 2″ x 0.4″ module and requiring only +5V power, the AD2023 and AD2023/B address DPM needs where available front panel space is limited. Optional operating temperature extremes of –40°C and +100°C and storage temperatures of –55°C and +125°C allow the user to apply the AD2023 in environments where conventional DPM's cannot be used.

AD2020

Completing the "Third Generation I^2L Family", Analog Devices now makes the AD2020 available to the market. Requiring only 10 support components, the AD2020 is the most complete DPM Chip available today. High reliability and performance are proven by success of the AD2026, introduced in November 1976.

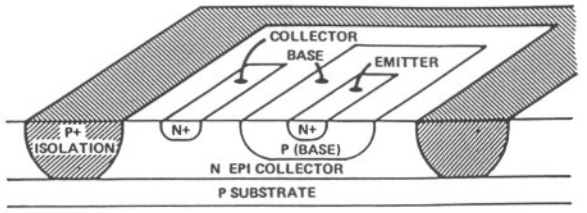


Figure 1. 3-Dimensional Section of Conventional NPN Transistor

Since I^2L logic gates can easily have multiple outputs, it is possible to use simple "wired-or logic", a means of implementing the logical "and" operation using only one conductor (wire).

A major contributor to I^2L's compactness is replacement of conventional "pullup" resistors or transistors by an injector bar. In Figure 2 the P injector acts as a combined power supply rail and pullup current source for the I^2L gates.

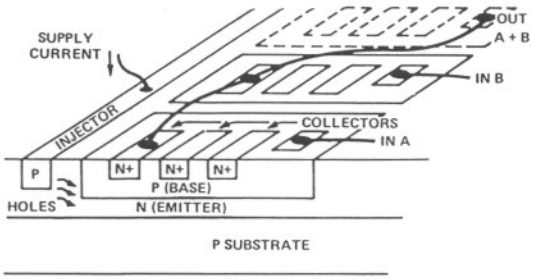


Figure 2. Sectional View of I^2L Circuit

Analog circuitry may be placed on the same chip by using conventional transistors like that of Figure 1. Thus, I^2L can be seen to combine the possibility of high-density logic functions with precision analog circuitry.

APPLYING THE AD2020

The Block Diagrams in Figure 3 and Figure 4 are two typical applications of the AD2020. In Figure 3 the AD2020 is shown in an application where LED's were the desired display. All of the A/D conversion takes place within the chip which feeds character serial data to a seven segment decoder driver. The appropriate digit is identified in three digit select lines. As shown, only 10 support components (including displays) are required. A return path for the bias current from each input (pins 11 and 10) to ground (pin 7) must be provided. Return impedance must not exceed 100kΩ.

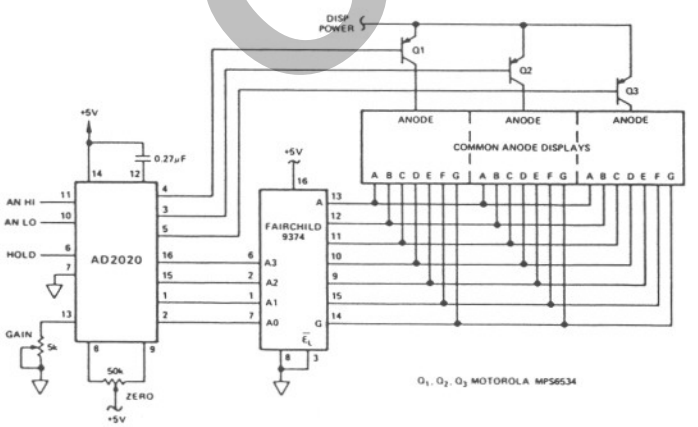


Figure 3.

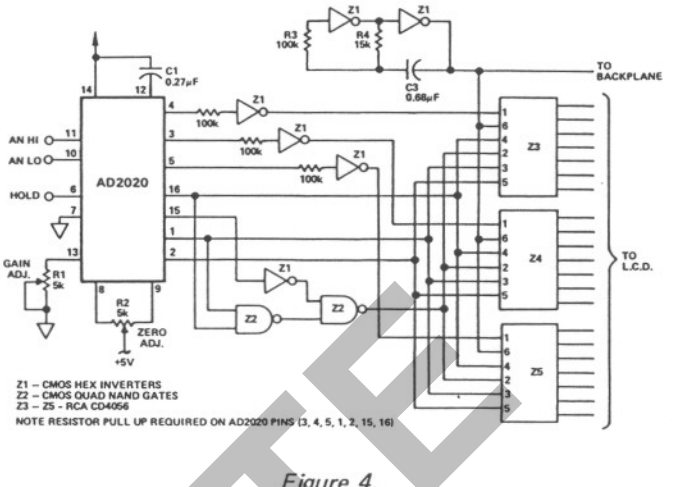
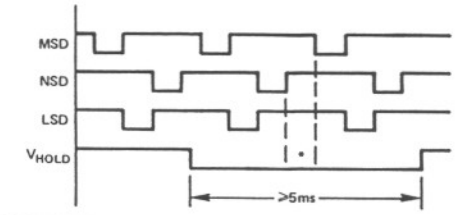


Figure 4.

The Block Diagram in Figure 4 shows an application where an LCD display was the choice. Digit selection is made via Z1, a HEX Inverter. The character serial BCD data feeds Z3, Z4, and Z5 LCD drivers by way of Z2, a CMOS quad nand gate. For CMOS compatibility, pullup resistors are required on the output pins (3, 4, 5, 1, 2, 15, 16).

TIMING DIAGRAM

The Timing Diagram, Figure 5, shows that the Hold input may be used as a psuedo-trigger provided the trigger pulse is ⩾5ms (insures at least 1 conversion). A conversion can only be initiated when all three digit lines are high and the Hold line is low. As shown, the sequence of digits is MSD, LSD, and NSD.



*CONVERSION TAKES PLACE HERE
NOTE: [1]OVERLAP MAY OCCUR BETWEEN DIGITS
[2]DATA IS VALID 2μsec. AFTER FALLING EDGE OF DIGIT SELECT LINE
[3]SWITCHING SPIKES MAY OCCUR ON DIGIT SELECT LINES

Figure 5.

A/D CONVERTER

The AD2020 can also be used as a low cost A/D Converter. The digit select signals are used to strobe the BCD data into latches. Since the AD2020 design was optimized for display applications, precautions should be taken in generating the strobe pulse. Figure 6 shows a typical configuration that provides filtering and delays necessary to ensure proper latching of data (4μs delay is sufficient).

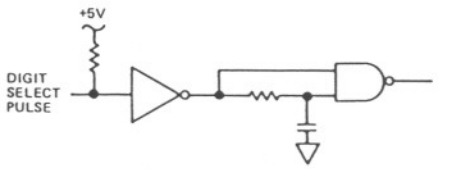


Figure 6.