Low Cost, 16-Bit Synchro/ Resolver-to-Digital Converter

AD2S46

OBSOLETE

FEATURES
1.3 Arc Minute Accuracy
16-Bit Resolution
Small 28-Pin Ceramic DIP
Low Cost

APPLICATIONS
Gimbal/Gyro Control Systems
Radar System
Engine Controllers
Sonar
Military Servo Control Systems
Fire Control Systems
Avionic Systems
Antenna Monitoring
CNC Machine Tooling

GENERAL DESCRIPTION

The AD2S46 series are 16-bit, continuous tracking synchro/ resolver-to-digital converters. They have been designed specifically for applications where space and performance are at a premium. Each 28-pin hybrid device uses a Type 2 servo loop tracking converter with a ratiometric conversion technique to provide excellent noise immunity, repeatability and tolerance of long lead lengths.

The core of each conversion is performed by a state of the art monolithic integrated circuit manufactured in Analog Devices' proprietary BiMOS II process which combines the advantage of low power CMOS digital logic with bipolar linear circuits. The use of these ICs keeps the internal component count low providing both packaging which reflects LSI monolithic standards and ensures high reliability.

The device incorporates a high accuracy differential conditioning circuit for signal inputs providing more than 74 dB of common-mode rejection. Options are available for both synchro and resolver format inputs. The converter output is via a tristate transparent latch allowing data to be read without interruption of converter operation.

Digital data transfer is accommodated by an $\overline{\text{ENABLE}}$ input which controls the tristate outputs and presents the data to the bus when taking from a HI to a LO state.

An $\overline{\text{INHIBIT}}$ precedes the $\overline{\text{ENABLE}}$ input and freezes the data transfer from the up-down counter to the output latches. This action does not interrupt the operation of the tracking loop. Releasing the $\overline{\text{INHIBIT}}$ automatically generates a data refresh. A BYTE SELECT input provides the facility for interfacing to an 8- or 16-bit bus system.

MODELS AVAILABLE

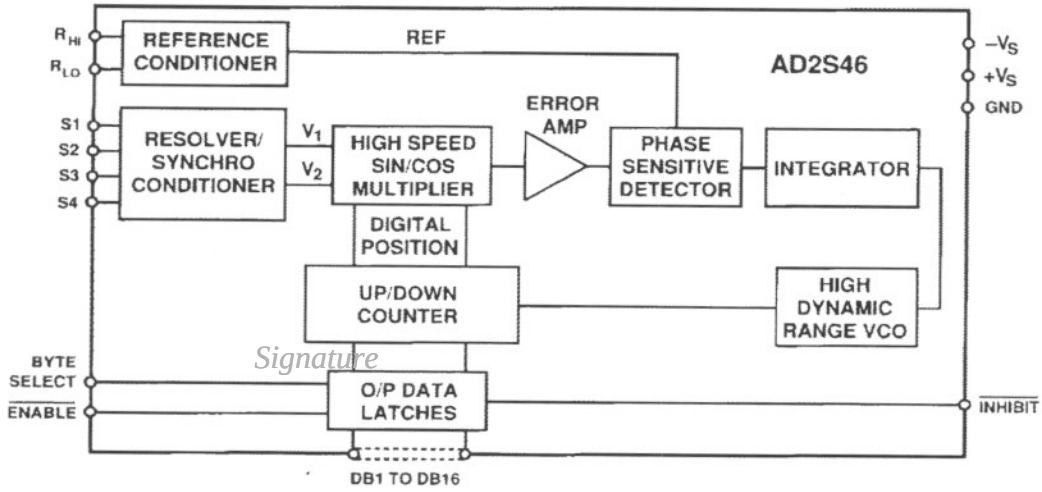
The AD2S46 series is available in 2 accuracy grades:

AD2S46TD	16 Bits	± 1.3 arc mins	−55°C to +125°C
AD2S46SD	16 Bits	± 2.6 arc mins	−55°C to +125°C

Each grade has options available which will interface to standard synchros and resolvers.

All components are 100% tested at −55°C, +25°C, and +125°C. Devices processed to high reliability screening standards (Suffix B) receive further levels of testing and screening to ensure high levels of reliability. Full ordering information is given on the back page of this data sheet.

FUNCTIONAL BLOCK DIAGRAM



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AD2S46—SPECIFICATIONS (typical at +25°C unless specified otherwise)

Parameter	AD2S46 Min	Typ	Max	Units	Comments
PERFORMANCE					
Accuracy[1]					
AD2S46TD			±1.3	arc min	
AD2S46SD			±2.6	arc min	
Tracking Rate			12	rev/s	
Resolution			16	Bits	Parallel Natural Binary
		(1 LSB = 20 arc sec)			1 IN65356
Repeatability			1	LSB	
Signal/Reference					
Frequency	360		2860	Hz	
Bandwidth			85	Hz	
SIGNAL INPUTS					
Signal Voltage		2, 11.8, 26, 90 ±10%		V rms	See Ordering Information
Impedance					
90 V Signal		200		kΩ	Resistive Tolerance ±2%
26 V Signal		58		kΩ	
11.8 V Signal		26		kΩ	
2 V Signal		4.4		kΩ	
Common-Mode Rejection	74			dB	
Common-Mode Range					
90 V Signal			±250	V dc	
26 V Signal			±120	V dc	
11.8 V Signal			±60	V dc	
2 V Signal			±12	V dc	
REFERENCE INPUTS					
Reference Voltage		2, 11.8, 26, 115 ±10%		V rms	See Ordering Information
Impedance					
115 V Reference		275		kΩ	Resistive Tolerance ±2%
26 V Reference		275		kΩ	
11.8 V Reference		25		kΩ	
2 V Reference		25		kΩ	
Common-Mode Range					
115 V Reference			±210	V dc	
26 V Reference			±210	V dc	
11.8 V Reference			±35	V dc	
2 V Reference			±35	V dc	
INHIBIT					See Figure 3
Sense					Logic LO to Inhibit
Time to Stable Data (After Negative Edge of Inhibit)			600	ns	
ENABLE					See Figure 3
Logic LO to Data Available			110	ns	Presents Data to Output
Logic HI to High Impedance			110	ns	Outputs in High Impedance State
BYTE SELECT					See Figure 3
Logic HI to Data Stable			130	ns	MS Byte DB1–DB8
Logic LO to Data Stable			140	ns	LS Byte DB1–DB8
STEP RESPONSE					
Large Step[1]		75	95	ms	179° to 1 LSB of Error
Small Step[1]		25	30	ms	2° to 1 LSB of Error
ACCELERATION CONSTANT	48000			sec^{-2}	
DIGITAL INPUTS (ENABLE, INHIBIT, BYTE SELECT)					
V_{IL}			0.8	V dc	
V_{IH}	2.0			V dc	
I_{IL}			±100	μA	V_{IL} = 0 V
I_{IH}			±100	μA	V_{IH} = 5 V

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Parameter	AD2S46 Min	Typ	Max	Units	Comments
DIGITAL OUTPUTS (DB1–DB16)					
V_{OL}[1]			0.4	V dc	I_{OL} = 1.2 mA
V_{OH}[1]	2.4			V dc	I_{OH} = 100 μA
Tristate Leakage Current			±100	μA	
Drive Capability			3	LSTTL	
POWER SUPPLIES					
Voltage Levels					
$+V_S$[1]	+14.25	+15	+15.75	V dc	
$-V_S$[1]	−14.25	−15	−15.75	V dc	
Current					
$+I_S$		30	35	mA	
$-I_S$		15	20	mA	
Power Dissipation		675	825	mW	
DIMENSIONS	1.4 × 0.6 × 0.135			inch	See Package Information
	35.6 × 15.2 × 3.4			mm	
WEIGHT			0.25	Oz	
			6.3	Grams	

NOTES

[1]Specified over temperature range, −55°C to +125°C, and for: (a) ±10% signal and reference amplitude variation; (b) ±10% signal ± and reference harmonic distortion; (c) ±5% power supply variation; (d) ±10% variation in reference frequency.

Boldface type indicates parameters which are 100% tested at nominal values of power supplies, input signal voltages, and operating frequency. All other parameters are guaranteed by design, not tested.

Specifications subject to change without notice.

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ABSOLUTE MAXIMUM RATINGS

$+V_S$ to GND . . . . . +17.25 V dc
$-V_S$ to GND . . . . . −17.25 V dc
Any Logic Input to GND (max) . . . . . +5.5 V dc
Any Logic Input to GND (min) . . . . . −0.4 V dc
Maximum Junction Temperature . . . . . 150°C
S1, S2, S3, S4 (Line to Line)[1]
(90 V Option) . . . . . ±600 V dc
(26 V Option) . . . . . ±160 V dc
(11.8 V Option) . . . . . ±80 V dc
(2 V Option) . . . . . ±14 V dc
S1, S2, S3, S4 to GND
(90 V Option) . . . . . ±250 V dc
(26 V Option) . . . . . ±120 V dc
(11.8 V Option) . . . . . ±60 V dc
(2 V Option) . . . . . ±12 V dc
R_{HI} to R_{LO}
(26 V, 115 V Options) . . . . . ±600 V dc
(2 V, 11.8 V Options) . . . . . ±50 V dc
R_{HI} and R_{LO} to GND
(26 V, 115 V Options) . . . . . ±210 V dc
(2 V, 11.8 V Options) . . . . . ±35 V dc
Storage Temperature Range . . . . . −65°C to +150°C
Operating Temperature Range[2] . . . . . −55°C to +125°C

NOTE

[1]On synchro input options, line to line voltage refers to the S2–S1, S1–S3 and S3–S2 differential voltages. On resolver input options line to line levels refer to the S1–S3 and S2–S4 voltages.

[2]Thermal Resistance: To ensure that the junction temperature of the hottest component within the hybrid does not exceed the rated maximum of 150°C, the case temperature must not exceed 130°C.

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage ($+V_S$ to GND) . . . . . +15 V dc ±5%
Power Supply Voltage ($-V_S$ to GND) . . . . . −15 V dc ±5%
Analog Input Voltage (S1, S2, S3, S4 Line to Line)
(90 V Option) . . . . . 90 V rms ±10%
(26 V Option) . . . . . 26 V rms ±10%
(11.8 V Option) . . . . . 11.8 V rms ±10%
(2 V Option) . . . . . 2 V rms ±10%
Analog Input Voltage (R_{HI} to R_{LO})
(26 V Option) . . . . . 26 V rms ±10%
(115 V Option) . . . . . 115 V rms ±10%
(11.8 V Option) . . . . . 11.8 V rms ±10%
(2 V Option) . . . . . 2 V rms ±10%
Signal and Reference Harmonic Distortion . . . . . ±10%
Phase Shift Between Signal and Reference . . . . . ±10 Degrees
Ambient Operating Temperature Range . . . . −55°C to +125°C

CAUTION

1. Absolute maximum ratings are the limits beyond which damage to the device may occur.
2. Correct polarity voltages must be maintained on the $+V_S$ and $-V_S$ pins.

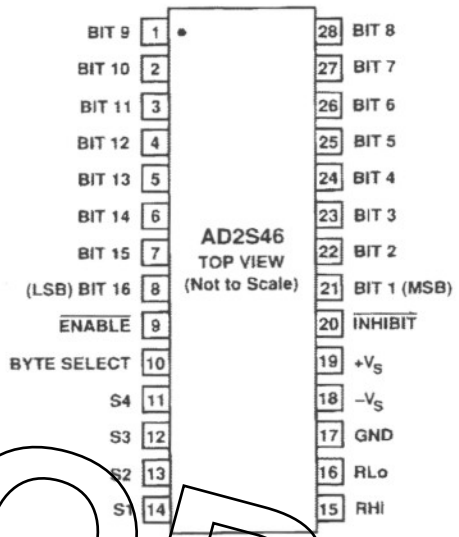
ESD SENSITIVITY

The AD2S46 features input protection circuitry consisting of large "distributed" diodes and polysilicon series resistors to dissipate both high energy discharges (Human Body Model) and fast, low energy pulses (Charged Device Model).

Proper ESD precautions are strongly recommended to avoid functional damage or performance degradation. For further information on ESD precautions, refer to Analog Devices' *ESD Prevention Manual*.

AD2S46

PIN CONFIGURATION



AD2S46 PIN FUNCTION DESCRIPTION

PIN	MNEMONIC	DESCRIPTION
1–8	DB9–DB16	PARALLEL OUTPUT DATA BITS
21–28	DB1–DB8	PARALLEL OUTPUT DATA BITS
9	$\overline{\text{ENABLE}}$	OUTPUT ENABLE INPUT
10	BYTE SELECT	BYTE SELECT INPUT SIGNAL
11–14	S4–S1	SYNCHRO/RESOLVER SIGNAL INPUTS
15	R_{HI}	INPUT PIN FOR REFERENCE HIGH
16	R_{LO}	INPUT PIN FOR REFERENCE LOW
17	GND	POWER SUPPLY GROUND
18	$-V_S$	NEGATIVE POWER SUPPLY
19	$+V_S$	POSITIVE POWER SUPPLY
20	$\overline{\text{INHIBIT}}$	INPUT PIN TO INHIBIT CONVERTER

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PRINCIPLES OF OPERATION

The AD2S46 series operate on a Type 2 tracking closed-loop principle. The output digital word continually tracks the position of the resolver/synchro shaft without the need for external convert commands and wait states. As the transducer moves through a position equivalent to the least significant bit weighting, the output digital word is updated by one LSB.

If the device is a synchro-to-digital converter, the 3-wire synchro output will be connected to S1, S2 and S3 on the unit and a solid-state Scott-T input conditioner will convert these signals into resolver format, i.e.,

$$V_1 = K\,E_0 \sin \omega t \sin \theta \quad \text{(sin)}$$
$$V_2 = K\,E_0 \sin \omega t \cos \theta \quad \text{(cos)}$$

Where θ is the angle of the synchro shaft, $E_0 \sin \omega t$ is the reference signal, and K is the transformation ratio of the input signal conditioner. If the unit is a resolver-to digital converter, the 4-wire resolver output will be connected directly to S1, S2, S3 and S4 on the unit.

To understand the conversion process, assume that the current word state of the up-down counter is ϕ. V_1 is multiplied by $\cos \phi$ and V_2 is multiplied by $\sin \phi$ to give:

$$K\,E_0 \sin \omega t \sin \theta \cos \phi$$
$$K\,E_0 \sin \omega t \cos \theta \sin \phi$$

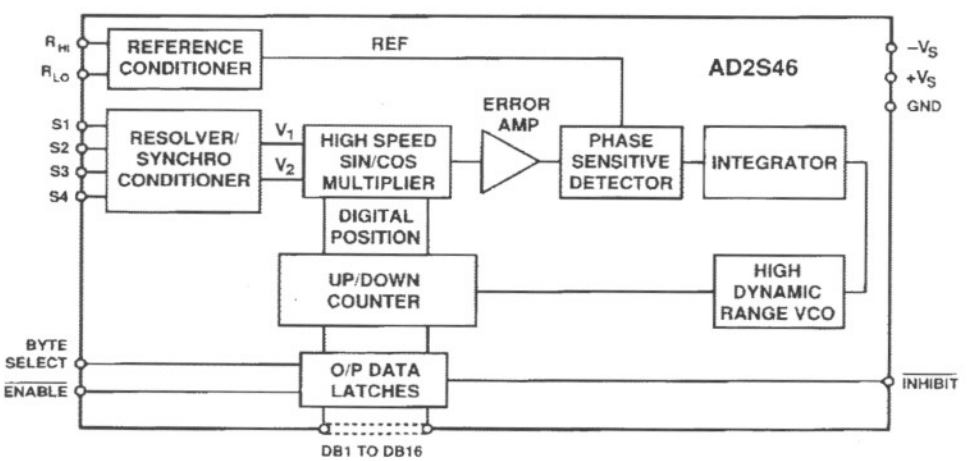
These signals are subtracted by the error amplifier to give:

$$K\,E_0 \sin \omega t (\sin \theta \cos \phi - \cos \theta \sin \phi)$$

or

$$K\,E_0 \sin \omega t \sin (\theta - \phi)$$

A phase sensitive detector, integrator and voltage controlled oscillator (VCO) form a closed-loop system which seeks to null sin $(\theta - \phi)$. When this is accomplished, the word state of the up-down counter, ϕ, equals, to within the rated accuracy of the converter, the synchro/resolver shaft angle, θ.



AD2S46 Functional Block Diagram

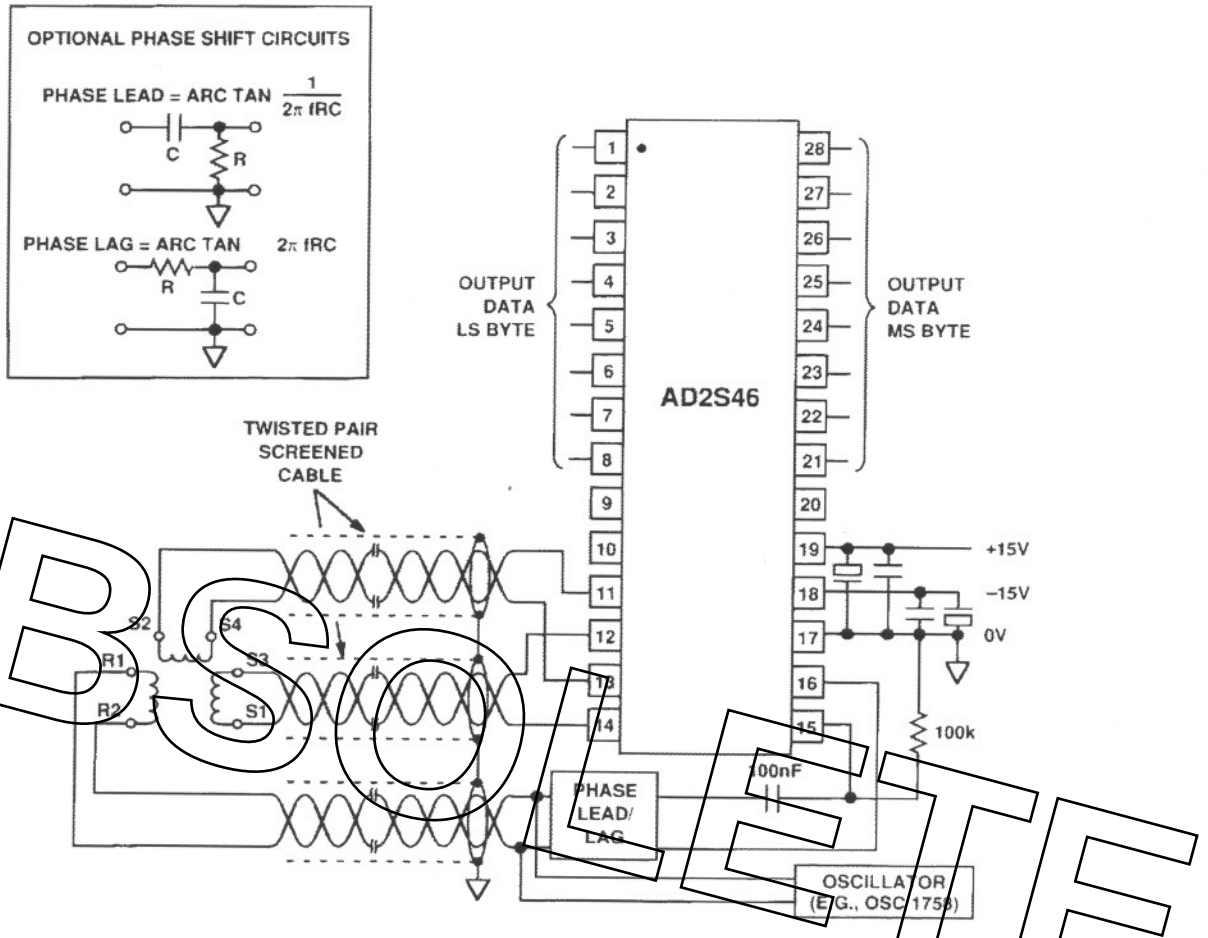


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Figure 1. Connection Diagram

CONNECTING THE CONVERTER

The power supply voltages connected to $-V_S$ and $+V_S$ pins should be −15 V and +15 V and must not be reversed.

It is suggested that a parallel combination of a 100 nF (ceramic) and a 6.8 μF (tantalum) capacitor be placed from each of the supply pins to GND.

The digital output is taken from Pins 21–28 and Pins 1–8. Pin 21 is the MSB, Pin 8 the LSB.

The reference connections are made to REF HI and REF LO. In the case of a synchro, the signals are connected to S1, S2 and S3 according to the following convention:

$$E_{S1-S3} = E_{RLO-RHI} \sin \omega t \sin \theta$$
$$E_{S3-S2} = E_{RLO-RHI} \sin \omega t \sin (\theta + 120°)$$
$$E_{S2-S1} = E_{RLO-RHI} \sin \omega t \sin (\theta + 240°)$$

For a resolver, the signals are connected to S1, S2, S3 and S4 according to the following convention:

$$E_{S1-S3} = E_{RLO-RHI} \sin \omega t \sin \theta$$
$$E_{S2-S4} = E_{RLO-RHI} \sin \omega t \cos \theta$$

It is recommended that the resolver is connected using individually screened twisted pair cables with the sine, cosine and reference signals twisted separately.

DATA TRANSFER

To transfer data the $\overline{\text{INHIBIT}}$ input should be used. The data will be valid 600 ns after the application of a logic "LO" to $\overline{\text{INHIBIT}}$. By using the $\overline{\text{ENABLE}}$ input the two bytes of data can be transferred after which the $\overline{\text{INHIBIT}}$ should be returned to a logic "HI" state to enable the output latches to be updated.

$\overline{\text{INHIBIT}}$ INPUT

The $\overline{\text{INHIBIT}}$ logic input only inhibits the data transfer from the up-down counter to the output latches and, therefore, does not interrupt the operation of the tracking loop. Releasing the $\overline{\text{INHIBIT}}$ automatically generates a refresh of the output data.

$\overline{\text{ENABLE}}$ INPUT

The $\overline{\text{ENABLE}}$ input determines the state of the output data. A logic "HI" maintains the output data pins in the high impedance state, and application of a logic "LO" presents the data of the latches to the output pins. The operation of the $\overline{\text{ENABLE}}$ has no effect on the conversion process. Timing information is shown in Figure 2.

AD2S46

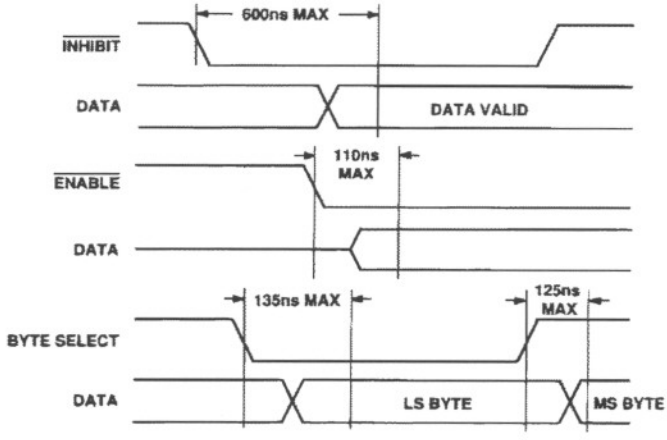

Figure 2. Timing Diagrams

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BYTE SELECT INPUT

The BYTE SELECT input on the AD2S46 can be used to interface the converter to either an 8-bit or 16-bit microprocessor bus.

To interface to a 16-bit parallel bus, the BYTE SELECT pin should be at logic HI. Thus, the most significant byte of the digital output position is at Pins 21 to 28 (Bit 1 MSB to Bit 8, respectively). Also the least significant byte is at Pin 1 to 8 (Bit 9 to Bit 16 LSB, respectively). The $\overline{\text{ENABLE}}$ control is used to present the digital 16-bit parallel digital output position data to the pins.

To interface to an 8-bit parallel bus, two sequential readings must take place. The BYTE SELECT pin at logic HI places the MS BYTE at Pins 21 (MSB) to 28. Using the $\overline{\text{ENABLE}}$, the parallel data is presented to the bus.

A logic LO on the BYTE SELECT place the LS BYTE at Pins 21 to 28 (LSB). Using the $\overline{\text{ENABLE}}$, the parallel data is presented to the bus.

The operation of the BYTE SELECT has no effect on the conversion process of the converter.

REFERENCE INPUT

The amplitude of the reference signal applied to the converter's input is not critical, but care should be taken to ensure it is within the recommended operating conditions.

The AD2S46 will not be damaged if the reference is supplied to the converter without the power supplies and/or the signal inputs.

CAUSES OF ERROR

Differential Phase Shift

Phase shift between the sine and the cosine signals from the resolver is known as differential phase shift and can cause static errors. Some differential phase shift will be present on all resolvers being a characteristic of the transducer. A small resolver residual voltage (quadrature voltage) indicates a small differential phase shift. Additional phase shift can be introduced if the sine channel wires and the cosine channel wires are treated differently. For instance, different cable lengths or different capactive loads could cause differential phase shift. The additional error caused by differential phase shift on the input signals approximates to:

$$Error = 0.53 \times a \times b \text{ arc minutes}$$

where a = differential phase shift in degrees
and b = signal to reference phase shift in degrees.

This error can be minimized by choosing a resolver with a small residual voltage, ensuring that the sine and cosine signals are routed identically and removing the reference/signals phase shift (see section on "CONNECTING THE CONVERTER"). By taking these precautions, the extra error can be made insignificant.

Resolver Phase Shift

Under static operating conditions phase shift between the reference and the signal lines alone will not theoretically affect the converter's stated accuracy. However, most resolvers exhibit a phase shift between the signal and the reference. This phase shift will give rise under dynamic conditions to an additional error defined by

$$\frac{Shaft\ Speed\ (rps) \times Phase\ Shift\ (degrees)}{Reference\ Frequency}$$

This effect can be eliminated by placing a phase lead/lag network on the reference signal to the converter equivalent to the phase shift caused by the resolver (see section "CONNECTING THE CONVERTER").

NOTE: Capacitive and inductive crosstalk in the signal and reference leads can cause similar conditions as described above.

SCALING FOR NONSTANDARD SIGNALS

A feature of these converters is that the signal and reference inputs can be resistively scaled to accommodate nonstandard input signal and reference voltages which are outside the nominal ±10% limits of the converter. Using this technique, it is possible to use a standard converter with a "personality card" in systems where a wide range of input and reference voltages are encountered.

NOTE: The accuracy of the converter will be affected by the matching accuracies of resistors used for external scaling. For resolver format options, it is critical that the value of the resistors on the S1-S3 signal input pair be precisely matched to the S4–S2 input pair. For synchro options, the three resistors on S1, S2, S3 must be matched. In general, a 0.1% mismatch between resistor values will contribute an additional 1.7 arc minutes of error to the conversion. In addition, imbalances in resistor values can greatly reduce the common-mode rejection ratio of the signal inputs.

Binary Bits (N)	Resolution (2^N)	Degrees /Bit	Minutes /Bit	Seconds /Bit
0	1	360.0	21600.0	1296000.0
1	2	180.0	10800.0	648000.0
2	4	90.0	5400.0	324000.0
3	8	45.0	2700.0	162000.0
4	16	22.5	1350.0	81000.0
5	32	11.25	675.0	40500.0
6	64	5.625	337.5	20250.0
7	128	2.8125	168.75	10125.0
8	256	1.40625	84.375	5062.5
9	512	0.703125	42.1875	2531.25
10	1024	0.3515625	21.09375	1265.625
11	2048	0.1757813	10.546875	632.8125
12	4096	0.0878906	5.273438	316.40625
13	8192	0.0439453	2.636719	158.20313
14	16384	0.0219727	1.318359	79.10156
15	32768	0.0109836	0.659180	39.55078
16	65536	0.0054932	0.329590	19.77539
17	131072	0.0027466	0.164795	9.88770
18	262144	0.0013733	0.082397	4.94385

Bit Weight Table

To calculate the values of the external scaling resistors add 1.111 kΩ extra per volt of signal in series with S1, S2, S3 and S4 (resolver options only), and 3 kΩ in extra per volt of reference in series with R_{LO} and R_{HI}.

DYNAMIC PERFORMANCE

The transfer function of the converter is given below.

Open-loop transfer function

$$\frac{\theta_{OUT}}{\theta_{IN}} = \frac{K_A\,(1 + sT_1)}{S^2\,(1 + sT_2)}$$

Closed-loop transfer function

$$\frac{\theta_{OUT}}{\theta_{IN}} = \frac{1 + sT_1}{1 + sT_1 + s^2/K_A + s^3\,T_2/K_A}$$

where $K_A = 48000\ \text{sec}^{-2}$
$T_1 = 0.0071$ sec
$T_2 = 0.00125$ sec

The gain and phase diagrams are shown in Figures 3 and 4.

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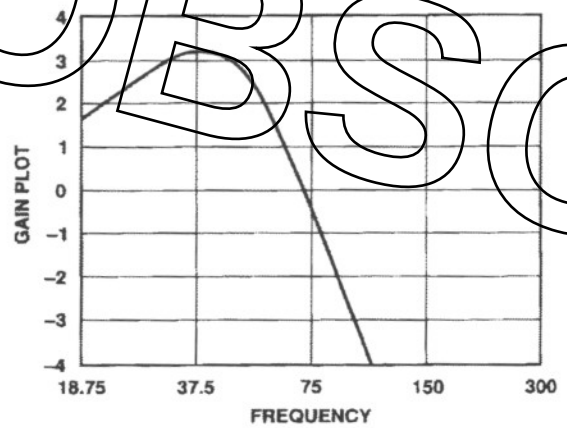


Figure 3. AD2S46 Gain Plot

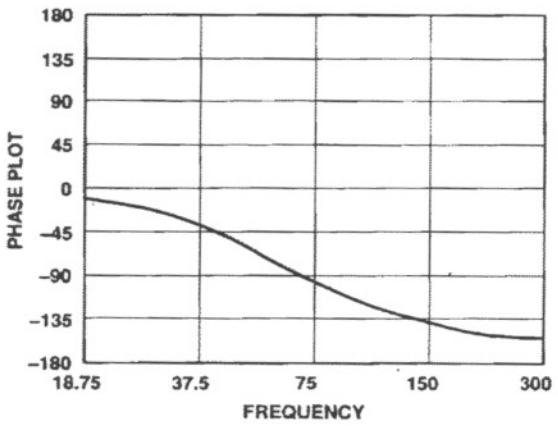


Figure 4. AD2S46 Phase Plot

ACCELERATION ERROR

A tracking converter employing a Type 2 servo loop does not suffer any velocity lag, however, there is an additional error due to acceleration. This additional error can be defined using the acceleration constant K_A of the converter.

$$K_A = \frac{\textit{Input Acceleration}}{\textit{Error in Output Angle}}$$

The numerator and denominator must have consistent angular units. For example, if K_A is in sec^{-2}, then the input acceleration may be specified in degrees/sec and the error in output angle in degrees. Alternatively, the angular unit of measure may be in radians, minutes of arc, LSBs, etc.

K_A does not define maximum acceleration, only the error due to acceleration. The maximum acceleration for which the AD2S46 will not lose track is in the order of $5° \times K_A = 238{,}000\ °/\text{sec}^2$ or about 660 revolutions/sec^2.

K_A can be used to predict the output position error due to input acceleration. For example, for an acceleration of 50 revolutions/sec^2 with $K_A = 48000$,

$$\textit{Error in LSBs} = \frac{\textit{Input Acceleration}\ [LSB/sec^2]}{K_A\ [sec^{-2}]}$$

$$= \frac{50\ [rev/sec^2] \times 2^{16}\ [LSB/sec^2]}{47662\ [sec^{-2}]}$$

$$= 68\ LSBs$$

RELIABILITY

The reliability of these products is very high due to the extensive use of custom chip circuits that decrease the active component count. Calculations of the MTBF figure under various environmental conditions are available on request.

Figure 5 shows the MTBF in years vs. case temperature for Naval Sheltered conditions and airborne uninhabited cargo calculated in accordance with MIL-HDBK-217E.

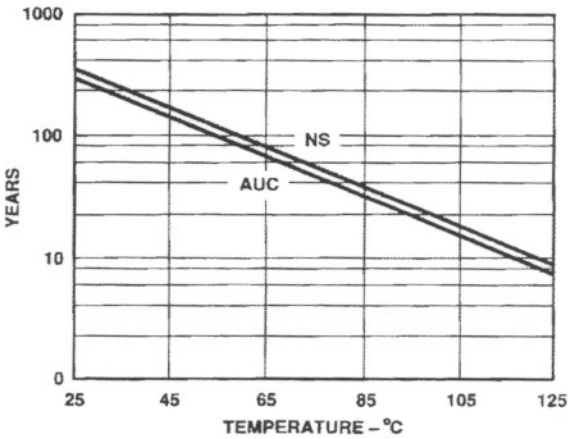


Figure 5. AD2S46 MTBF vs. Temperature

AD2S46

ORDERING INFORMATION

When ordering, the converter part numbers should be suffixed by a two letter code defining the accuracy grade, and a two digit numeric code defining the signal/reference voltage and frequency. All the standard options and their option codes are shown below. For options not shown, please contact Analog Devices, Inc.

AD2S46XD Y Z B

- B — High-Rel Processing
- Z — Base Part Number
  - Z = 0 Signal 2 V, Reference 2 V, Resolver
  - Z = 1 Signal 11.8 V, Reference 26 V, Synchro
  - Z = 2 Signal 90 V, Reference 115 V, Synchro
  - Z = 3 Signal 11.8 V, Reference 11.8 V, Resolver
  - Z = 4 Signal 26 V, Reference 26, Resolver
  - Z = 8 Signal 11.8 V, Reference 26 V, Resolver
- Y = 1 400 Hz to 2.6 kHz Reference Frequency
- X
  - X = "T" ±1.3 arc min Accuracy −55°C to +125°C Operating Temperature Range
  - X = "S" ±2.6 arc min Accuracy −55°C to +125°C Operating Temperature Range

For example, the correct part number for a component to operate with a 90 V signal, 115 V reference synchro format inputs and yield a ±1.3 arc minute accuracy over the −55°C to +125°C temperature range would be AD2S46TD12. The same part processed to high reliability standards would carry the designator B, i.e., AD2S46TD12B.

OTHER PRODUCTS

Many other products concerned with the conversion of synchro/resolver data are manufactured by Analog Devices, some of which are listed below. If you have any questions about our products or require advice about their use for a particular application please contact our Applications Engineering Department.

The SDC/RDC1740/41/42 are hybrid synchro/resolver-to-digital converters with internal isolating micro transformers.

The SDC/RDC1767/1768 are identical to the SDC/RDC1740 series but with the additional features of analog velocity output and dc error output.

The OSC1758 is a hybrid sine/cosine power oscillator which can provide a maximum power output of 1.5 watts. The device operates over a frequency range of 1 to 10 kHz.

The DRC1745 and DRC1746 are 14- and 16-bit natural binary latched output high power hybrid digital-to-resolver converters. The accuracies available are ±2 and ±4 arc minutes and the outputs can supply 2 VA at 7 V rms. Transformers are available to convert the output to synchro or resolver format at high voltage levels.

The AD2S65/66 are similar to the DRC1745/46 but do not include the power output stage. These devices are available with accuracy grades up to ±1 arc minute.

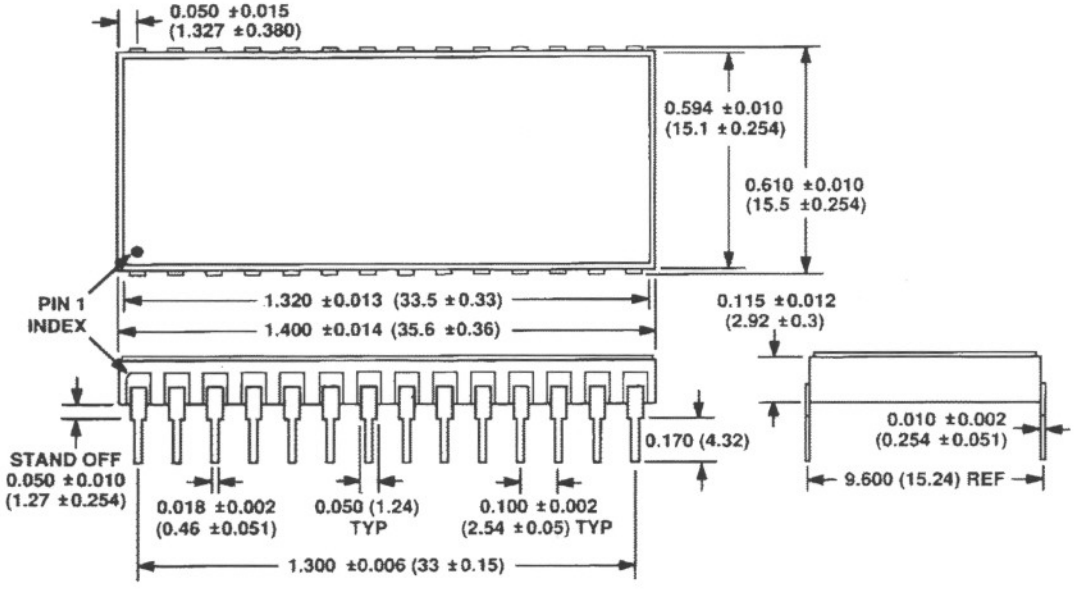
The AD2S44 and AD2S34 are 14 bit, dual channel synchro and resolver-to-digital converters. They are available with accuracy grades up to ±2.6 arc minutes and can be supplied in surface mount packages.

The 2S80 series are monolithic ICs performing resolver-to-digital conversion with accuracies up to ±2 arc minutes and 16-bit resolution.

OBSOLETE

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



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