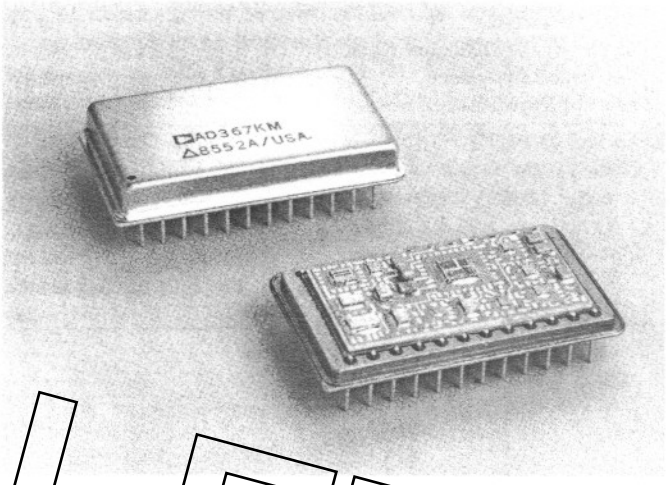
High Resolution Programmable Gain DAS

AD367

FEATURES
- Differential Input – Programmable Gain Amplifier
- 6 Bit (1 of 64) Gain Control
- Internal −10V Reference
- 15 Bit Integral Nonlinearity
- ±305μV Resolution
- 10ms Conversion Time
- External Integration Capacitor
- Programmable Conversion Time

APPLICATIONS
- Medical Instruments
- Blood Analyzers
- Analytical Instrumentation
- Data Acquisition Systems
- Chromatography
- Process Control



PRODUCT DESCRIPTION

The AD367 is a wide dynamic range integrated circuit which contains all the analog functions needed to construct a high resolution, high accuracy integrating Data Acquisition System. It utilizes hybrid technology to incorporate a programmable gain amplifier, integration amplifier, −10V reference, comparator, and control logic in a 24-pin hermetic dual-in-line package.

The programmable gain amplifier provides 6 bits (1 of 64) gain control which are digitally selectable with CMOS voltage levels. The dual slope converter uses time to quantitize the analog input signal. The differential front-end allows true differential inputs with high common-mode rejection, or single-ended inputs with ground sense capability. This conversion technique has inherent high frequency noise immunity and excellent normal mode noise rejection at frequencies that are integal multiples of $1/T_1$ (T_1 = the signal integration period). The conversion accuracy is independent of both the integration capacitance and clock frequency, since they affect both the signal integration phase and reference integration phase in the same ratio. A microprocessor and software routine or any digitizing timer that accepts TTL inputs can be used to count clock pulses to digitize the AD367 output. The integration capacitor is external, therefore conversion time may be adjusted by the user. The nominal value is 0.012μF for an integration time of 4ms and total conversion time of 10ms. By choice of integration capacitor and clock frequency the integration time is programmed from a minimum of 2ms to a maximum of 20ms. The maximum conversion rate is 200 per second.

PRODUCT HIGHLIGHTS

1. The AD367KM provides true 15-bit (±0.00305% FSR maximum linearity error) performance with 305μV resolution.
2. The differential input programmable gain amplifier front end has 6-bit (1 of 64) gain control. This provides gains of 0.282V/V to 24V/V, or input full scale ranges of 0.417V to 10.0V for maximum flexibility.
3. The integration capacitor is external. Integration time is user-programmable, from 2ms to 20ms. The maximum conversion rate is 200 conversions per second.
4. The dual slope integration conversion technique provides superior high frequency noise immunity, and excellent normal mode noise rejection of frequencies which are multiples of the inverse of the integration period.
5. An internal precision −10.0V reference is provided, but an external reference may be used for multi-channel applications where use of a system reference is required.
6. The pulse-width output is easily converted to digital binary format by the addition of external IC counter-timers. The counter clock rate is independent of the integrator clock rate.

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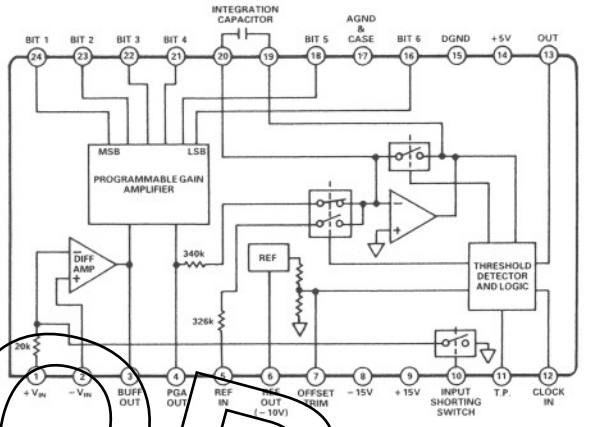
SPECIFICATIONS (typical @ +25°C, V_S = ±15V, +5V, T1 = 4.000ms, C_{INT} = 0.012µF[1] unless otherwise noted)

Parameter	AD367KM Min	Typ	Max	Units
ACCURACY/RESOLUTION				
Integral Nonlinearity Error[2]			0.00305	% FSR
Resolution[3]	±305			µV
ANALOG INPUTS				
V_{INPUT}	0		10	V
Input Resistance	80			kΩ
Common Mode Rejection Ratio[4]	90	100		dB
V_{REF} Input Resistance	300			kΩ
Shorting Switch Isolation[5]	45	56		dB
DIGITAL INPUTS				
Clock				
V_{INH}	2			V
V_{INL}			0.7	V
Gain Bits[6]				
V_{INH}	14.5			V
V_{INL}			0.5	V
DIGITAL OUTPUT (LSTTL Compatible)				
V_{OH}	2.4			V
V_{OL}			0.4	V
I_{OH}	−370			µA
I_{OL}			6	mA
DYNAMIC PERFORMANCE				
Conversion Time			10	ms
Offset Pulse Width[7]	152	200	248	µs
Scale Factor	361	384	407	µs/V
Over Temperature		±10		ppm/°C
PSRR[8]				
+15V ± 3%		0.5		µs/V
−15V ± 3%		0.5		µs/V
+5V ± 3%		1		µs/V
PROGRAMMABLE GAIN AMPLIFIER[9]				
Maximum Gain		24		V/V
Minimum Gain		0.282		V/V
Resolution			6	Bits
Gain Error, Any Range			±2	%
Gain Linearity Error			±0.00305	% FSR
INTERNAL VOLTAGE REFERENCE				
V_{REF}	−9.95	−10	−10.05	V
vs. Temperature		10	15	ppm/°C
Maximum External Current without Degradation			500	µA
POWER REQUIREMENTS				
Positive Supply Range	14.55	15	15.45	V
Negative Supply Range	−14.55	−15	−15.45	V
Logic Supply Range	4.75	5	5.25	V
Supply Current				
+15V		18		mA
−15V		23		mA
+5V		27		mA
Power Dissipation		750	1100	mW
TEMPERATURE RANGE				
Specification	0		70	°C
Operating	−25		+85	°C
Storage	−55		+125	°C
PACKAGE	24-Pin DIP			

NOTES
[1]Polystyrene or Teflon.
[2]Referenced to the input.
[3]Referenced to the output of the programmable gain stage (Pin 4).
[4]Source impedance < 1Ω 0 to 10V
[5]A_{INL} (Pin 2) at analog ground.
[6]Open collector TTL and 15V CMOS compatible.
[7]Offset Pulse width (V_{IN} = 0V) = $\frac{V_{OS} C R_{INT2}}{V_{REF}}$, R_{INT2} = 327kΩ nominal.
[8]V_{IN} = 10V, Gain = 1.03.
[9]Gain = $\frac{24 \times (128 \times B1 + 64 \times B2 + 32 \times B3 + 16 \times B4 + 8 \times B5 + 4 \times B6 + 3)}{255}$

Specifications subject to change without notice.



AD367 FUNCTIONAL BLOCK DIAGRAM

BASIC OPERATION

The AD367 is a high resolution dual slope integrating converter building block. Its output is a pulse width whose duration is proportional to the input voltage and the gain selected. The active-low output pulse is used to gate a separate counter which accumulates pulses from a high-speed clock. This partition of the analog-to-digital conversion function into an analog processing section and digital counting greatly reduces the potential for crosstalk between the noisy digital function and the low-level signal processing performed by the analog front-end. This preserves the inherent rejection of high frequency normal mode noise that is a prime advantage of the dual slope conversion technique.

INPUT STAGE

The AD367 is internally partitioned into a differential-input amplifier, a single-ended user-programmable gain amplifier, and the actual dual-slope converter. The differential amplifier allows digitization of input signals with common mode voltages of up to ±10V. It has a nominal input impedance of 100kΩ and is configured for unity gain.

The programmable gain amplifier (PGA) is programmed via a 6-bit digital code. If "B_1", represents the logical value of the most significant gain-selected bit, "B_2" the next most significant bit, etc., then the gain of the PGA is:

$$G = \frac{(128B_1 + 64B_2 + 32B_3 + 16B_4 + 8B_5 + 4B_6 + 3) \times 24}{255}$$

The gain-select pins are internally pulled-up to the +15V supply. Gain programming can be accomplished using either an open collector TTL Driver such as the 7406 or with 4000-series CMOS (V_{DD} = 15V). For fixed gain applications the gain-select pins can be tied to analog ground or left open as required.

B_1	B_2	B_3	B_4	B_5	B_6	GAIN (V/V)
0	0	0	0	0	0	0.282
0	0	0	0	0	1	0.659
			.			.
			.			.
			.			.
1	0	0	0	0	0	12.33
			.			.
			.			.
			.			.
1	1	1	1	1	1	24.00

Table I. AD367 PGA Truth Table

INTEGRATOR STAGE

The AD367 integrator stage uses the dual slope conversion technique. A simplified dual slope converter is shown in Figure 1. While the input pulse is applied to clock in, the input signal is applied to the integrator. After a predetermined period the input pulse is removed, a reference signal of opposite polarity is applied to the integrator, and the output pulse is initiated. At the moment the integrator is switched to the reference (deintegration) phase the accumulated charge on the integrating capacitor is proportional to the average value of the input over the integration interval. The deintegration of the reference is an opposite going ramp with slope V_{REF}/RC. When the integrator output reaches zero, the comparator is tripped and the output pulse is terminated. This completes the conversion cycle. Since the charge gained in the integration phase is proportional to $V_{IN} \times T$ (see Figure 1) and the amount of charge lost is proportional to $V_{REF} \times t$ (and equal to the amount of charge gained) t is proportional to V_{IN}/V_{REF}. The converter output is thus a pulse whose width is proportional to the input voltage. A dual slope converter is therefore a Voltage-to-Time converter. If the output pulse is used to gate a binary counter, the output of the counter will be binary digital representation of the input voltage.

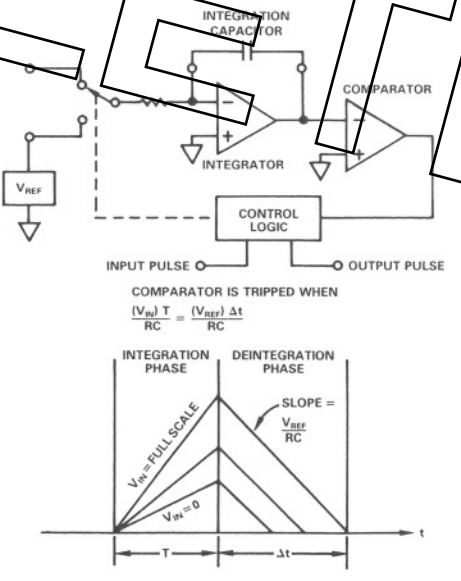


Figure 1. Simplified Basic Dual Slope Converter

ADVANTAGES OF DUAL-SLOPE INTEGRATION

Conversion accuracy is independent of the length of the clock period and the integrating capacitance. Theoretical accuracy depends only on the absolute value of the reference and the stability of the clock. Even changes in other components such as the comparator input offset voltage have no effect as long as they do not change during a conversion. Differential linearity is excellent since the technique is analog and inherently free from discontinuities.

AD367 DETAILED OPERATION

The input differential amplifier operates with input voltages within the common mode range of 0 to 10V. The input resistance is 100kΩ (80kΩ minimum) and there is a shorting switch on the noninverting input for user calibration in single-ended mode.

The input shorting switch shorts $+V_{IN}$ to ground through 20kΩ to limit the short circuit current of the driver. The AD367 inputs must be buffered. The AD OP-07 is well recommended for this purpose, due to its low noise. For source impedances of less than 5-10kΩ the AD OP-27 would be an even better choice. Note: The high 1/f noise of most FET and BiFET amplifiers make them unsuitable for this application.

The offset of the PGA section is not trimmable per se, however, the direct PGA output is available on Pin 4. Great care must be exercised to avoid introducing extraneous signals at this point. A more detailed procedure for offset trim and calibration of the AD367 is given below in the calibration section.

The dual slope converter section is configured for a nominal full-scale input voltage of 10V. In addition, the zero point of the converter is offset by 5% full-scale. This guarantees that the converter linearity will not be degraded for inputs near zero. Maximum linearity is obtained when the gain is programmed so that the maximum full-scale input voltage produces an output pulse of maximum duration consistent with the desired conversion rate. Alternatively the gain can be set to provide a 10V signal to the integrator (or Pin 4, the output of the PGA) when a full-scale input is supplied.

The built-in offset is also used to protect against possible negative polarity inputs while taking very low level measurements (or "dark current" readings from optical sensors). The offset pulse is accomplished by using a portion of the internal reference as the threshold voltage to signal the end of conversion as shown in Figure 2. This voltage appears on Pin 7 and is factory set for

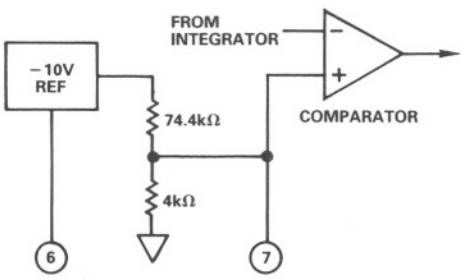


Figure 2.

−0.510V, which yields a nominal 200μs offset pulse with a 0.012μF integration capacitor. This offset pulse width may be adjusted by using a 100kΩ potentiometer as shown in Figure 3.

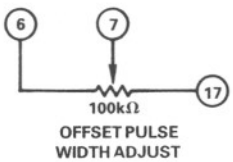


Figure 3.

The leading edge of an externally applied negative going clock pulse initiates a conversion. The AD367 will output a pulse whose width is proportional to the input signal. The output pulse is active low. Its leading (falling) edge is triggered by the rising edge of the external clock, and its trailing edge is dependent upon the input signal level. When using the internal reference or with an external −10V reference a clock pulse of 4ms provides an integrator full scale range of 10V with a 0.012μF integration cap.

For other reference and integration capacitor values the signal integration period should be adjusted to prevent saturation of the integrator, i.e., the maximum integrator deflection should not exceed 10V.

The AD367 Transfer Function is:

$$\text{Pulse Width} = \frac{-V_{IN}}{V_{REF}} \times \frac{R_{INT2}}{R_{INT1}} T_1 + \frac{V_{OS}\, C\, R_{INT2}}{V_{REF}}$$

Where:

T_1 = The clock period
V_{OS} = Voltage Offset (−0.510V nominal)
C = Integration Capacitor
R_{INT1} = Signal Integration Resistor = 340kΩ
R_{INT2} = Reference Integration Resistor = 327kΩ
V_{REF} = −10V (if internal voltage reference is used)

Figure 4 shows the AD367 operation for a near full scale input voltage. The input signal is integrated as the negative slope, and the reference voltage as the positive slope. The output pulse is low until the positive going edge (the reference integration phase) exceeds $-V_{OS}$ (+0.510V). The rising edge of the clock coincides with the knee of the integrator and the falling edge of the output.

Figure 5 shows a good view of the offset at work. A slight negative input voltage will not cause an absence of output pulse ($V_{IN} > -0.05V$).

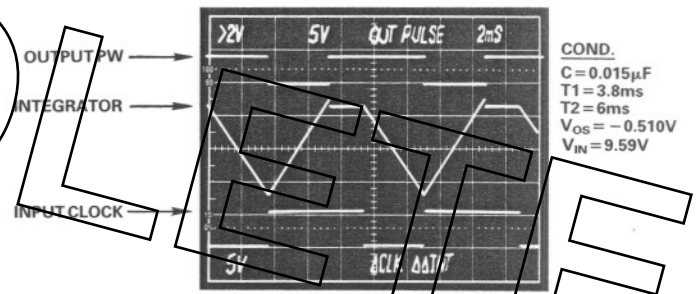


Figure 4.

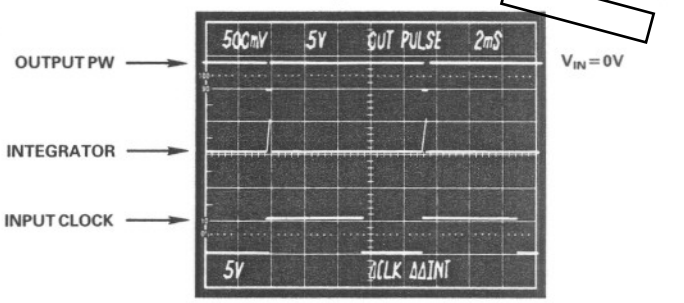


Figure 5.

To maximize the resolution and accuracy of the converter, the PGA gain should be set such that the maximum input signal voltage provides a 10V signal to the integrator (Pin 4). Then the clock pulse width and integration capacitor should be selected using the relation:

$$\frac{T_1}{C_{INT}} \cong R_{INT1} = 340k\Omega$$

This ensures that the maximum dynamic range of the integrator is used, and will result in the best linearity from the converter. Polystyrene or Teflon capacitors only are recommended. The AD367 Timing Diagram is shown in Figure 6.

PGA settling under worst-case conditions (Gain = 24, full scale input voltage step) is typically 70μs, as shown in Figure 8. The PGA output must be allowed to settle before a conversion is initiated, or the first conversion result after an input voltage change ignored if the AD367 is operated in continuous conversion mode. Figure 9 shows the PGA settling after a change from minimum to maximum gain (0.282 to 24 V/V), which is also 70μs typically.

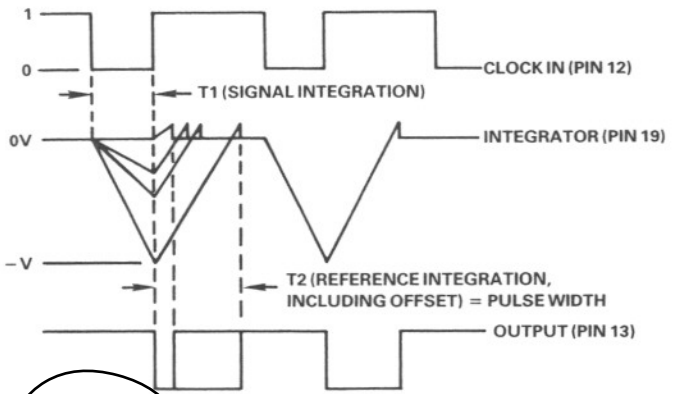


Figure 6. AD367 Timing Diagram

CALIBRATION

The AD367 should be endpoint calibrated for maximum system accuracy. Calibration is a straightforward procedure:

1. Choose a gain consistent with keeping the output of the programmable gain amplifier at or below 10V when a full scale input voltage is applied.
2. Apply a zero input signal, V_Z. Use the shorting switch if the input is single-ended. The shorting switch will ensure a good ground potential at the input.
3. Measure the output offset pulse, PW_{OS}.
4. Apply a known full scale voltage, V_{FS}, to the inputs.
5. Measure the output full scale pulse, PW_{FS}.
6. Subsequent measurements will give, to within ±0.00305% FSR, the input voltage according to the following equation:

$$V_{IN} = (\text{Pulse Out} - PW_{OS}) \times \frac{(V_{FS} - V_Z)}{(PW_{FS} - PW_{OS})} + V_Z$$

INPUT, GROUNDING, AND DECOUPLING CONSIDERATIONS

For most applications, the AD367 will be used with single-ended inputs and the internal −10V reference. The connections for this mode of operation are shown in Figure 7, including input buffering, power supply decoupling, and input ground sense. As with many data acquisition components, the AD367 has separate analog and digital grounds. These pins (15 and 17) are not connected internally, but should be tied together at one point as close to the converter as possible. Ideally, a single solid ground plane under the converter is desirable. Current flows through the wires and etch stripes of circuit cards, and since these paths have resistance and inductance, hundreds of millivolts can be generated between the system analog ground and the ground pins of the AD367. Separate wide conductor stripe ground returns should be provided for high resolution converters to minimize IR losses from current flow in the converter to system ground run. Care must be taken to prevent digital logic return currents from being summed into the same return path as analog signals to prevent measurement errors.

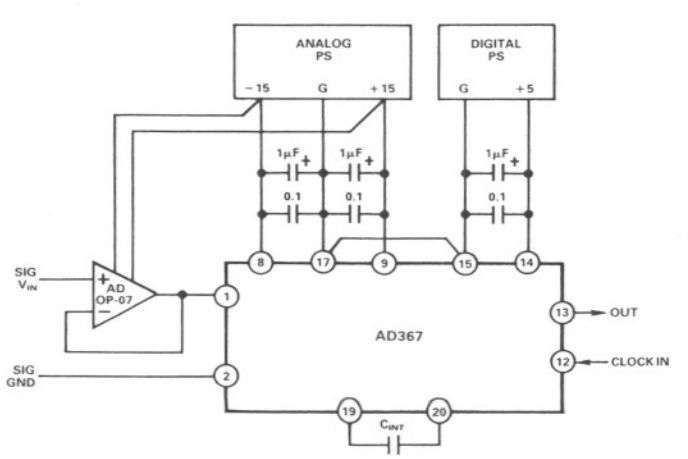


Figure 7. Input Connections for Single-Ended Operation

Each of the AD367's supply terminals should be capacitively decoupled as close to the AD367 as possible. A large value capacitor, such as 1µF, in parallel with a 0.1µF capacitor is usually sufficient. Analog supplies should be decoupled to the analog ground pin, and the logic supply to the digital ground pin.

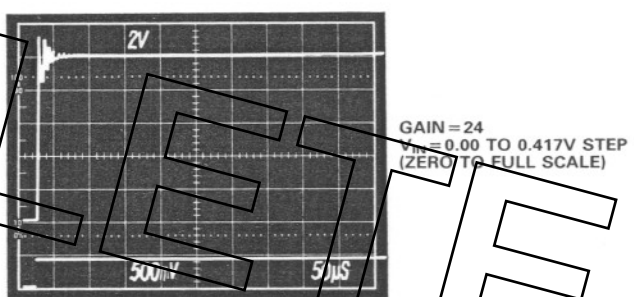


Figure 8. AD367 PGA Section Settling

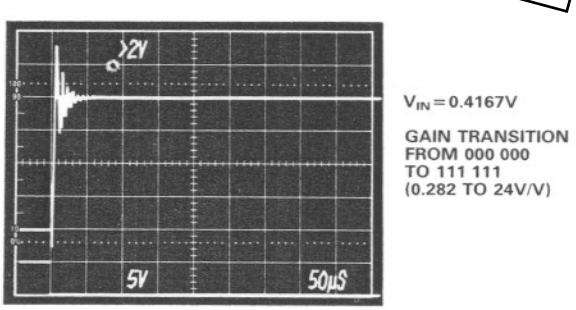


Figure 9. AD367 PGA Section Gain Settling

The metal case is at analog ground potential for shielding. Care should be exercised to prevent shorting to board circuitry beneath the part.

GENERAL INTERFACE CONSIDERATIONS

The control logic of the AD367 and the synchronous counter scheme shown in Figure 10 makes direct connection to most microprocessor buses possible. While it is impossible to describe the details of the interface connections for every microprocessor, a representative example is presented here.

Analog-to-digital converters, like any I/O device, may be interfaced to microprocessors by several methods. These include direct memory access (DMA), isolated or accumulator I/O, and memory-mapped I/O. DMA is the fastest, since conversions occur automatically and data updates into memory are transparent to the processor. DMA logic is very processor-dependent and requires specialized dedicated hardware.

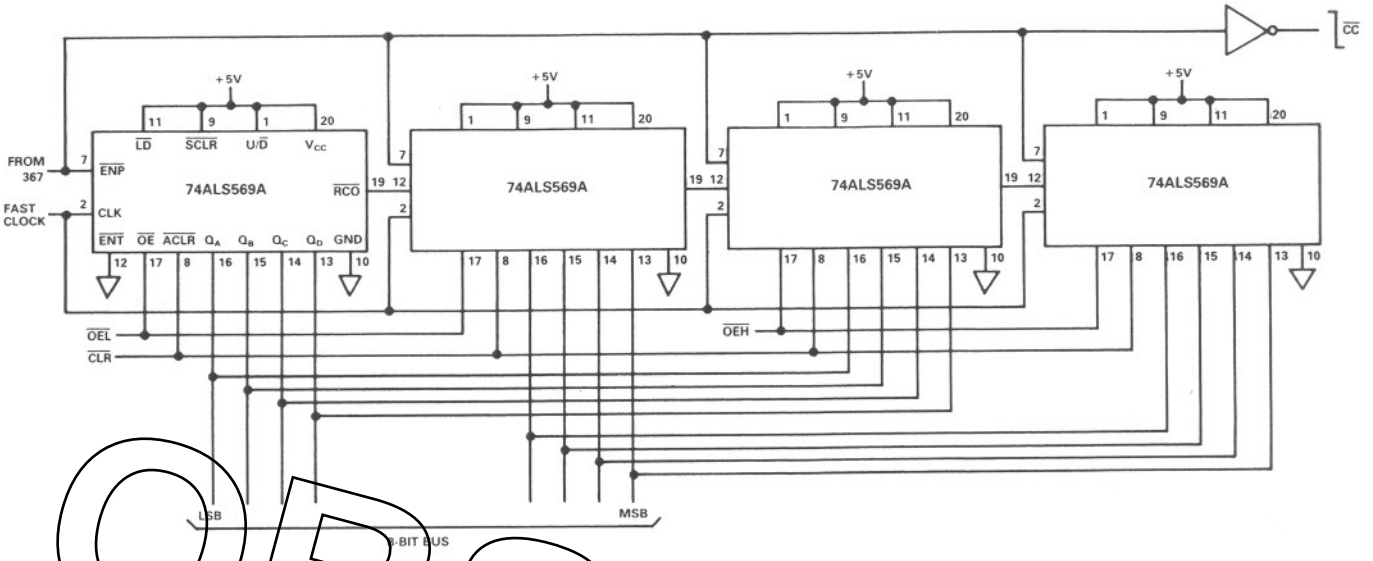


Figure 10. General Counter Scheme 8-Bit Bus

Memory-mapped and accumulator I/O are more often used and easier to implement. Accumulator I/O uses a distinct set of control signals which, combined with the address bus, define a totally separate I/O address space. The architecture is simple from a hardware standpoint, since address decoding requirements are not severe, and distinct I/O pulses are easily located for system debugging. However, processors using accumulator I/O can generally only send data to an output device from the accumulator. This can make for cumbersome software, since processor controlled transfers of I/O data to a memory location cannot be accomplished in a single instruction.

Memory-mapped I/O assigns the I/O device to one or more locations in the logical memory space of the microprocessor. This technique has the advantage that the full range of memory reference instructions may be used to operate on the data. The potential disadvantages include limiting the memory space available for program and data memory, somewhat more complex address decoding and more difficult isolation of device select pulses for system debugging. Nevertheless, many microprocessors offer only the memory-mapped I/O.

CONNECTING COUNTERS FOR DIGITAL OUTPUT

Figure 10 shows a simple circuit for converting the AD367 pulse width output to binary digital code using the 74LS569A synchronous counter. This scheme is compatible with μP systems using an 8-bit wide data bus structure, such as the 6809. It is easily upgraded to 16-bit structures by connecting OEH to OEL and connecting the 16 outputs directly to the bus instead of together.

Decode logic for the 6809μP is shown in Figure 11.

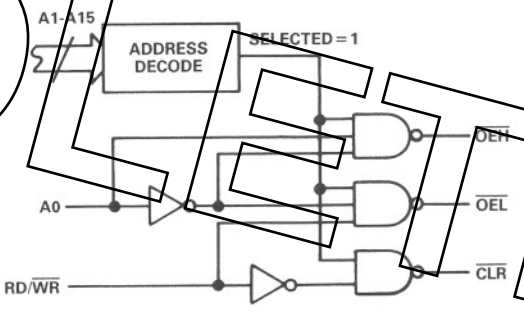
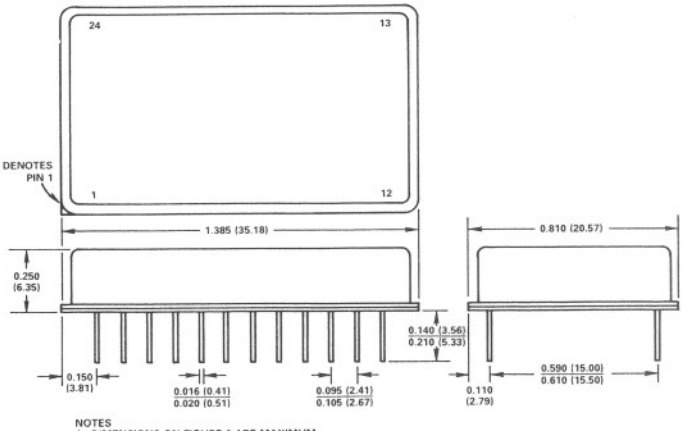


Figure 11. Decode Scheme for 6809

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



NOTES
A. DIMENSIONS ON FIGURE 2 ARE MAXIMUM
B. LEADS IN TRUE POSITION WITHIN 0.010"

PIN NUMBERS SHOWN FOR REFERENCE ONLY.

ORDERING GUIDE

Model	Linearity Error	Resolution	Temperature Range	Price (250)
AD367KM	±0.00305% FSR	±305μV	0 to +70°C	$116

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