ANALOG DEVICES

True 16-Bit Track-and-Hold Amplifier

AD386

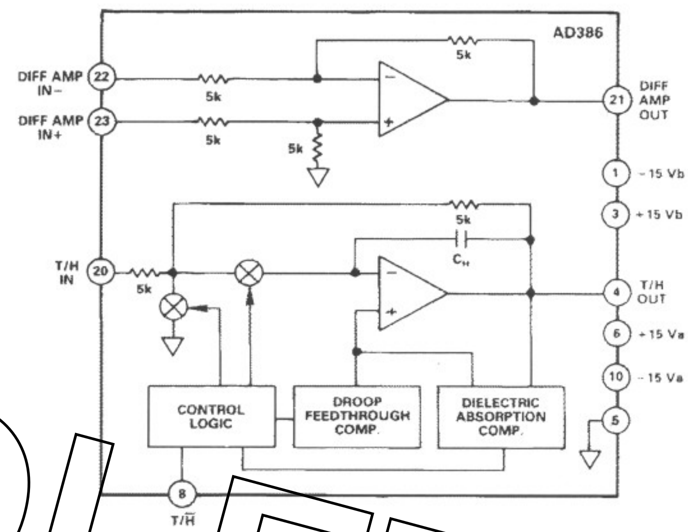
FEATURES

Companion to True 16-Bit A/D Converters
16-Bit Linear (−40°C to +85°C)
14-Bit Linear (−55°C to +125°C)
Fast Acquisition Time: 3.6 µs to 0.00076%
Low Droop Rate: 20 µV/ms
Differential Amplifier for Ground Sense
Low Aperture Jitter: 40 ps

APPLICATIONS

Medical and Analytical Instrumentation
Signal Processing
Multichannel Data Acquisition Systems
Automatic Test Equipment
Guidance and Control
Sonar

AD386 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD386 is a high accuracy, adjustment free track-and-hold amplifier designed for high resolution data acquisition applications. The fast acquisition time (3.6 µs to 75 µV) and low aperture jitter (40 ps) make it ideal for use with fast A/D converters.

The AD386 is complete with an internal hold capacitor, and it incorporates a compensation network which minimizes the track-to-hold charge offset and dielectric absorption. The AD386 also includes an internal differential amplifier for very high accuracy applications.

Typical applications for the AD386 include sampled data system, peak hold function, strobe measurement system and simultaneous sampling converter systems. When used with autozero and autocalibration techniques, this T/H combined with a high linearity A/D will offer true 16-bit performance (0.00076% linearity) over the industrial temperature range, and 14-bit performance (0.003% linearity) over the military temperature range.

REV. A

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AD386—SPECIFICATIONS (@ +25°C unless otherwise noted, V_S = ±15 V ± 10%)

Model	Conditions	AD386BD Min	AD386BD Typ	AD386BD Max	AD386TD Min	AD386TD Typ	AD386TD Max	Units
DIFFERENTIAL AMPLIFIER								
INPUT CHARACTERISTICS								
Input Range		±10			±10			V
Common-Mode Range		±10			±10			V
Input Resistance[1]								
Signal			5			5		kΩ
Ground Sense			10			10		kΩ
Offset[2]			0.6	**2.0**		0.6	**2.0**	mV
Offset Drift	T_{min} to T_{max}		10	30		10	30	μV/°C
CMRR	V_{CM} = ±10	**80**	90		**80**	90		dB
PSRR[3]		**76**	85		**76**	85		dB
TRANSFER CHARACTERISTICS								
Gain			−1			−1		V/V
Gain Error				**0.02**			**0.02**	%
Gain Error Drift	T_{min} to T_{max}		1	5		1	5	ppm/°C
Gain Linearity			0.0002	**0.00076**		0.0002	**0.00076**	%
Gain Linearity Drift	T_{min} to T_{max}		0.01	0.05		0.01	0.05	ppm/°C
Noise (ENBW = 1.8 MHz)			32	45		32	45	μV rms
DYNAMIC CHARACTERISTICS								
Small Signal Bandwidth			6			6		MHz
Slew Rate			65			65		V/μs
Settling Time[4]								
10 V Step to 1/2 LSB16			2.0	3.0				μs
10 V Step to 1/2 LSB14			0.8	1.5		0.8	1.5	μs
20 V Step to 1/2 LSB16			2.0	**3.0**				μs
20 V Step to 1/2 LSB16	T_{min} to T_{max}		2.0	3.0				μs
20 V Step to 1/2 LSB14			0.8	**1.5**		0.8	**1.5**	μs
20 V Step to 1/2 LSB14	T_{min} to T_{max}		0.8	1.5		0.8	1.5	μs
OUTPUT								
Voltage	R_{LOAD}>3.5 kΩ, T_{min} to T_{max}	±10			±10			V
Current	Short Circuit		15			15		mA
POWER SUPPLY								
Rated Performance			±15			±15		V
Operating Range		±5		±18	±5		±18	V
Quiescent Current			4.2	**5.0**		4.2	**5.0**	mA
TRACK-AND-HOLD								
INPUT CHARACTERISTICS								
Input Range		±10			±10			V
Input Resistance[1]			5			5		kΩ
Offset[2]			0.6	**2.0**		0.6	**2.0**	mV
Offset Drift	T_{min} to T_{max}		10	30		10	30	μV/°C
TRANSFER CHARACTERISTICS								
Gain			−1			−1		V/V
Gain Error				**0.02**			**0.02**	%
Gain Error Drift	T_{min} to T_{max}		1	5		1	5	ppm/°C
Gain Linearity			0.0002	**0.00076**		0.0002	**0.00076**	%
Gain Linearity Drift	T_{min} to T_{max}		0.01	0.05		0.01	0.05	ppm/°C
PSRR[3]		**76**	85		**76**	85		dB
DYNAMIC CHARACTERISTICS								
Small Signal Bandwidth			2			2		MHz
Slew Rate			15			15		V/μs
TRACK-TO-HOLD SWITCHING								
Pedestal + Offset			0.5	**1.5**		0.5	**1.5**	mV
Pedestal + Offset	T_{min} to T_{max}			5.0			7.5	mV
Pedestal Linearity	T_{min} to T_{max}		0.0004	0.00076		0.0004	0.003	%
Aperture Delay			12			12		ns
Aperture Jitter			40			40		ps
Transient Settling[4]								
to 1/2 LSB16	T_{min} to T_{max}		600	**800**				ns
to 1/2 LSB14	T_{min} to T_{max}		400	**500**		400	**500**	ns

Model	Conditions	AD386BD Min	AD386BD Typ	AD386BD Max	AD386TD Min	AD386TD Typ	AD386TD Max	Units
HOLD MODE								
Droop Rate			20	**100**		20	**100**	mV/s
Droop Rate	T_{max}		0.2	1.0		3.6	18	V/s
Feedthrough[5]			−99	**−94**		−99	**−94**	dB
Noise (ENBW = 1.7 MHz)			32	50		32	50	µV rms
PSRR[3]		**60**	66		**60**	66		dB
Dielectric Absorption[6]			7	**10**		7	**10**	ppm
HOLD-TO-TRACK DYNAMICS								
Acquisition Time[4]								
10 V Step to 1/2 LSB16			3.6	4.1				µs
10 V Step to 1/2 LSB14			3.1	3.6		3.1	3.6	µs
20 V Step to 1/2 LSB16			3.6	**4.1**				µs
20 V Step to 1/2 LSB16	T_{min} to T_{max}		4.0	4.5				µs
20 V Step to 1/2 LSB14			3.1	**3.6**		3.1	**3.6**	µs
20 V Step to 1/2 LSB14	T_{min} to T_{max}		3.5	4.0		4.0	4.5	µs
DIGITAL INPUTS								
V_{IH}	T_{min} to T_{max}	**3.5**			**3.5**			V
V_{IL}	T_{min} to T_{max}			**0.9**			0.9	V
I_{IH}	T_{min} to T_{max}	**−10**		**+10**	**−10**		**+10**	µA
I_{IL}	T_{min} to T_{max}	**−10**		**+10**	**−10**		**+10**	µA
OUTPUT								
Voltage	$R_{LOAD} > 3.5$ kΩ, T_{min} to T_{max}	±10			±10			V
Current	Short Circuit		15			15		mA
POWER SUPPLY								
Rated Performance			±15			±15		V
Operating Range		±8		±18	±8		±18	V
Quiescent Current								
Positive Supply			8.0	**12.0**		8.0	**12.0**	mA
Negative Supply		**−6.0**	−5.4		**−6.0**	−5.4		mA
SYSTEM								
Gain Linearity	T_{min} to T_{max}		0.0003	0.0012		0.0003	0.0012	%
Acquisition Time[4, 7]								
20 V Step to 1/2 LSB16			4.1	5.1				µs
20 V Step to 1/2 LSB16	T_{min} to T_{max}		4.5	5.4				µs
20 V Step to 1/2 LSB14			3.2	3.9		3.2	3.9	µs
20 V Step to 1/2 LSB14	T_{min} to T_{max}		3.6	4.3		4.1	4.8	µs
Power Dissipation			312	435		312	435	mW
TEMPERATURE RANGE								
Operating		−40		+85	−55		+125	°C
Storage		−60		+150	−60		+150	°C

NOTES
[1]Typical resistance tolerance is ±25%.
[2]After 5 minute warmup at +25°C.
[3]Test conditions: $+V_S = +15$ V, $-V_S = -16$ V to -14 V and $+V_S = +14$ V to $+16$ V, $-V_S = -15$ V.
[4]$R_{LOAD} = 5$ kΩ, $C_{LOAD} = 10$ pF, settling measured to 1/2 LSB at output.
[5]Measured at 1 kHz.
[6]Dielectric Absorption represents the magnitude of long-term settling artifacts for hold times up to 80 µs as a fraction of the difference in voltages between two successive held samples.
[7]Specifications also apply for 10 V step.

Specifications subject to change without notice.
Specifications in **bold** are 100% production tested.

AD386

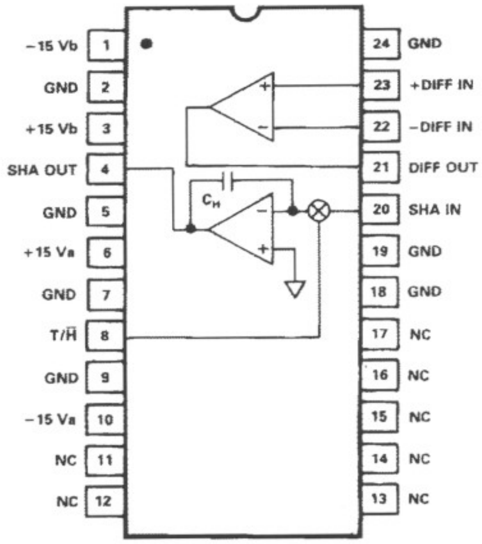
ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . ±18 V
Internal Power Dissipation . . . . 800 mW
Input Voltage[2] . . . . ±18 V
T/$\overline{H}$ Input Voltage . . . . −0.5 V, + 16 V
Output Short Circuit Duration . . . . Indefinite
Storage Temperature Range . . . . −65°C to +150°C
Operating Temperature Range
  AD386B . . . . −40°C to +85°C
  AD386T . . . . −55°C to +125°C
Lead Temperature Range (Soldering 60 sec) . . . . +300°C

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]For supply voltages less than ±18 V, the absolute maximum input voltage is equal to the supply voltage.



NC= NO CONNECT
±15 Vb – DIFF AMP ONLY
±15 Va – SHA ONLY

AD386 Pin Configuration

ORDERING GUIDE

Model	Max Linearity Error	Temperature Range	Package Option*
AD386BD	0.00076% FSR	−40°C to +85°C	DH-24B
AD386TD	0.003% FSR	−55°C to +125°C	DH-24B
AD386TD/883B	0.003% FSR	−55°C to +125°C	DH-24B

*DH-24B = Ceramic DIP.

Typical Performance Characteristics

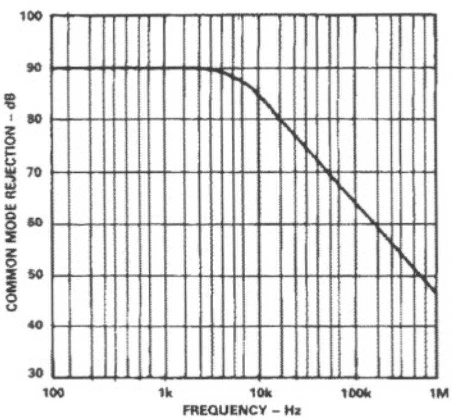


Figure 1. Differential Amplifier Common Mode Rejection vs. Frequency

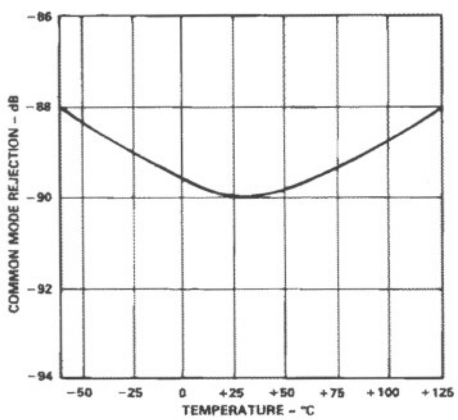


Figure 2. Differential Amplifier Common Mode Rejection vs. Temperature (100 Hz)

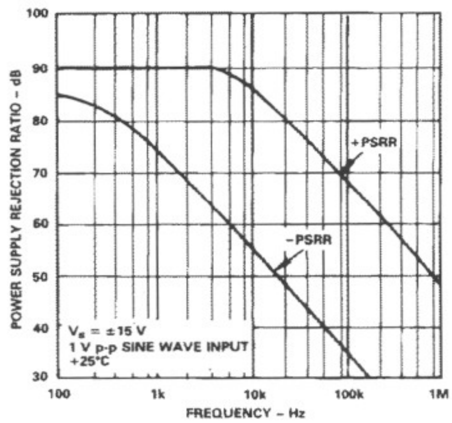


Figure 3. Differential Amplifier Power Supply Rejection vs. Frequency

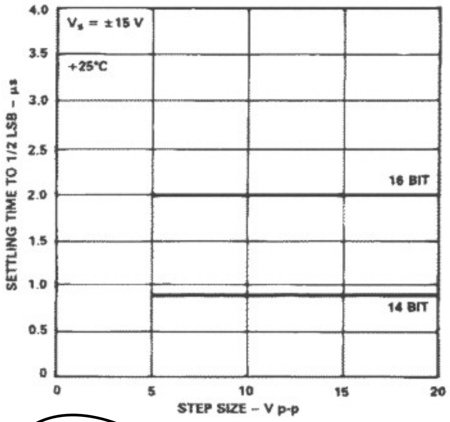


Figure 4. Differential Amplifier Settling Time vs. Step Size

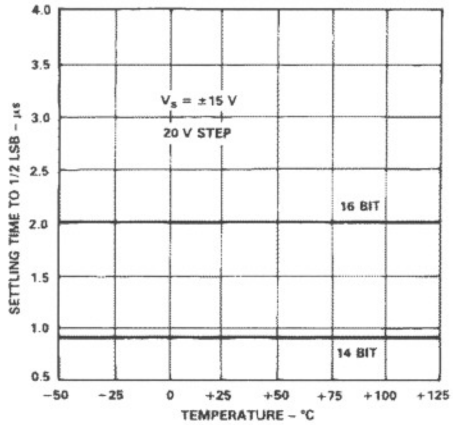


Figure 5. Differential Amplifier Settling Time vs. Temperature

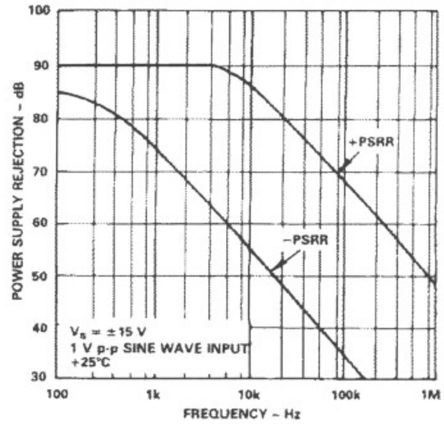


Figure 6. T/H Power Supply Rejection vs. Frequency, Track Mode

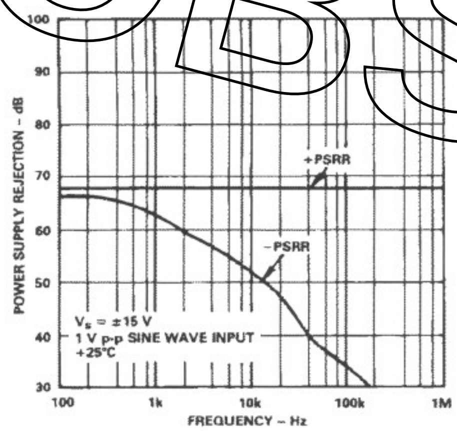


Figure 7. T/H Power Supply Rejection vs. Frequency, Hold Mode

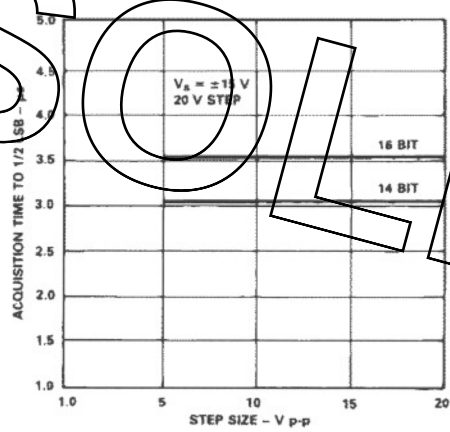


Figure 8. T/H Acquisition Time vs. Step Size

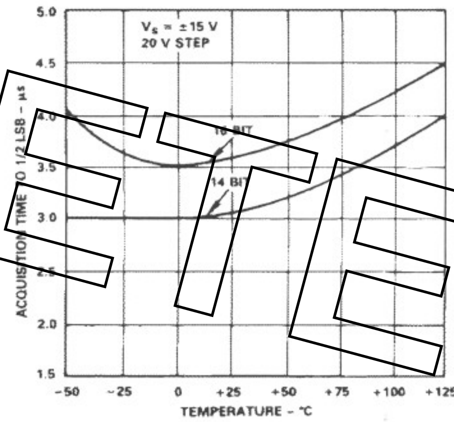


Figure 9. T/H Acquisition Time vs. Temperature

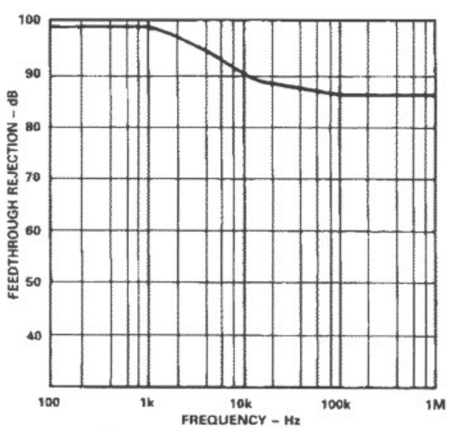


Figure 10. Feedthrough vs. Frequency

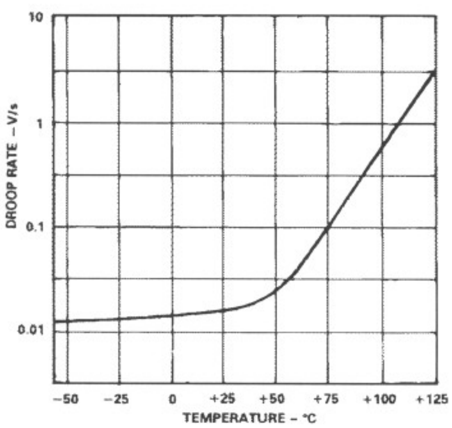


Figure 11. Droop Rate vs. Temperature

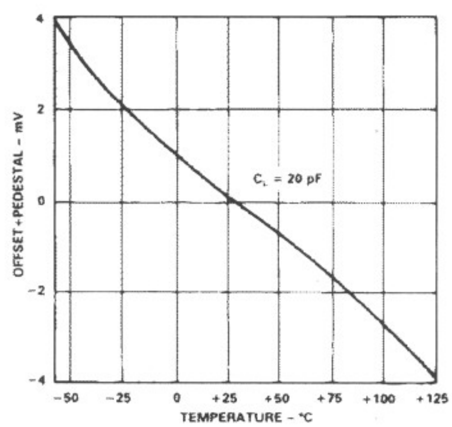


Figure 12. (Pedestal+Offset) vs. Temperature

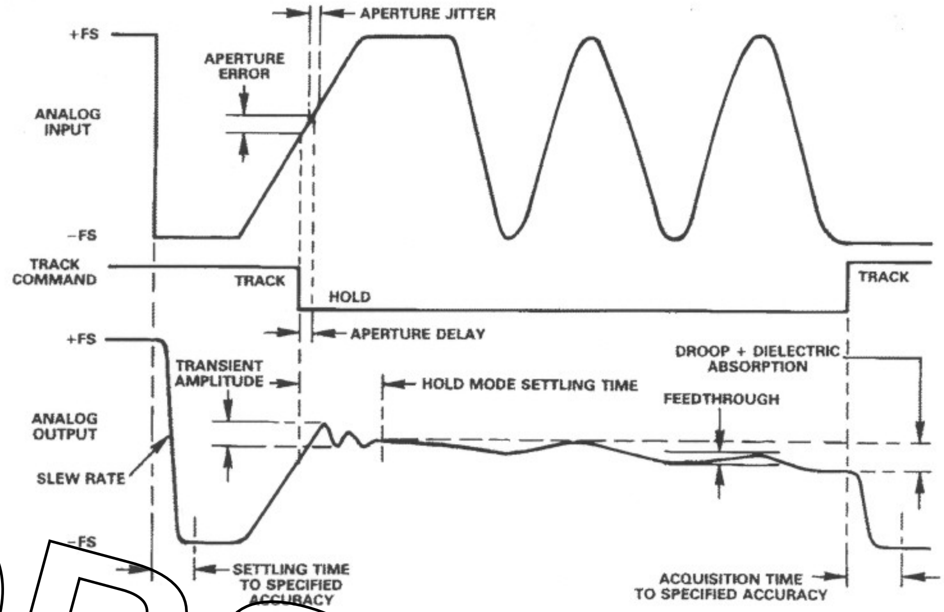


Figure 13. T/H Characteristic Features

TERMINOLOGY

Aperture Delay: the time required by the internal switch(es) to disconnect the hold capacitor from the input, which produces an effective delay in the sample timing.

Aperture Jitter: the uncertainty in Aperture Delay caused by internal noise and the variation of switching thresholds with signal level. The error caused by aperture jitter depends on the rate of change of the input and as such determines the maximum input frequency which can be sampled without error.

Pedestal: a step change in the output voltage which occurs when switching from track mode to hold mode.

Hold Mode Settling Time: the time required for the pedestal to reach its final value to within a specified fraction of full scale.

Droop: the change in the held output voltage resulting from leakage currents.

Feedthrough: the fraction of input signal variation which appears at the output in hold mode as a result of capacitive coupling.

Dielectric Absorption: the tendency of charges within a capacitor to redistribute themselves over time, resulting in "creep" in the voltage of an open circuit capacitor after a large rapid change.

Acquisition Time: the time required after entering track mode for the voltage on the hold capacitor to settle to within a specified fraction of full scale. This is usually specified for a full-scale step change in output voltage.

Settling Time: the time required in track mode for the output to reach its final value within a specified fraction of full scale following a step change in the input voltage.

Nonlinearity: the degree to which a plot of output versus input deviates from the straight line defined by the end points. It is usually specified as a percentage of full scale.

THEORY OF OPERATION

The architecture of the AD386 differs from that usually encountered in inverting Track-and-Hold (T/H) circuits. The hold capacitor in a conventional T/H (Figure 14) is always connected from the amplifier's output to its inverting input. In track mode switch A is open and switch B is closed. Since the summing junction is a virtual ground, the voltage across the capacitor follows the input. The switches change state in hold mode which disconnects the capacitor from the input and holds the output voltage constant. The clamping action of switch A reduces the variations across switch B, improving feedthrough performance.

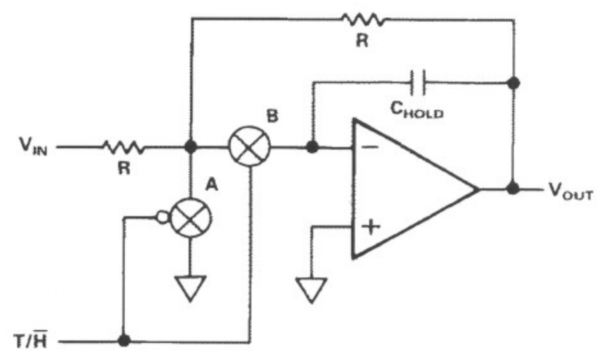


Figure 14. Conventional Inverting Integrator T/H

This circuit forces several tradeoffs. The hold capacitor's charging current is limited by the input resistor. Either the resistor or the capacitor, or both, must be made small to obtain fast acquisition times. A small resistor creates greater demands on the circuit which drives the T/H, while a small capacitor leads to increased pedestal and droop. In addition, the parallel combination of the feedback resistor and the hold capacitor acts as a low pass filter and constrains both bandwidth and acquisition time.