AD4111/AD4112/AD4114/AD4115 Frequently Asked Questions (FAQs)

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Q1. What is the difference between the AD4111/AD4112/AD4114/AD4115?

AD4111 and AD4112 are pin compatible and have an almost identical feature set except the AD4111 has a unique solution for open wire detection from a single 3.3V/5V supply. Details can be found on page 27 in the Open Wire Detection section of the AD4111 datasheet. AD4114 and AD4115 support voltage inputs only allowing more voltage channel counts as compared to AD4111/AD4112 which support both voltage and current inputs. The AD4115 runs at a higher speed than the rest of the family. Key differences are summarized in Table 1 below.

Q2. On the AD4111/AD4112/AD4114/AD4115 can I detect if the input signals are floating due to faulty wiring?

AD4111 provides a unique solution for open wire detection on the voltage inputs from a single 5V/3.3V supply. Open wire detection is calculated by comparing the difference between the two channel conversions to a certain threshold. Details can be found on page 27 in the Open Wire Detection section of the AD4111 datasheet.

AD4112/AD4114/AD4115 do not have built in open wire detection feature.

Q3. What is the recommended anti-aliasing filter required for the AD4111/AD4112/AD4114/AD4115?

For the AD4111/ AD4112/AD4114/AD4115 the recommend anti-aliasing is 4.7nF/180Ω as this combination will give you the optimum performance and were used in the EMC evaluation.

For AD4111, when using open wire detection on voltage inputs, a 1kΩ resistor and 680pF capacitor should be placed between voltage pins and compensation pins. The value of the anti-aliasing filter can be changed but the 680pF compensation capacitor must be taken into consideration. See Figure 1.

Note that one should always consider the effect of a resistor connected in series with the internal input resistance of the AD411x. This will affect the divider ratio resulting in a gain error. The nominal internal resistor value for AD4111/AD4112 is 1.17MΩ and may vary from part to part. If for example the 180 resistor is used then this would introduce a worst-case error of 180/1170000 * 100 = 0.015%, however this additional error can be removed by a system calibration or by adjusting the Gain register appropriately. For more details about calibration, please see Calibration section of the AD4111/AD4112/AD4114/AD4115 datasheet.

Table 1. AD411x Summary

Specification/ Product	Voltage Measurement Channel	Current Measurement Channel	Speed (SPS)	VIN Max Ratings	AVDD Supply	Open wire Detection
AD4111	4 Differential/ 8 Single Ended	4 Single Ended 0 to 20mA	31,250	±50V	3V to 5.5V	YES
AD4112	4 Differential/ 8 Single Ended	4 Single Ended 0 to 20mA	31,250	±50V	3V to 5.5V	N/A
AD4114	8 Differential/ 16 Single Ended	N/A	31,250	±65V	3V to 5.5V	N/A
AD4115	8 Differential/ 16 Single Ended	N/A	125,00	±65V	4.5V to 5.5V	N/A

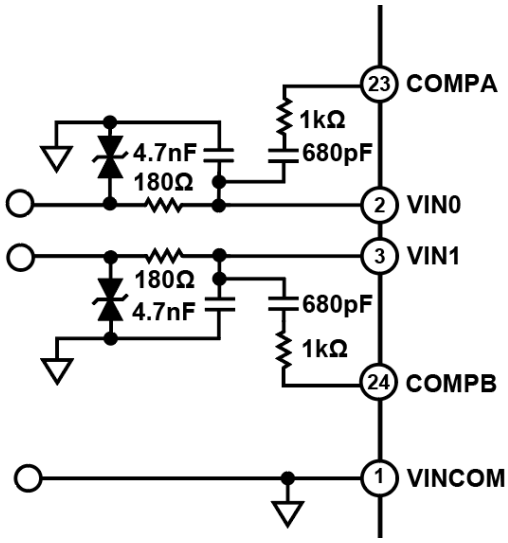

Figure 1. Antialiasing RC filter with Open wire detection

Q4. Will the same anti alias filter work for both voltage and current inputs of AD4111/AD4112?

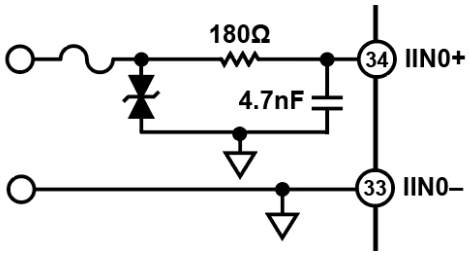

Figure 2. Antialiasing RC filter

The current inputs do not have any special considerations and thus can use the same anti alias RC filter as voltage inputs, 4.7nF/180Ω. Just note that a 180 Ω resistor in series with 60 Ω impedance of the AD4111 /AD4112 current input results in a typical total input impedance of 250Ω.

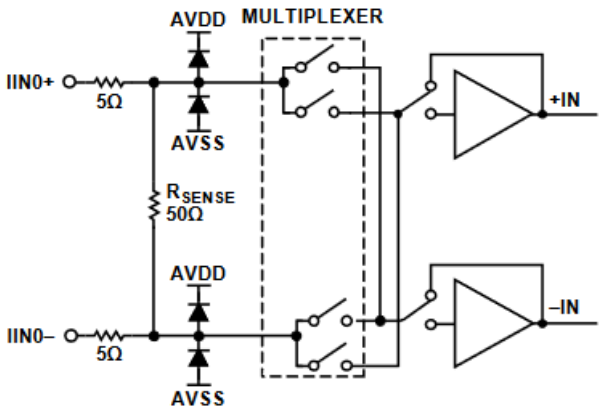

Figure 3. Simplified Current input circuit

Q5. Why are the onboard Analog input buffers not required for current measurements AD4111/AD4112?

To enable currents to be measured below 0mA, the Analog input buffers should be disabled for current measurement. This would extend the ADC input range to -0.05V below ground and allows accurate measurements of currents close to and below 0mA. If the measurement range is always above 0mA then input buffers can be enabled but are not required.

Q6. Can the AD4111/AD41112 current channels accept a bipolar (±20mA) inputs?

The current input range is specified from -0.5mA to 24mA using a single supply. However, the part can accept a true bipolar inputs when it operates with a split supply ±2.5V.

Q7. What is the AD4111/AD41112 current channels common-mode input?

The absolute input voltage per IINx pin is from AVSS-0.05V to AVDD+0.05V when input buffers are disabled. The maximum current between IINx+ and IINx- for specified performance is +24mA, therefore the upper voltage limit can only be reached if IINx- is biased to a non-zero voltage. Connecting the IIN- pin to AVSS/GND ensures that for the entire current input range the absolute input voltage at each pin are always within specification.

Q8. Why are the Analog input buffers required for voltage measurements AD4111/AD4112/AD4114/AD4115?

The Analog input buffers should be enabled for voltage Analog inputs as these provide a low source impedance to the sampling ADC. If these buffers were disabled, then a large resistance would exist. This combined with any parasitic capacitance from the resistive front end driving the ADC input will result in a very large gain error.

Q9. What's the equivalent input impedance for a pair of voltage input pins of AD4111/AD4112/AD4114/AD4115?

Below is the detailed figure of the voltage input stage. Please take note that the 10MΩ is not relevant to the VIN 1/10X transfer function, and is already accounted for in the 1 MΩ minimum input impedance spec. The resistor die used the 10MΩ resistors for the Open-Wire-Detect function on AD4111. It is present on the AD4112 VINs, but the other end is internally connected to AVSS. Therefore, the differential input impedance of AD4111/AD4112 has an approximate nominal value of 2.34 MΩ and may vary from part to part. The differential resistance range is higher on AD4114/AD4115 because without the10MΩ, the nominal input impedance is 1.33MΩ, therefore the differential impedance is 2.66MΩ.

Q10. What's the maximum VIN input voltage range allowed for AD4111/AD41112/AD4114/AD4115?

The AD4111/AD4112/AD4114 is specified for analog input voltages within the ±10V differential input voltage range and is functional up to a differential input signal of ±VREF× 10 for a supply voltage of 3V to 5.5V.

However, the specified absolute (pin) voltage must not be exceeded for the proper function. This absolute pin voltage is directly dependent on the supply voltage used.

When the AVDD=>4.75V (e.g. 5V) the allowed input pin voltage range is up to ±20V, however for supply voltages below this to AVDD=3V (e.g. 3.3V) the allowed input pin voltage range is up to ±12V only.

The AD4115 also operate within the ±10V differential input voltage range and is functional up to a differential input signal of ±VREF× 10. However, AD4115 can only operate with AVDD from 4.5V to 5.5V, thus the absolute input pin voltage range is up to ±20V.

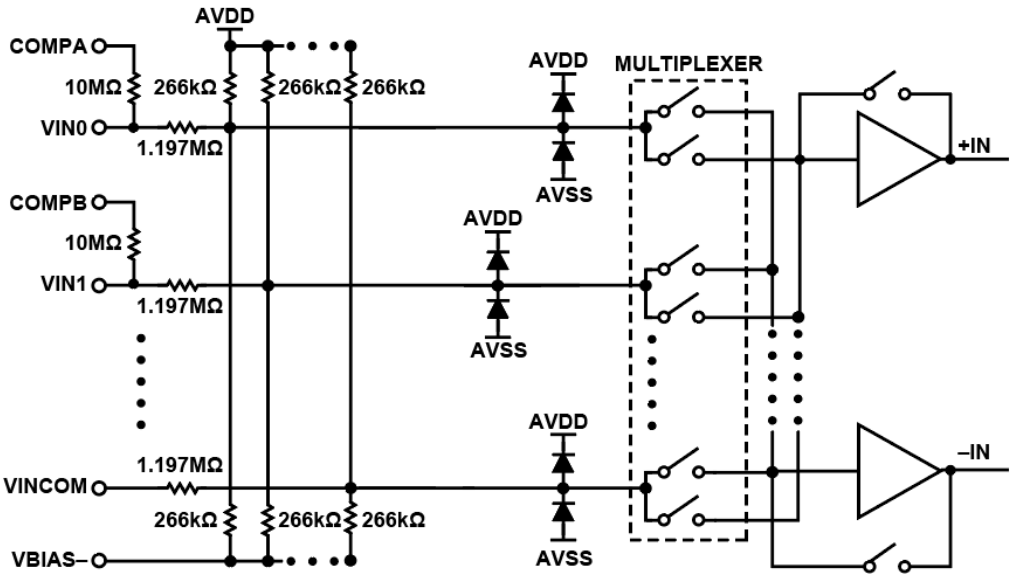

Figure 4. Simplified Voltage input circuit of AD4111/AD4112 (Note that COMPA and COMPB pins are DNC pins in AD4112 but nodes in the diagram are internally connected to AVSS)

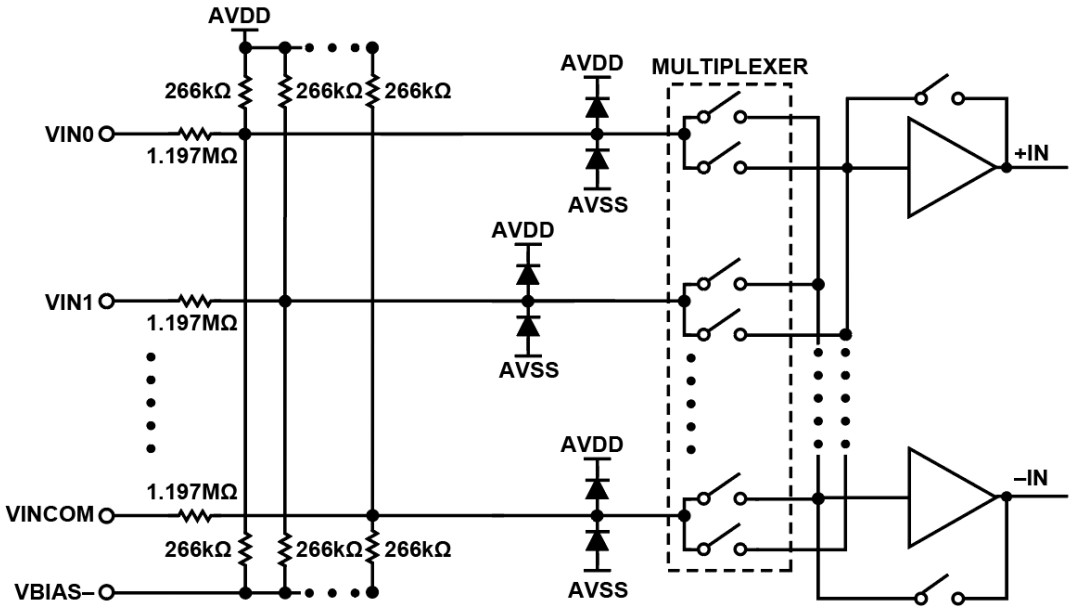

Figure 5. Simplified Voltage input circuit of AD4114/AD4115

Q11. On the AD4111/AD4112/AD4114/AD4115 what's the equivalent TUE (total uncompensated error) spec across different input voltage ranges for example ±10V, ±5V, ±2.5V or 0-10V, 0-5V, 0-2.5V?

AD4111/AD41112/AD4114/AD4115 are specified for a TUE spec at ±10V full scale range. When input span is reduced the error will change as TUE is specified as a percentage of Full-scale range (%FSR).

In order to calculate the equivalent TUE spec for smaller ranges, we would take the assumption that gain-error and offset error both account for 50% of the total TUE. Please take note that this method provides only an estimated value, the actual performance could be better or worse as we only guaranteed the TUE spec at ±10V input range.

We can start by working through the errors in mV or V initially and then translating to a final TUE Specification

If we take an input span of ±10V and take the TUE from the datasheet specification for ±10V input at 25°C.

For **AD4111/AD4112**, TUE specs at 25°C is 0.06% Thus,

Offset error = 0.03% of 20V span =>6mV

Full-Scale error at +10V (after correcting for offset error) = 0.03% of 20V span =>6mV

TUE = (6mV+6mV)/20 *100 = 0.06%

For **AD4114/AD4115**, TUE specs at 25°C is specified as 0.07%. Taking the same steps as above will give you

Offset error = 0.035% of 20V span =>7mV

Full-Scale error at +10V (after correcting for offset error) = 0.035% of 20V span =>7mV

TUE = (7mV+7mV)/20 *100 = 0.07%

Table 2 shows the TUE estimation at 25°C across different ranges. The same approach can be applied when calculating TUE across different temperature.

Table 2. AD411x TUE estimation at 25°C

Input span	AD4111/AD4112	AD4114/AD4115
±5V	Offset error = 6mV; Full-Scale error = 6mV*(5V/10V) = 3mV; TUE = (6mV + 3mV)/10 *100 = 0.09%	Offset error = 7mV; Full-Scale error = 7mV*(5V/10V) = 3.5mV; TUE = (7mV + 3.5mV)/10 *100 = 0.105%
±2.5V	Offset error = 6mV; Full-Scale error = 6mV*(2.5V/10V) = 1.5mV; TUE = (6mV + 1.5mV)/5 *100 = 0.15%	Offset error = 7mV; Full-Scale error = 7mV*(2.5V/10V) = 1.75mV; TUE = (7mV + 1.75mV)/5 *100 = 0.175%
0 – 10 V	Offset error = 6mV; Full-Scale error = 6mV*(10V/10V) = 6mV; TUE = (6mV + 6mV)/10 *100 = 0.12%	Offset error = 7mV; Full-Scale error = 7mV*(10V/10V) = 7mV; TUE = (7mV + 7mV)/10 *100 = 0.14%
0 – 5 V	Offset error = 6mV; Full-Scale error = 6mV*(5V/10V) = 3mV; TUE = (6mV + 3mV)/5 *100 = 0.18%	Offset error = 7mV; Full-Scale error = 7mV*(5V/10V) = 3.5mV; TUE = (7mV + 3.5mV)/5 *100 = 0.21%
0 – 2.5 V	Offset error = 6mV; Full-Scale error = 6mV*(2.5V/10V) = 1.5mV; TUE = (6mV + 1.5mV)/2.5 *100 = 0.3%	Offset error = 7mV; Full-Scale error = 7mV*(2.5V/10V) = 1.75mV; TUE = (7mV + 1.75mV)/2.5 *100 = 0.35%

Q12. What is the difference in output data rate between multiple channel configuration and single channel configurations for AD4111/AD4112/AD4114/AD4115?

The AD4111/AD4112/AD4114/AD4115 can run at faster output data rates when converting on a single channel. When multiple channels are enabled the digital filter must settle fully for each channel and therefore the result is a slower output data rate.

As an example, **For AD4111/AD4112/AD4114:** When the filter is configured to Sinc5+Sinc1 and the fastest output data rate of 31250 SPS is selected.

For a single channel the effective output data rate is 31250 SPS, the time between conversions is 1/ODR = 32us. If "SING_CYC" bit is set or If more than one channel is enabled for the same filter configuration i.e. 31250 SPS then the time between conversions is 161us, because the digital filter must fully settle for each output. For more details about the timing you can download and view the AD4111 Filter Model.

For AD4115: When the filter is configured to Sinc5+Sinc1 and the fastest output data rate of 125000 SPS is selected.

For a single channel the effective output data rate is 125000 SPS, the time between conversions is 1/ODR = 8us. If "SING_CYC" bit is set or If more than one channel is enabled for the same filter configuration i.e. 125000 SPS then the time between conversions is 40.25us, the delay required is due to the filter settling time. For more details about the timing you can download and view the AD4115 Filter Model.

Q13. What is the SPI mode of operation of the AD4111/AD4112/AD4114/AD4115, what polarity do I need to consider?

The interface operates in SPI Mode 3 (CPOL=1, CPHA=1) wherein SCLK idles high, the falling edge of SCLK is the drive edge, and the rising edge of SCLK is the sample edge. Data is clocked out on the falling/drive edge and data is clocked in on the rising/sample edge.

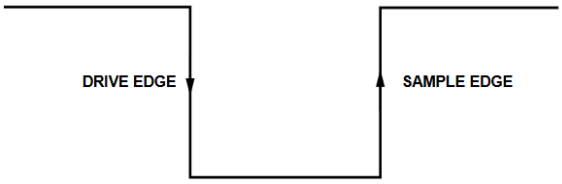

Figure 6. SPI Mode 3

Q14. Where can I find a full and workable sample codes for AD4111/AD4112/AD4114/AD4115 for a ST processor?

We have firmware example code with SDP-K1 EVAL board available on the link below.

ad717x_ad411x_mbed_example

The firmware provides a basic user-interface for interacting with the evaluation-board as it waits for user input over serial interface (UART). All the main functionality of the AD411x is provided in the application-code in abstracted form and the user is free to customize the software to suit their own needs for working with the AD411x.

Q15. What is the recommended initialization and register configuration sequence for AD4111/AD4112/AD4114/AD4115?

On power-up, it is advisable to perform a reset by writing 64 consecutive ones to the part.

This will reset the serial interface, and it will also reset the on-chip registers to their default conditions. The device does have a power-on reset function. However, any glitches during power-up can cause corruption of the registers, therefore a reset in the initialization routine is advisable.

After the reset, the device can be configured for the application. Please refer to AD4111/AD4112/AD4114/AD4115 Datasheet Register map section.

The recommended flow is as follows:

1. Write to Channel Configuration (Select input and setup for each ADC channel, enable open wire detection in GPIO configuration)
2. Write to Setup Configuration (Select Filter order, Output data rate, etc.)
3. Write to ADC Mode and Interface Mode Configuration (Select ADC operating mode, Clock source, enable CRC, Data+Status, etc.)

Q16. How many data registers does the AD4111/AD4112/AD4114/AD4115 have to store conversion results for each channel?

The AD411x devices have one data register, therefore only one conversion result is stored at any given time. When several channels are enabled, the ADC will automatically sequence through the enabled channels, performing one conversion on each channel before moving to the next. Therefore, it is important to ensure the current conversion result is read before the next conversion is complete. The data register is updated as soon as each conversion is available. The DRDY/RDY output pulses low each time a conversion is available. The user can then read the conversion while the ADC converts the next enabled channel. Figure 7 shows an example of timing diagram when ADC is in continuous conversion mode.

For more details please reference the product pages AD4111/AD4112/AD4114/AD4115 or Engineer Zone

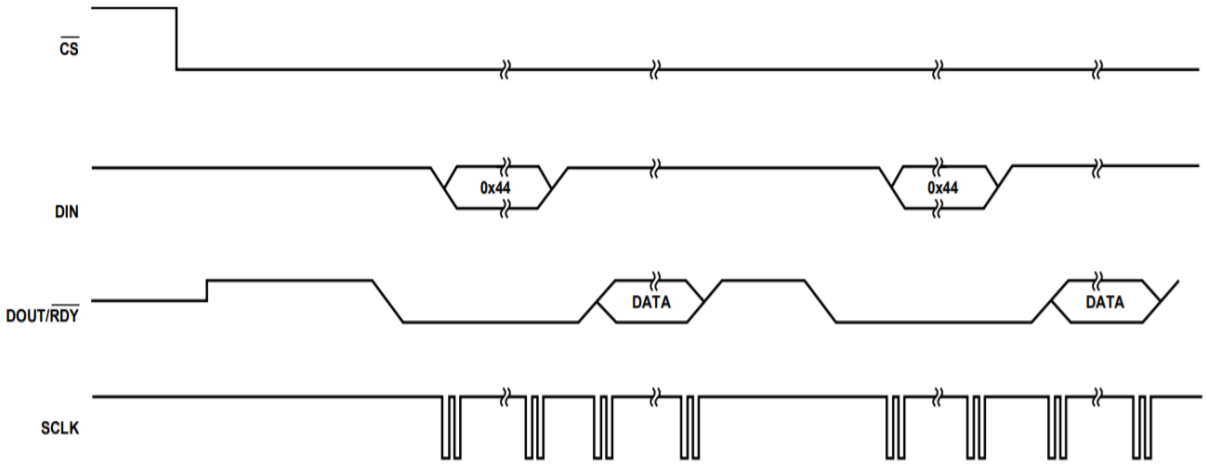

Figure 7. Continuous conversion mode