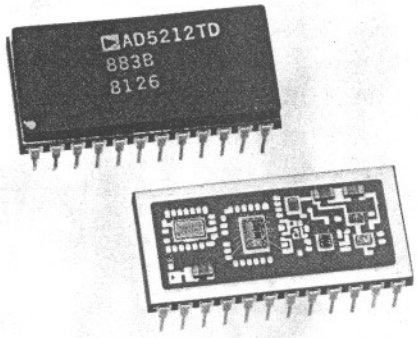
12-Bit Successive Approximation High Accuracy A/D Converter

AD5210 SERIES

FEATURES

- True 12-Bit Operation: ±1/2LSB max Nonlinearity
- Totally Adjustment-Free
- Guaranteed No Missing Codes Over the Specified Temperature Range
- Hermetically-Sealed Package
- Standard Temperature Range: –25°C to +85°C
- Military Temperature Range: –55°C to +125°C
- MIL-STD-883 Processing Available
- Serial and Parallel Outputs
- Monolithic DAC with Scaling Resistors for Stability
- Low Chip Count for High Reliability
- Industry Standard Pin Out
- Small 24-Pin DIP



GENERAL DESCRIPTION

The AD5210 series devices are 12-bit successive approximation analog-to-digital converters. The hybrid design utilizes MSI digital, linear monolithic chips and active laser trimming of high-stability thin-film resistors to provide a totally adjustment free converter—no potentiometers are required for calibration.

The innovative design of the AD5210 series devices incorporates a monolithic 12-bit feedback DAC for reduced chip count and higher reliability. The exceptional temperature coefficients of the monolithic DAC guarantees ±1/2LSB linearity over the entire operating temperature range of –25°C to +85°C for the commercial grade and –55°C to +125°C for the military grade.

The AD5210 series converters are available in 2 input voltage ranges: ±5V (AD5211/AD5214) and ±10V (AD5212/AD5215). The converters are available either complete with an internal buried zener reference or with the option of an external reference for improved absolute accuracy.

The AD5210 series converters are available in two performance grades; the "B" is specified from –25°C to +85°C and the "T" is specified from –55°C to +125°C. The "B" and "T" grades are also available processed to MIL-STD-883 level B requirements. All units are available in a 24-pin hermetically sealed ceramic DIP.

PRODUCT HIGHLIGHTS

1. The AD5210 series devices are laser trimmed at the factory to provide a totally adjustment free converter—no potentiometers are required for 12-bit performance.
2. A monolithic 12-bit feedback DAC is used for reduced chip count and higher reliability.
3. The AD5210 series directly replaces other devices of this type with significant increases in performance.
4. The devices offer true 12-bit accuracy and exhibit no missing codes over the entire operating temperature range.
5. The fast conversion rate of the AD5210 series makes it an excellent choice for applications requiring high system throughput rates.

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SPECIFICATIONS (typical @ +25°C, ±15V and +5V unless otherwise noted)

INPUT RANGE[1]	INPUT IMPEDANCE				
−5V to +5V	5.0kΩ	AD5211B	AD5211T	AD5214B	AD5214T
−10V to +10V	10.0kΩ	AD5212B	AD5212T	AD5215B	AD5215T
REFERENCE		Internal	*	External −10.000V	***
RESOLUTION		12 Bits	*	*	*
LINEARITY MAX		±1/2LSB	*	*	*
No Missing Codes T_{min} to T_{max}		Guaranteed	*	*	*
ZERO ERROR, MAX		±1LSB	*	*	*
ZERO ERROR, MAX T_{min} to T_{max}		±2LSB	*	*	*
ABSOLUTE ACCURACY, MAX		±2LSB	*	*	*
ABSOLUTE ACCURACY, MAX T_{min} to T_{max}		±0.4% of FSR[2]	*	±0.1% of FSR[2]	***
CONVERSION TIME, MAX Clock = 1MHz		13μs	*	*	*
LOGIC RATINGS					
Input Logic Commands					
Logic "0"		0.8V max	*	*	*
Logic "1"		+2.0V min	*	*	*
Loading		0.5TTL Load	*	*	*
CLOCK INPUT PULSE WIDTH		100ns min	*	*	*
OUTPUT LOGIC					
Logic "0"		0.4V max	*	*	*
Logic "1"		3.6V (2.4 min)	*	*	*
FANOUT - HIGH		8TTL Loads	*	*	*
FANOUT - LOW		2TTL Loads	*	*	*
POWER SUPPLY REQUIREMENTS					
V_{LOGIC}		+5V ±10%	*	*	*
V_{CC}		+15V ±10%	*	*	*
V_{DD}		−15V ±10%	*	*	*
OPERATING CURRENT					
V_{LOGIC}		25mA (42mA max)	*	*	*
V_{CC}		10mA (16mA max)	*	*	*
V_{DD}		20mA (28mA max)	*	*	*
V_{REF}				0.5mA	***
POWER SUPPLY REJECTION					
V_{CC}		±0.005%/%	*	*	*
V_{DD}		±0.005%/%	*	*	*
POWER CONSUMPTION		575mW	*	*	*
OPERATING TEMPERATURE RANGE		−25°C to +85°C	−55°C to +125°C	*	**

*Same specifications as AD5211/12B.
**Same specifications as AD5211/12T.
***Same specifications as AD5214/15B.
[1] Other input ranges are available, consult factory.
[2] FSR is Full Scale Range and is equal to the peak to peak input signal.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Positive Supply	+18V
Negative Supply	−18V
Logic Supply	+7V
Analog Input	±25V
Digital Outputs	Logic Supply
Digital Inputs	+5.5V
Reference Supply	−15V

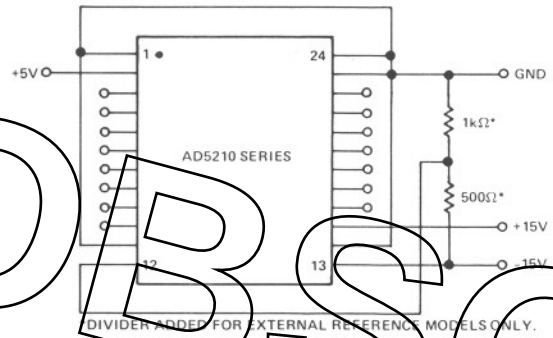


Figure 1. Burn In Circuit

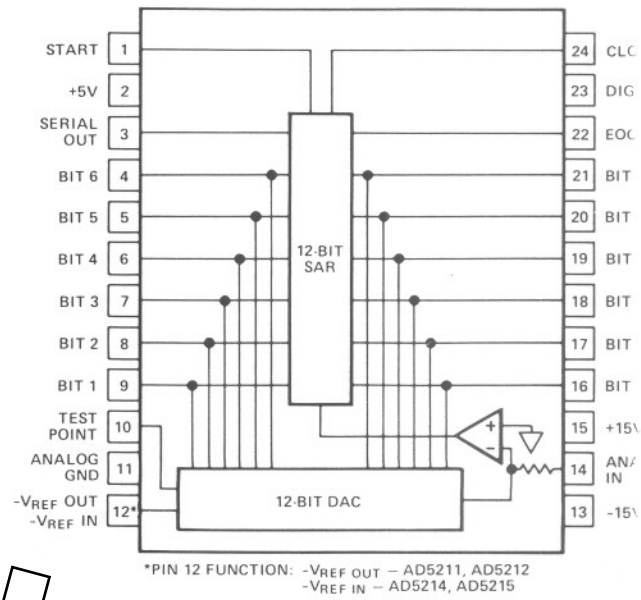
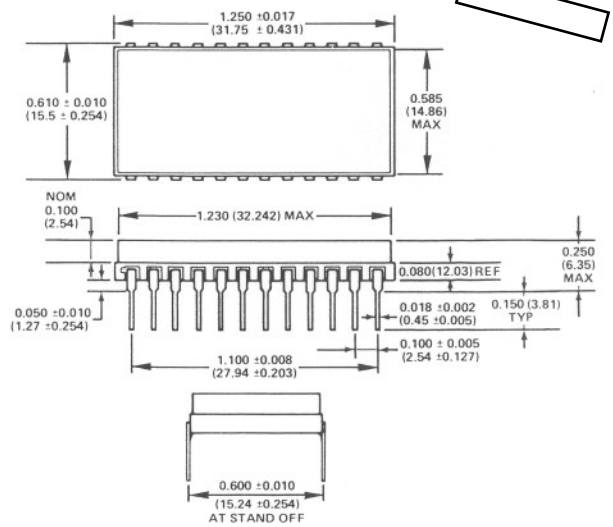


Figure 2. Pin Designations

OUTLINE DIMENSIONS
PACKAGING SPECIFICATIONS

Dimensions shown in inches and (mm).



AD5211/AD5214	AD5212/AD5215	MSB LSB
+5.0000V	+10.000V	0000000000
0.0000V	0.000V	1000000000
−4.9976V	− 9.995V	1111111111

Table I. Logic Coding (Complementary Offset Binary)

AD5210 SERIES ORDERING GUIDE

Model	Linearity	Absolute Accuracy	Temperature Range
AD521*BD	1/2LSB	2LSB	−25°C to +85°C
AD521*BD/883B	1/2LSB	2LSB	−25°C to +85°C
AD521*TD	1/2LSB	2LSB	−55°C to +125°C
AD521*TD/883B	1/2LSB	2LSB	−55°C to +125°C

*Insert number according to desired input voltage range.

THEORY OF OPERATION

On receipt of a CONVERT START command, the AD5210 converts the voltage as its analog input into an equivalent 12-bit binary number. This conversion is accomplished as follows: the 12-bit successive-approximation register (SAR) has its 12-bit outputs connected both to the device bit output pins and to the corresponding bit inputs of the feedback DAC. The analog input is successively compared to the feedback DAC output, one bit at a time (MSB first, LSB last). The decision to keep or reject each bit is then made at the completion of each bit comparison period, depending on the state of the comparator at that time.

TIMING

The timing diagram is shown in Figure 3. A conversion is initiated by holding the start convert low during a rising edge of the clock. The start convert transition must occur at a minimum of 25ns prior to the clock transition. The end of conversion (E.O.C.) signal will be set simultaneously with the initiation of conversion. The actual conversion will not start until the first rising edge of the clock after the start convert is again set high. At time t_0, B_1 is reset and B_2–B_{12} are set unconditionally. At t_1 the Bit 1 decision is made and Bit 2 is unconditionally reset. At t_2, the Bit 2 decision is made (keep) and Bit 3 is reset unconditionally. This sequence continues until the Bit 12 (LSB) decision (keep) is made at t_{12}. The STATUS flag is reset at time t_{12} indicating that the conversion is complete and that the parallel output data is valid.

Corresponding serial and parallel data bits become valid on the same positive-going clock edge. Serial data does not change and is guaranteed valid on negative-going clock edges, however; serial data can be transferred quite simply by clocking it into a receiving shift register on these edges (see Figure 3) An external clock of 1MHz will yield 13μs conversion time. Increasing the clock frequency will decrease the conversion time; the linearity error, however, will increase.

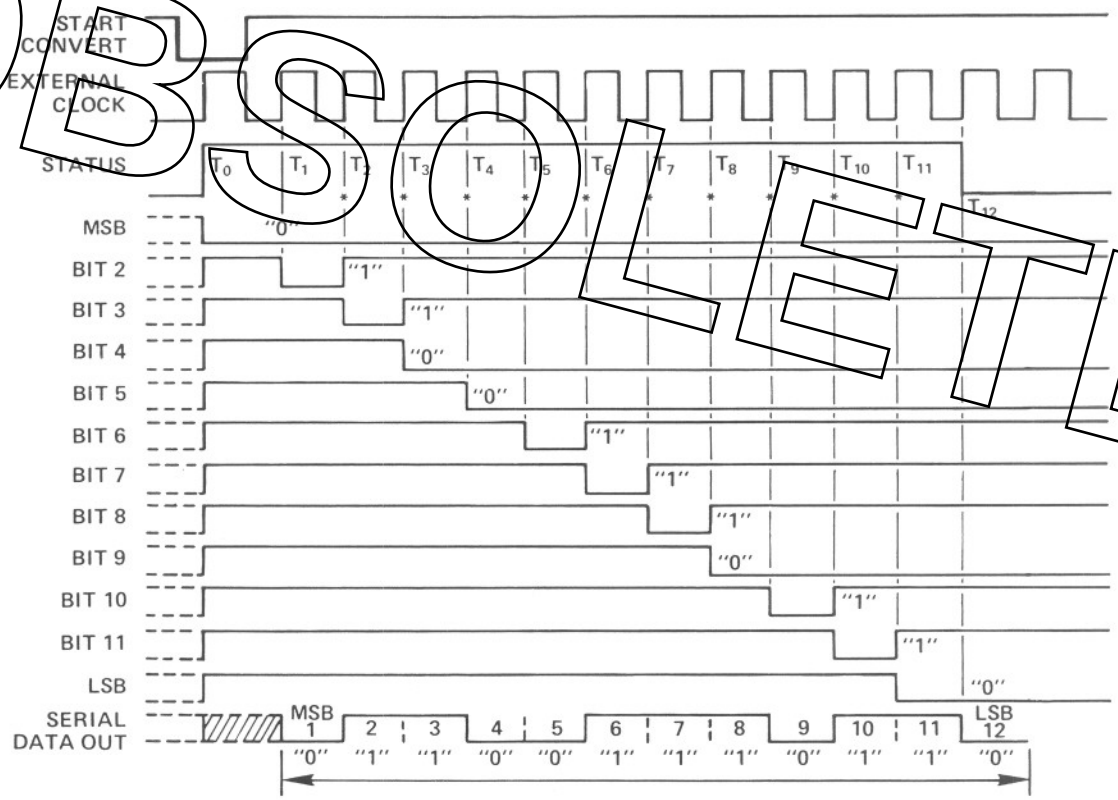


Figure 3. Timing Diagram

The analog continuum is partitioned into 2^{12} discrete ranges for 12-bit conversion. All analog values within a given quantum are represented by the same digital code, usually assigned to the nominal midrange value. There is an inherent quantization uncertainty of ±1/2LSB, associated with the resolution, in addition to the actual conversion errors.

The actual conversion errors that are associated with A/D converters are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, reference error and power supply rejection. The matching and tracking errors in the converter have been minimized by the use of a monolithic DAC that includes the scaling network. The initial gain and offset errors have been internally trimmed to provide an absolute accuracy of ±0.05%. Linearity error is defined as the deviation from a true straight line transfer characteristic from a zero analog input which calls for a zero digital output to a point which is defined as full scale. The linearity error is unadjustable and is the most meaningful indication of A/D converter accuracy. Differential nonlinearity is a measure of the deviation in the staircase step width between codes from the ideal least significant bit step size (Figure 4).

Monotonic behavior requires that the differential linearity error be less than 1LSB, however a monotonic converter can have missing codes; the AD5210 is specified as having no missing codes over the entire temperature range as specified on the data page.

There are three types of drift error over temperature: offset, gain and linearity. Offset drift causes a shift of the transfer characteristic left or right over the operating temperature range. Gain drift causes a rotation of the transfer characteristic about the zero or minus full scale point. The worst case accuracy drift is the summation of all three drift errors over temperature. Statistically, however, the drift error behaves as the root-sum-squared (RSS) and can be shown as:

$$RSS = \sqrt{\epsilon_G{}^2 + \epsilon_O{}^2 + \epsilon_L{}^2}$$

ϵ_G = Gain Drift Error (ppm/°C)
ϵ_O = Offset Drift Error (ppm of FSR/°C)
ϵ_L = Linearity Error (ppm of FSR/°C)

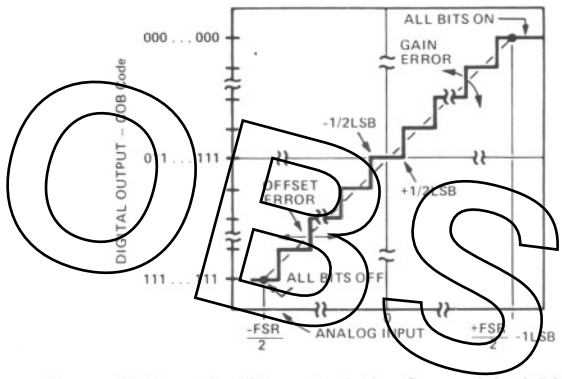


Figure 4. Transfer Characteristics for an Ideal Bipolar A/D

GROUNDING

Many data-acquisition components have two or more ground pins which are not connected together within the device. These "grounds" are usually referred to as the Digital Ground and Analog Ground (Analog Power Return). These grounds must be tied together at one point, usually at the system power-supply ground. Ideally, a single solid ground would be desirable. However, since current flows through the ground wires and etch stripes of the circuit cards, and since these paths have resistance and inductance, hundreds of millivolts can be generated between the system ground point and the ground pin of the AD5210. Separate ground returns should be provided to minimize the current flow in the path from sensitive points to the system ground point. In this way supply currents and logic-gate return currents are not summed into the same return path as analog signals where they would cause measurement errors.

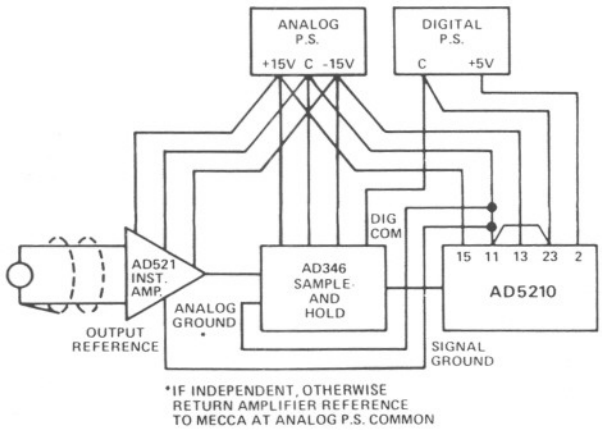


Figure 5. Basic Grounding Practice

Each of the AD5210's supply terminals should be capacitively decoupled as close to the AD5210 as possible. A large value capacitor such as 1μF in parallel with 0.01μF capacitor is usually sufficient. Analog supplies are bypassed to the Analog Ground pin and the logic supply is bypassed to the Digital Ground pin.

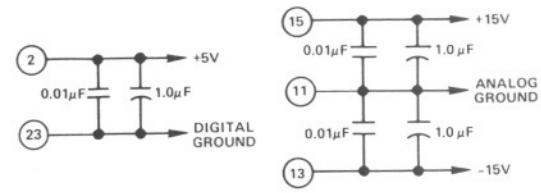


Figure 6. Power Supply Decoupling

SAMPLED DATA SYSTEMS

The conversion speed of the AD5210 allows accurate digitization of high frequency signals and high throughput rates in multichannel data acquisition systems. To make the AD5210 capable of full benefit from this high speed, a fast sample-hold amplifier such as the AD346 or ADSHC-85 is required. Figures 7 and 8 show the use of an AD346 and ADSHC-85 as sample and holds in combination with the AD5210.

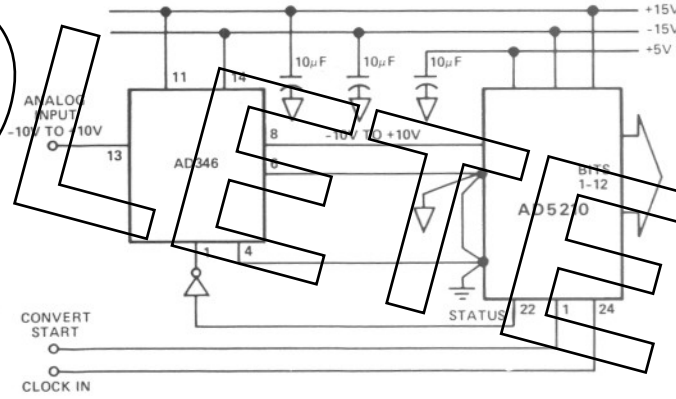


Figure 7. 66.6Hz—12-Bit, A/D Conversion System

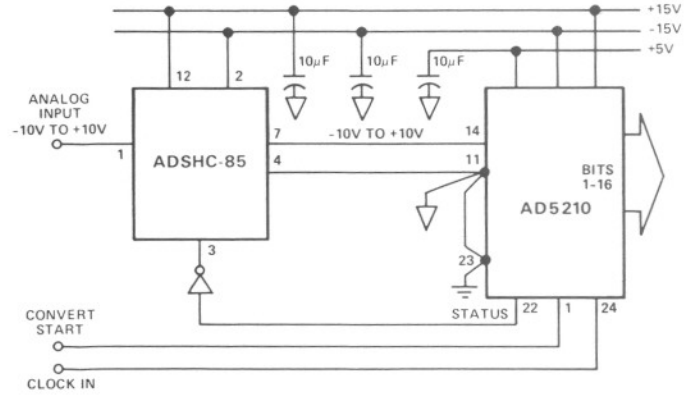


Figure 8. 57.1kHz—12-Bit, A/D Conversion System

In sampled data systems there are two limiting factors in digitizing high frequency signals. The maximum value of input signal frequency that can be acquired and digitized using a sample and hold amplifier and A/D converter combination is influenced by the bandwidth of the SHA, but it is also dictated by:

A. The aperture uncertainty (jitter) of the sample and hold amplifier.

B. The desired accuracy and corresponding resolution of the converter.

The resolution of an AD5210 is 1 part in 4096 to a tolerance of 0.012% of the full scale range, the maximum value of input signal frequency which can be digitized is determined by:

$$F_{MAX}/ = \frac{2^{-N}}{(2\pi)(\text{Aperture Uncertainty})}$$

$$F_{MAX}/\text{AD346} = \frac{1}{(2\pi)\ (4096)\ (4 \times 10^{-10})} = 97.1\text{kHz}$$

$$F_{MAX}/\text{ADSHC-85} = \frac{1}{(2\pi)\ (4096)\ (5 \times 10^{-10})} = 77.7\text{kHz}$$

The maximum throughput rate for each of these combinations is again different. The maximum throughput rate is the sum of the sample and hold acquisition time and A/D conversion time as shown in Figure 9.

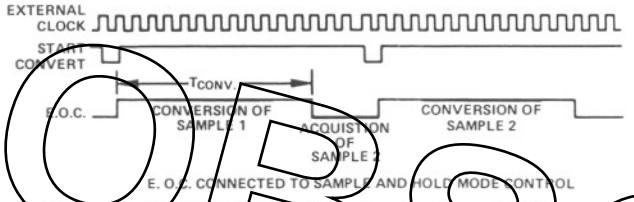


Figure 9. START/E.O.C. Timing for Sampled Data System

When using an AD346 with an AD5210 the throughput rate is, 2.0μs acquisition time plus 13μs conversion time, 66.6kHz. The ADSHC-85 used in combination with an AD5210 is, 4.5μs acquisition time plus 13μs conversion time, 57.1kHz. To meet the requirements of the nyquist sampling criteria, the AD346 and AD5210 combination can be used for input frequencies from dc through 33.3kHz; the ADSHC-85 and AD5210 combination for inputs from dc through 28.5kHz. Input frequencies higher than these (up to the maximum frequency) would result in "under-sampling" of the input signal. Signals up to the maximum frequency could be processed if their bandwidth is less than one-half the sample frequency.

A fast (32kHz) 12-bit DAS can be configured using the AD362 and the AD5210. The AD362 contains two 8-channel multiplexers, a differential amplifier, a sample-and-hold with high-speed output amplifier, a channel address latch and control logic. The multiplexers may be connected to the differential amplifier in either an 8-channel differential or 16-channel single-ended configuration. A feature of the AD362 is an internal user-controllable analog switch that connects the multiplexers in either a single-ended or differential mode. This allows a single device to perform in either mode without hard-wire programming and permits a mixture of single-ended and differential sources to be interfaced by dynamically switching the input mode control.

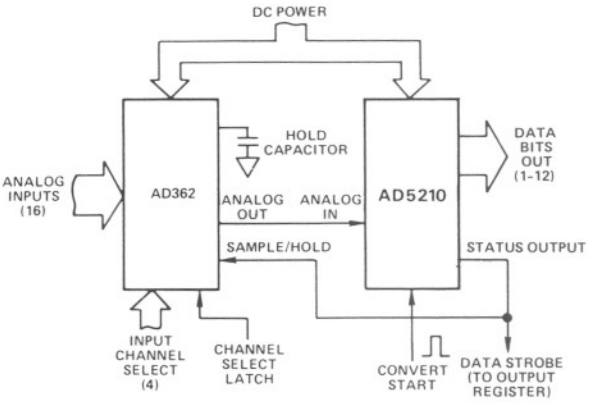


Figure 10. High Speed 12-Bit DAS

CONVERT START USING A POSITIVE EDGE

In some systems it may be inconvenient to generate a negative going start convert pulse of the proper width. The circuit of Figure 11 can be used to start a conversion on the AD5210 series of A/Ds with a positive going edge. To perform a conversion both the convert start signal and the E.O.C. must be low. The output of the inverter and nand gate will then be in the high state. The converter will reset on the next rising clock edge. Resetting brings the E.O.C. to a high state; the inverter goes low; the convert start is still high so the output of the nand gate goes high allowing the conversion to continue immediately. The convert start line has only to be brought back down before the conversion is complete.

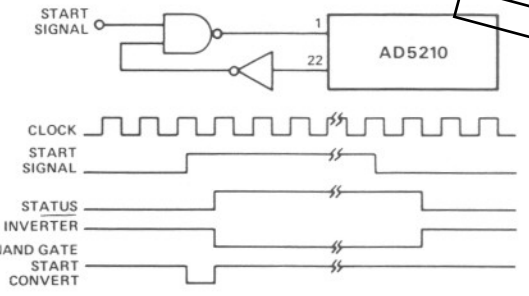


Figure 11. Convert Start Using a Positive Edge

MIL-STD-883

The rigors of the military/aerospace environment, temperature extremes, humidity, mechanical stress, etc., demand the utmost in electronic circuits. The AD5210 Series, with the inherent reliability of integrated circuit construction, was designed with these applications in mind. The hermetically-sealed, low profile DIP package takes up a fraction of the space required by equivalent modular designs and protects the chip from hazardous environments. To further insure reliability, the AD5210 Series is offered with 100% screening to MIL-STD-883B, method 5008.

Table II details the test procedures of MIL-STD-883. Analog Devices subjects each part ordered with 883B screening to these tests on a 100% basis.

PROCESS	CONDITIONS
1) 100% pre-cap Visual Inspection	2017.1, Internal Spec. A8075
2) Stabilization Bake	1008, 24 hours @ +150°C, Condition C
3) Temperature Cycle	1010, Test Condition C, 10 cycles, -65°C to +150°C
4) Constant Acceleration	2001, Y1 Plane, 5000G, Condition A
5) Visual Inspection	Visible Damage
6) Operating Burn-In	1015, Test Condition B 160 hours @ +125°C
7) Seal Test: Fine Leak	1014, Test Condition A, 5 x 10^{-7} std cc/sec
Gross Leak	1014, Condition C
8) Final Electrical Test	Per Data Sheet
9) External Visual Inspection	2009

Table II.