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APPLICATION NOTE

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Modem-Circuit Techniques Simplify Instrumentation Designs

by Walt Jung and Moshe Gerstenhaber

A commutating modem circuit, whether an IC or pc-board version, can serve as a building block for many measurement-system functions, reducing noise and ensuring the integrity of transmitted data.

Although used extensively in communications, amplitude modulation/demodulation can also serve industrial-control instrumentation systems. In such applications, a commutating modulation/demodulation circuit is an extremely versatile building block that can perform several functions—such as amplification and clock generation—in addition to helping assure the integrity of measurement-data transmission. This article describes the operation and application of that type of modem in a variety of instrumentation situations.

Modulating and demodulating the output of an instrumentation system's sensors, a process often referred to as balanced mod/demod, provides a host of advantages:

- Ease of filtering
- Inherent noise discrimination
- Good linearity over a wide dynamic range
- Transmission of phase as well as amplitude information
- Relaxation of intermediate-stage amplification requirements.

Fig 1's representation of a typical control-instrumentation system helps demonstrate how to use a modem to realize these advantages. Transducers typically used in such control systems—such as linear and rotary variable differential transformers (LVDTs or RVDTs), ac bridges and photochoppers—measure occurrences that are usually static or slowly varying. This measurement

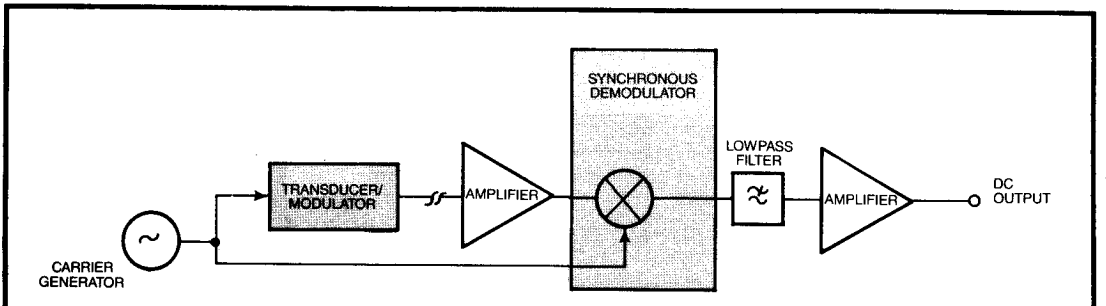

Fig 1—A typical instrumentation system *can include a synchronous demodulator that removes the carrier signal from a transducer's modulated output. Using balanced modulation/demodulation removes system offset, drift and noise too.*

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Balanced modem circuit removes low-frequency noise

data can be imposed on a carrier signal by modulation; modulation capability may be inherent to the transducer, as is the case with an LVDT, or require use of an external modulator, as with some types of photochoppers.

The modulated signal is then typically transmitted to a central controller that extracts raw measurement data from the signal. If the carrier's frequency is well above the measured parameter's rate of change (typically, a carrier frequency of about 1 kHz gives sufficient carrier/data separation), simple post-demodulation filtering rejects all noise and dc errors but leaves the original signal intact.

The balanced modulation/demodulation scheme inherently rejects frequency disturbances—such as 1/f components, drift and power-line noise—that are either asynchronous to or in quadrature with the demodulating carrier. Thus, the combination of balanced modulation/demodulation and filtering eliminates many of the chief causes of measurement errors.

Consider, though, that the additional modulation/demodulation circuitry could introduce new sources of error. One type of modulation/demodulation circuit, the commutating modem, minimizes the sensitivity of the measurement signal to variations in the amplitude and waveform of the demodulating carrier signal, thus minimizing the effects of demodulation on measurement results.

To understand how a commutating modem minimizes noise sensitivity, consider two ac signals: a modem input that you wish to demodulate and a carrier signal that you can use to do the demodulating. When the carrier is positive, the commutating modem multiplies the input by +K (a scaling constant that you choose), and when the carrier is negative, by −K. Because the carrier's transitions between positive and negative states control the modulation process, the carrier's waveform and amplitude do not affect the output.

Fig 2 graphically shows the commutating modem's multiplication process. If the input and the carrier signal are in phase, the commutating modem's output is a positive, full-wave-rectified version of the input. When the input and the carrier are 180° out of phase, the output is a negative, full-wave-rectified version of the input. In either case, the average value of the output is proportional to the amplitude of input signal. But for an input signal in quadrature with the carrier, the output is a zero average value. In other words, the averaged output is proportional to the input amplitude as well as the phase difference between the input and the carrier.

Because modulation and demodulation are reciprocal processes, the **Fig 2** waveforms can also apply to a modulation scheme in which the input and output are reversed. That is, when the signal labeled output is mixed with the carrier at the modulator, that device creates the waveforms marked input.

This reciprocity is a powerful advantage of balanced modulation/demodulation because it allows you to use a common circuit for both modulation and demodulation. And most hardware implementations of the balanced modulation/demodulation circuit function are designed to be used either way.

Fig 3 shows a commutating balanced modulation/demodulation circuit that you can build with standard components. This circuit, commonly used in data acquisition and signal processing, is called an absolute-value circuit, a precision rectifier or a sign-programmable amplifier, depending on its specific use.

The **Fig 3** circuit is optimized for the commutating

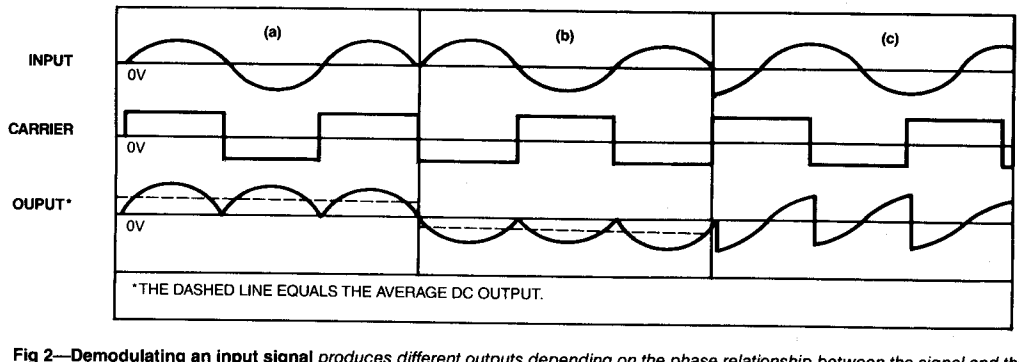


Fig 2—Demodulating an input signal *produces different outputs depending on the phase relationship between the signal and the modulating carrier. The average dc output is positive* ***(a)****, negative* ***(b)*** *or zero* ***(c)*** *when the input and carrier are in phase, 180° out of phase or 90 or 270° out of phase, respectively. For simplicity, the input is shown as a sine wave of the same frequency as the carrier, but a carrier whose frequency is an odd multiple of the signal frequency produces similar average-dc results.*

A commutating modem IC

The AD630 includes all the circuit blocks needed to implement balanced modulation and demodulation with high precision in a single IC. Shown functionally in the **figure**, it contains two uncommitted op-amp input stages, A and B. Depending on the state of the input to the IC's integral comparator, either stage A or B is connected to the chip's integrating output stage. When pin 10 is high relative to pin 9, input stage A is active; when the reverse is true, input stage B is active.

The chip's comparator is an internally latched stage with a specified switching window of ±1.5 mV (max), a window that includes not only comparator offset but a hysteresis of about 0.2 mV as well. The hysteresis is built in to make switching clean and unambiguous, even with slowly varying or noisy signals.

When switched, the AD630 can slew as fast as 45V/μsec between the output limits. In response to a 20V step, the output typically settles to within 0.01% of the final value in 3 μsec.

Inputs to stages A and B can be connected into conventional op-amp feedback loops, either with external components or internal resistors. On-chip resistors are ratio-trimmed for precise gains of ±1, ±2, +3 and +4 and are easily configured by appropriate pin strapping. Other gains are possible with external resistors.

The advantage of the internal resistors lies not only in their convenience, but also in their precision. Gain error is 0.05% (max) for B and K grade devices and 0.5% for other grades. These resistors also feature a 2-ppm/°C tracking specification. Resistors for bias-current compensation are also available at the A+ and B+ inputs for optional use in attaining the highest dc accuracy.

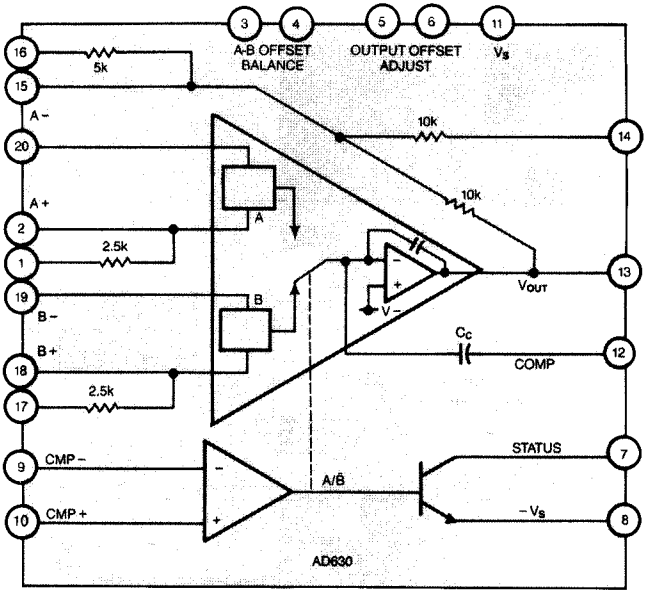
With its on-chip resistors, the AD630 can achieve submillivolt dc offsets and 0.1% or better dc accuracy without user trimming or gain-setting resistors. The dynamic specifications are such that the device is generally useful for modem uses to 100 kHz, and it is useful with high precision through the range of common instrumentation carrier frequencies—well above the limits of 0.5V/μsec-slew-rate devices.

All AD630 family devices come in plastic or ceramic 20-pin DIPs and operate from standard ±15V supplies, with conventional ±10V input/output ranges.

Many details of the AD630's design prove advantageous in various applications. For example, you can use the open collector output from the comparator (pin 7) as a logic status indicator. This status output can be used with an external pullup resistor to a positive voltage and can sink load current to $-V_S$ in the 0 state.

Another useful feature is that you can optimize device frequency compensation by strapping pin 12 to 13. Doing so reduces device bandwidth and phase at unity gain to its lowest value and reduces slew rate to 35V/μsec. With this pin open, the device speed is at its 45V/μsec maximum.

Two optional dc-offset trim connections use a pair of 10-kΩ trimmers: one between pins 5 and 6 and the other between pins 3 and 4. The wipers of both trimmers are tied to $-V_S$ (pin 8). The offset trimmer between pins 3 and 4 is first adjusted for a minimum-level square-wave output with a switching signal applied to the comparator and 0V dc input. The offset trimmer at pins 5 and 6 is then used to adjust the output offset to zero, with the comparator state fixed. These offset trims need only be used in the most demanding applications because of the low level of pretrimmed offset.



Uncommitted op-amp inputs A and B *allow the AD630 to operate as a commutating modem. An integral comparator selects between the two stages depending on the relative input levels at pins 9 and 10.*

function and minimizes errors from both the dc and ac sources. The carrier input controls output polarity with switch SW_1 set as shown, and the circuit functions as a modulation/demodulation circuit that exhibits the **Fig 2** waveforms. It might also be correctly referred to as a sign-bit amplifier, generally used in A/D or D/A conversion. In conversion applications, the carrier input would be called the sign-bit input.

When comparator stage A_3 is driven by the input signal rather than the carrier, the circuit is an absolute-value (or precision rectifier) circuit. Regardless of which signal does the driving, the output polarity can be changed by reversing the input of comparator A_3.

Although furnishing good performance, this circuit needs three separate active devices, a matched pair of precision resistors, board space, and design and debug time to build it. Furthermore, you have to optimize the amplifier for low noise, low offset and low drift and fast slew rate—not a trivial design problem. Integrating these components with an eye toward such performance objectives would be a logical improvement (**Ref 1**), and a chip that does just that is discussed in the accompanying **box** ("A commutating-modem IC"). This chip is used for simplicity in the examples that follow, but the discrete circuit of **Fig 3** could also be used.

Fig 4a shows a general-purpose modulation/demodulation circuit using the AD630. It is basically a switched-gain circuit with an absolute gain of 2; the V_{REF} input to the comparator determines the output polarity. Like the **Fig 3** circuit, this circuit can be used as a modulator or demodulator, a sign-bit amplifier, an absolute-value (precision rectifier) circuit or a phase detector applied to the device.

To understand the circuit operation, think of the AD630 as having three separate internal functions: a comparator stage and an output stage and two switched-input stages, only one of which is on at a time, depending on comparator state. The active input stage in conjunction with the output stage forms a single composite op amp, so you can regard the AD630 as an op amp that has two configurations depending on the comparator input.

For example, with input stage **A** on, the overall circuit is equivalent to that of **Fig 4b**. The circuit has a noninverting gain of 2 when V_{REF} is greater than V_{OV}, or in general, when the AD630's pin 10 has a higher input than its pin 9. Conversely, when input stage **B** is on, the overall circuit is equivalent to the circuit of **Fig 4c**. This circuit has an inverting gain of 2 when V_{REF} is less than V_{OV}, or in general, when pin 10 is lower than pin 9.

In this circuit, the feedback loop that sets the gain at 2 is defined using the chip's internal resistors that are

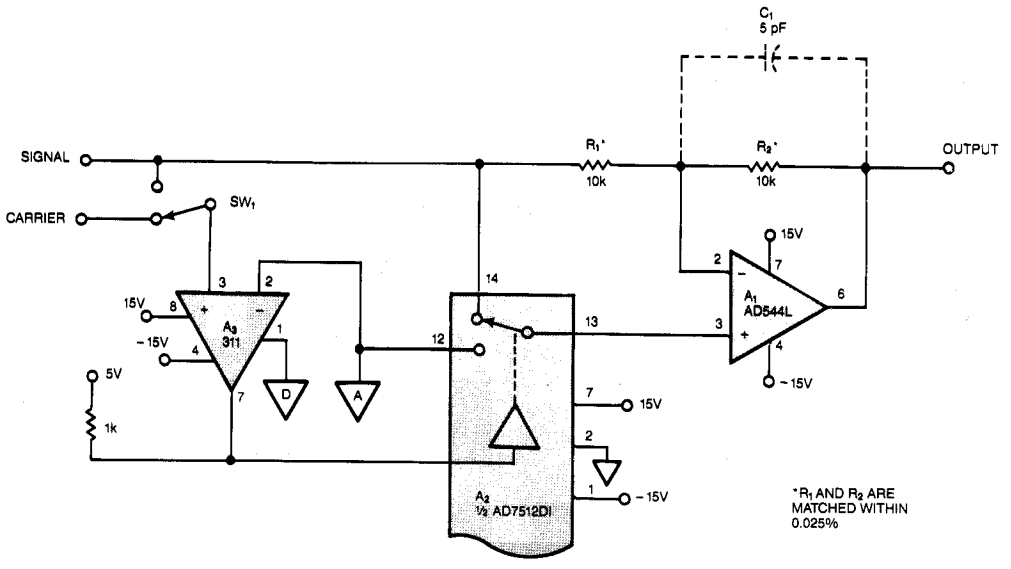


Fig 3—Known by a variety of names, *the basic commutating modulator/demodulator circuit is called a sign-bit amplifier when comparator A_3's carrier input, selected with switch SW_1 in the position shown, is a sign-bit signal. When the signal serves as A_3's input, the circuit is called an absolute-value or precision-rectifier circuit.*

connected to the circuit's pins 13, 14, 15 and 16. Including a variety of internal precision resistors with pin-accessible taps lets you use jumpers to simply select the gain state desired. If you should decide to use your own external feedback components, the sign and the gain magnitude might be different. Regardless of the feedback-loop approach you choose, the active state of inputs A and B (**Fig 4b** and **Fig 4c**) remain generally true.

In many applications, the A and B inputs are often interconnected, as A– and B– are in **Fig 4a**. This presents no output problem because the deselected input is switched off and presents no extra loading to the summing point.

However, the circuit presents different loads at its signal input depending on the input to the comparator. Note that the inverting configuration B in **Fig 4c** presents a load equal to R_{IN}, or 5 kΩ, when this input is selected, and the noninverting stage (**Fig 4b**) presents an input impedance intrinsically higher. Thus, the external input source faces a load that varies dynamically. To maintain the highest precision, you may have to add an input buffer to compensate for this dynamic loading.

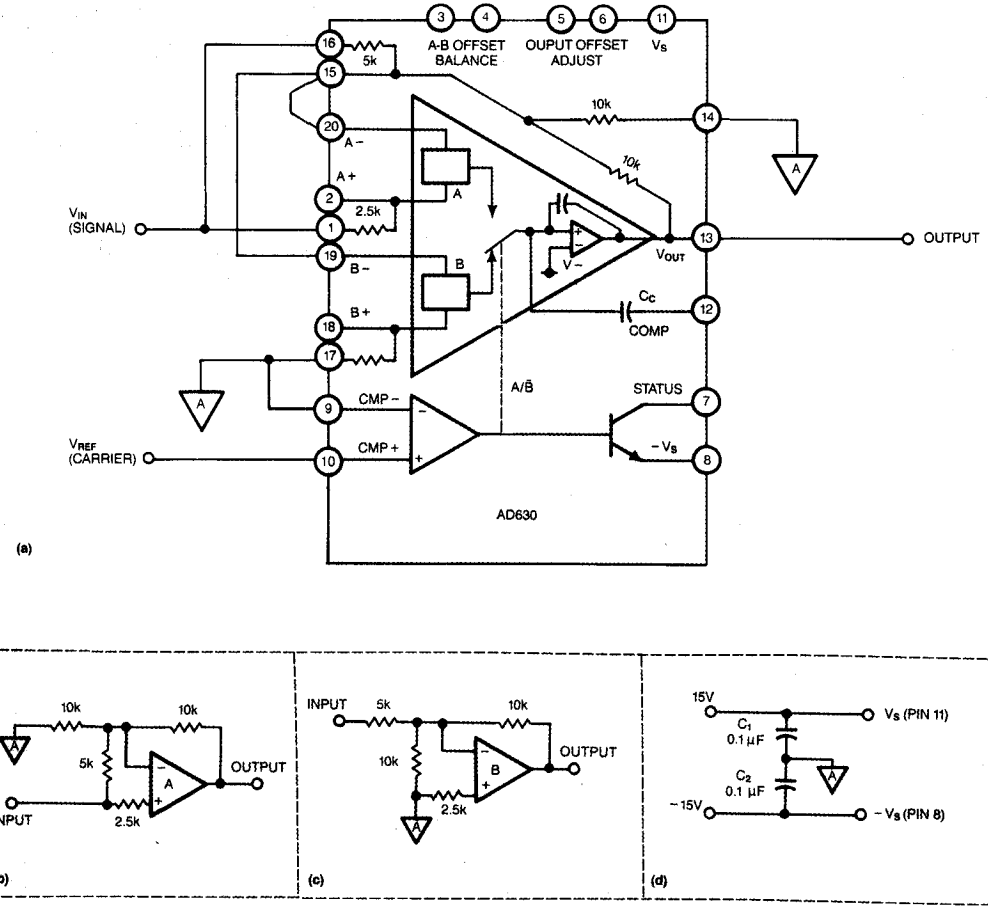


Fig 4—A building block IC *like the AD630 can be turned into a balanced modulator/demodulator* ***(a)*** *similar to that in* ***Fig 3.*** *Using the chip's precision resistors to set the gain (to a value of 2 with the configuration shown here) eliminates the need for trimming in most applications. The equivalent circuits seen when looking into the AD630's input when channel A or B is active are shown in* ***(b)*** *and* ***(c),*** *respectively, and the supply-conditioning circuitry for the chip appears in* ***(d).***

LVDTs' inherent modulation requires a precise carrier

For absolute-value applications, the AD630 has distinct advantages over the traditional op-amp approach. Even when implemented with high-performance amplifiers, traditional absolute-value circuits have classic problems: With high-frequency inputs of low amplitude, for example, the op amp must slew for high percentages of the time to accommodate the diode thresholds. As a result, the output waveform can be severely distorted. The balanced-modulator approach alleviates this problem simply by changing the sign of the forward signal path in synchronism with the zero crossings, with no diode thresholds to overcome. Using the **Fig 4** configuration as a gain-of-2 absolute-value circuit produces **Fig 5**'s results.

Such balanced modulation/demodulation techniques are highly useful with a variety of common transducers. What's more, a number of transducer types lend themselves to this approach because they perform the modulation of an ac carrier as an integral part of their transducing function. Examples of such transducers are those that fall in the LVDT and ac-bridge categories. Other types, such as some photochoppers, don't furnish modulation and require further interfacing to modulate their outputs. The **Fig 3** and **Fig 4** circuits can be built

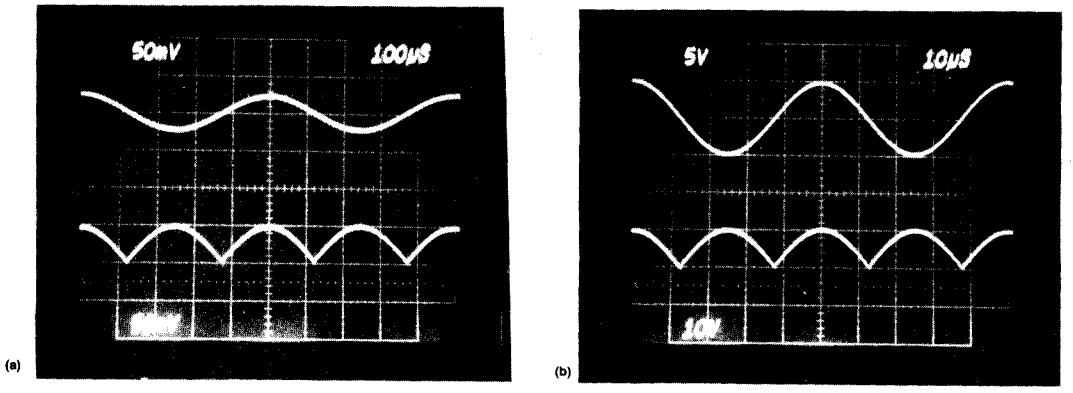


Fig 5—In an absolute-value circuit *with a gain of 2, the AD630 produces positive rectified outputs. In* ***(a)****, the 2-kHz, 25-mV pk signal at the top produces the 50-mV pk rectified output below it. In* ***(b)****, a high-amplitude (5V pk), high-frequency (20-kHz) signal at top produces the 10V pk output below it. In either case, the sign of the input is available from the device's status output.*

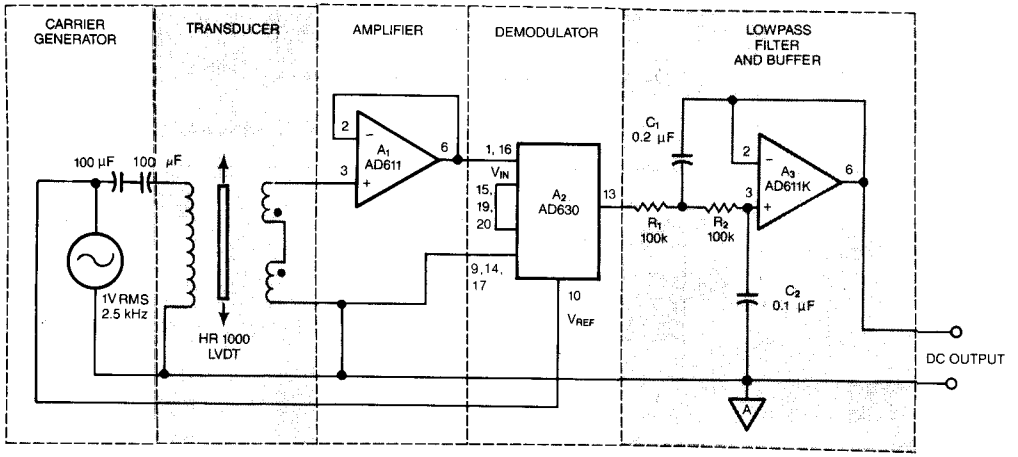


Fig 6—A linear variable differential transformer *whose measurement signal rides on a 1V rms, 2.5-kHz carrier can work with a commutating modulation/demodulation circuit such as the one shown in* ***Fig 4****. The lowpass filter at right, with a 10-Hz corner frequency, removes any high-frequency noise.*

into or added to the sensor/transducer to provide this modulation.

Among the transducers that have integral modulating capability, the LVDT measures linear displacement, and a related type, the RVDT, measures rotary displacement (**Ref 3**). Although the mechanical construction of these two types of transducers differs, they share many electrical similarities. Therefore, similar electrical considerations apply to the application of either type of device.

A transducer of either type is really a specialized transformer. The transformer is connected with two secondary windings in series opposition and exhibits a minimum electrical output at the LVDT's mechanical null point. The core motion, controlled by the object whose displacement is to be measured, varies the mutual inductance between the primary and the two secondaries. This variation produces a variable-phase and -amplitude ac output that is linearly proportional to the core displacement. A balanced demodulator can transform this variable ac output into a bipolar dc output that, when referred to the LVDT reference, or null, position, indicates the displacement.

The LVDT's physical advantages lie in the virtues of a low core mass, an essentially frictionless, no-hysteresis action, infinite resolution, and long mechanical life. Electrical advantages are the low sensitivity to external fields and the high common-mode isolation that a transformer inherently affords. The main disadvantage is the relatively high cost, which tends to be proportional to core length and accuracy. LVDTs come in a wide variety of mechanical and electrical configurations, with different nonlinearity and sensitivity specifications (**Ref 3**).

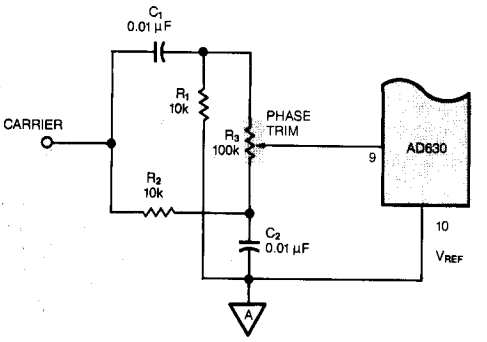


Fig 7—To trim a carrier signal *so that it's in phase with the input signal, you can use this lead-lag network. With the transducer at its maximum value, adjust resistor R_3 to maximize the circuit's average dc output.*

Fig 6 shows a representative application using a general-purpose LVDT, a Schaevitz Engineering (Pennsauken, NJ) Model HR 1000, whose core can travel distances of ±1 in. and whose output i

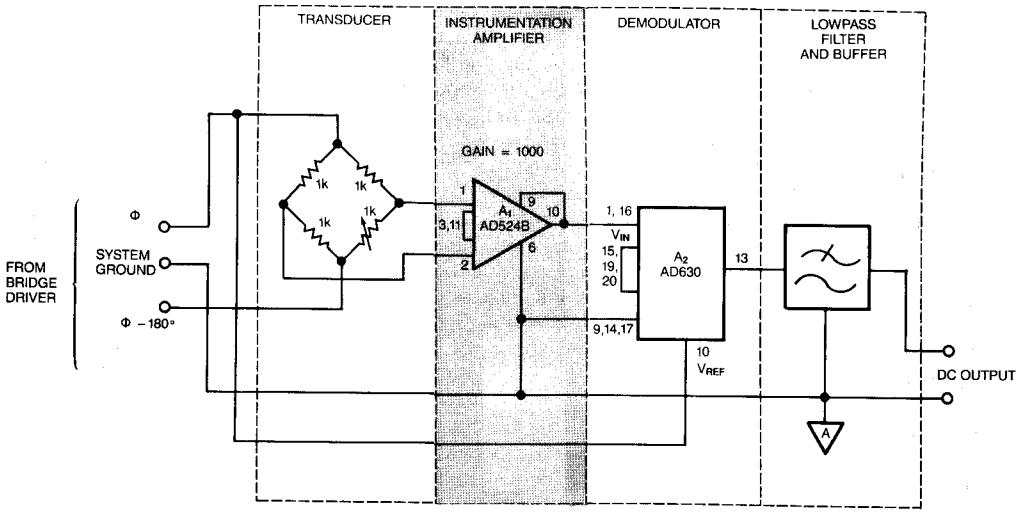


Fig 8—To measure changes in a bridge's variable arm, *this circuit uses a demodulator and filter similar to those in* ***Fig 6.*** *The bridge circuit's low-voltage output, however, requires use of a high-gain instrumentation amplifier, and the circuit requires a special bridge driver such as the one shown in* ***Fig 9.***

Carrier phase trimming may be needed for accuracy

within 0.25% FS. This circuit demonstrates some of the general principles of LVDT interfacing and can be used as a guide with other variable differential transformers. With the **Fig 6** circuit, system errors due to the electronics are negligible, and transducer errors predominate.

The HR 1000 can handle a 3V rms maximum excitation signal. An LVDT's sensitivity is typically specified in terms of millivolts of output per volt of excitation per mil (0.001 in.) of displacement (mV/V/mil). For this device, the rated sensitivity is 0.39 mV/V/mil, so with an excitation signal of 1.0V rms, the HR1000 produces a 390-mV rms FS (1-in. displacement) output. In **Fig 6**, a demodulator with a gain of 2 processes the LVDT output, doubling the sensitivity and producing a 780-mV rms FS output.

A Sallen-and-Key two-pole active filter with unity gain filters the demodulator output and buffers it to a low impedance. This circuit, using A_3 and the associated passive components, employs a maximally flat Butterworth alignment for minimum passband-amplitude errors. This filter's corner frequency is approximately 10 Hz, and the filter yields more than 80 dB of ripple attenuation for carriers as low as 1 kHz. Although this application is fairly straightforward, it serves to point out certain general rules you should know to use LVDTs effectively.

For maximum sensitivity and a minimum of susceptibility to carrier-frequency changes, the LVDT should see a high-impedance load. In **Fig 6**, a follower-connected FET-input op amp that acts as a buffer provides this load. The op amp also provides the balanced demodulator with a low source impedance that makes the circuit insensitive to dynamic load changes.

A stable oscillator

The performance of the carrier oscillator is critical to high-accuracy balanced modem signal processing. Although absolute accuracy and long-term frequency stability are not highly critical, amplitude stability and waveform purity are.

Amplitude stability is critical because the voltage level of the carrier signal applied to an LVDT or an ac bridge directly affects the overall system sensitivity. Therefore, the carrier amplitude must be stable against loading, time, supply-voltage and temperature changes. Waveform purity is also important—high harmonic content can introduce errors, particularly with regard to the LVDT null.

The circuit shown in the **figure** satisfies these amplitude and waveform requirements. It is a spot-frequency sine-wave oscillator whose frequency can be set to a value in the 1- to 5-kHz range. It produces a 1V rms output with harmonic distortion on the order of 0.05% or less.

The oscillator uses a Wien bridge configuration built around FET-input op amp A_{1A}. The Wien network consists of frequency-determining components R_1-C_1 and R_2-C_2. An oscillator frequency of 1 or 2.5 kHz can be selected by the choice of the timing components indicated in the **figure**.

Although the Wien bridge can provide a pure sine wave, automatic gain control (AGC) is required to regulate the output amplitude. AGC is provided by first having A_3, an AD536J rms/dc converter, detect and convert A_{1A}'s output. Op amp A_{1B} then compares A_3's rectified output to a dc reference voltage. In the process, A_{1B} integrates the input and supplies the resultant output as the gate voltage for Q_1.

A_4, an AD584, supplies the dc reference voltage to which A_3's output is compared. It applies a stable +2.5V dc to the amplitude-controlling potentiometer R_8. With a 2V control-voltage potential applied to R_6 from the arm of R_8, the loop develops a 1V rms output from the AD644 oscillator stage A_{1A}, which is available at TP_1.

So as not to disturb the automatic control loop with external loading effects, A_2 buffers the output. This design also lets you adjust the gain of the buffer stage to accommodate different output levels while the oscillator stage itself operates at a fixed low level for best stability and lowest distortion. This oscillator can operate with supply voltages ranging from ±5V to ±15V, but best performance occurs at ±15V.

Although the inherent stability of the AGC system nulls the differences in individual FET devices, there still may be applications where the carrier amplitude error might need to be monitored. With this circuit, such an output (TP_2) is provided from the AD536J's internal buffer at pin 6.

The dc voltage at TP_2 is proportional to the ac carrier amplitude to within 0.5%. It can be used simply for monitoring the carrier or as a reference signal for ratiometric-balanced detection. The latter use is much more effective than the former for system error minimization because an appropriately scaled/filtered version of this signal can be used as an A/D converter reference voltage, and thus the A/D converter provides ratiometric conversion.

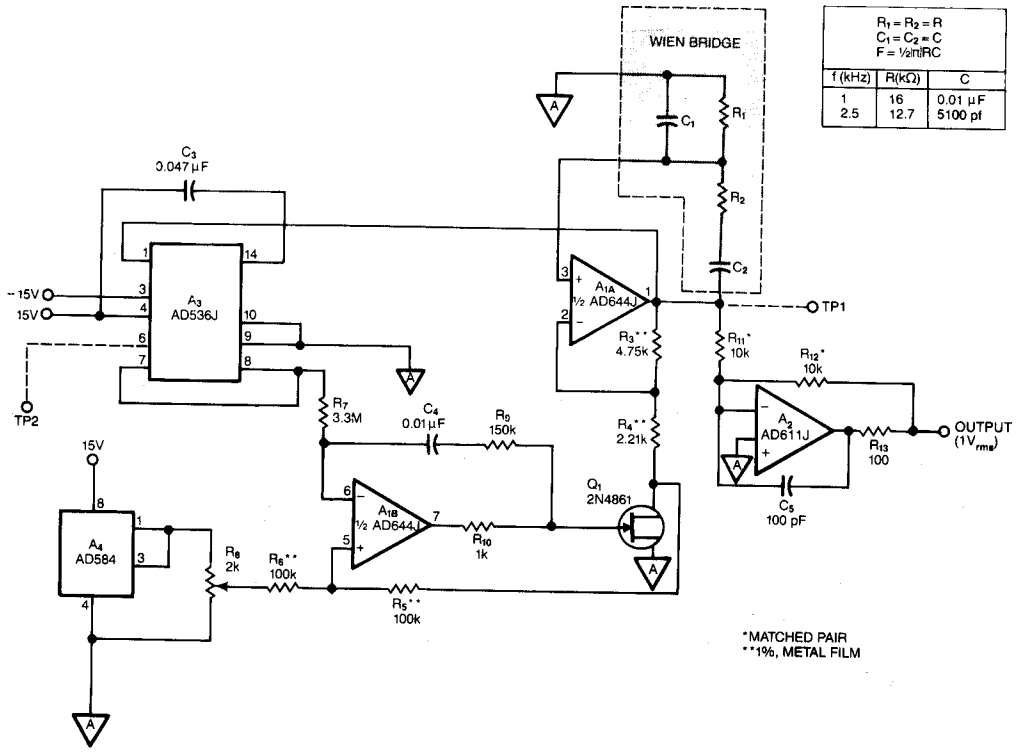
This op amp can also serve to introduce gain scaling. If you opt for gain scaling here, low temperature-coefficient resistors with ratios that track closely yield the best gain stability. Although amplifier drift and offset at this point is not critical, gain stability is because it directly influences overall sensitivity.

Depending on the specific transducer used, a phase-trim network might be needed in the reference channel. The **Fig 7** combination lead-lag network provides a carrier reference phase trim for minimum dc output at null, and if used it should be connected between the carrier generator and the AD630 as indicated. The circuit should employ stable components, which suggest a high-resolution multiturn trimmer for R_3, and, for the other components, fixed-value capacitors and resistors with low temperature coefficients. Metal-film resistors and polystyrene capacitors offer this performance.

As previously noted, the carrier excitation voltage applied to the LVDT directly influences the overall system sensitivity. Therefore, the carrier generator should provide a stable, low-distortion sine wave (see **box,** "A stable oscillator") and should be ac coupled with the LVDT, as **Fig 6** shows, to eliminate any possible primary dc in the transducer; any dc voltage here could result in nonlinearity or catastrophic faults.

Use balanced modems with ac bridges

The oscillator requirements also apply to another widely used class of transducers: bridge-type sources. For bridge transducers that can accommodate ac excitation as well as dc, balanced demodulation of the amplified ac output suppresses a host of problems, including the drift and noise of the (usually) necessary preamplification.



Based on a Wien bridge *that supplies a sine wave with little distortion, this oscillator circuit also employs automatic gain control to stabilize amplitude.*

AC bridge transducers work best with balanced inputs

Fig 8 illustrates an ac signal-conditioning system using a 1-kΩ/leg bridge, driven by a balanced 20V p-p, 1-kHz signal. An AD524B instrumentation amplifier (**Ref 4**) serves as a 1000× gain block (A_1), which is followed by a balanced demodulator with a gain of ±2 and by the 10-Hz lowpass filter used with the LVDT. Phase trim, if needed, is performed using **Fig 7**'s network.

Driving the bridge with balanced signals maximizes bridge sensitivity—enabling the system to resolve bridge unbalances of 1 ppm or less—and minimizes unbalance problems caused by stray capacitance. It also minimizes the common-mode voltage presented to the bridge preamp, thus enhancing input dynamic range. Remember that those preamp common-mode errors in quadrature with the carrier are nulled in the balanced demodulation process.

Fig 9 shows a push-pull circuit that provides balanced drive signals for the bridge. This driver develops two 10V p-p waveforms 180° out of phase when fed a 1V rms input from an oscillator. Because ac bridge excitation, like that of LDVTs, should be stable for best overall sensitivity, the **Fig 6** circuit's oscillator, described in the nearby **box**, should prove suitable for this application. The ratiometric option for the oscillator can be equally useful with bridge transducers.

The oscillator's output is fed to two halves of a dual op amp, with each half buffered by a 75-mA bipolar output stage. Although shown in **Fig 8** as driving a 1-kΩ/leg bridge (a load not directly suitable for typical IC op-amp loading), this buffer can drive even lower impedance bridges, down to 300Ω/leg. Note that the feedback resistors (R_1 through R_4) for the two driver amplifiers should be stable types with low temperature coefficients that track. This type of temperature-coefficient performance can best be realized using a single resistor-array device.

In addition to balanced modulation/demodulation op-

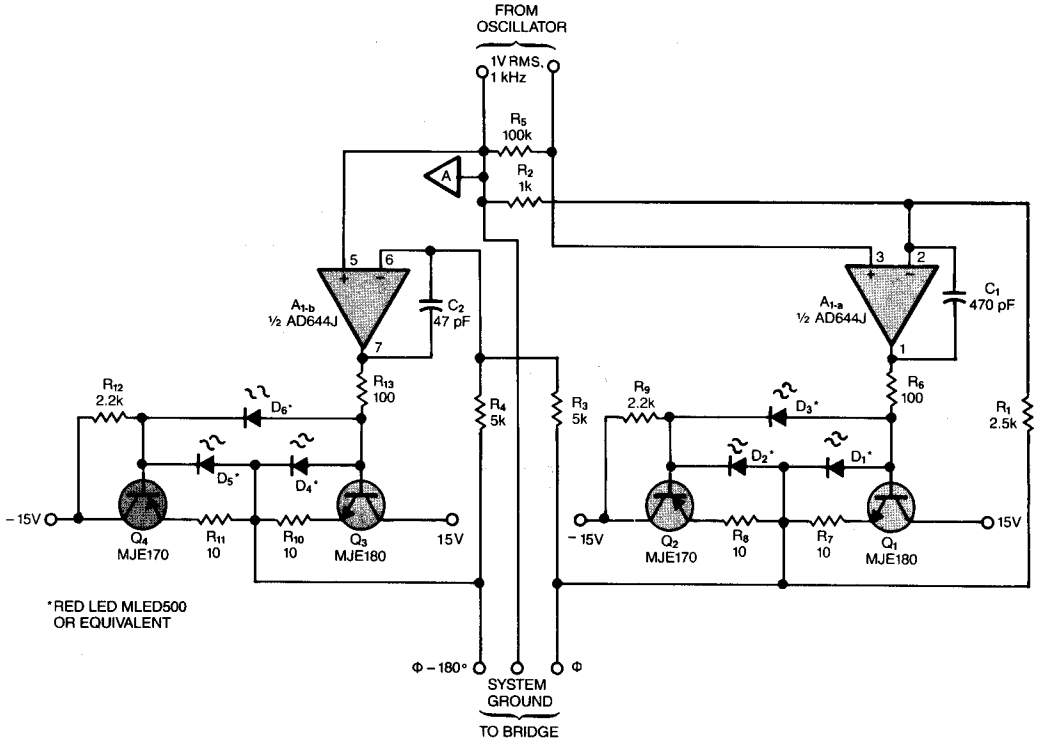


Fig 9—To drive the ac bridge *in Fig 8, this driver circuit produces two 5V peak sine waves that are 180° out of phase. Using these balanced signals maximizes system sensitivity.*

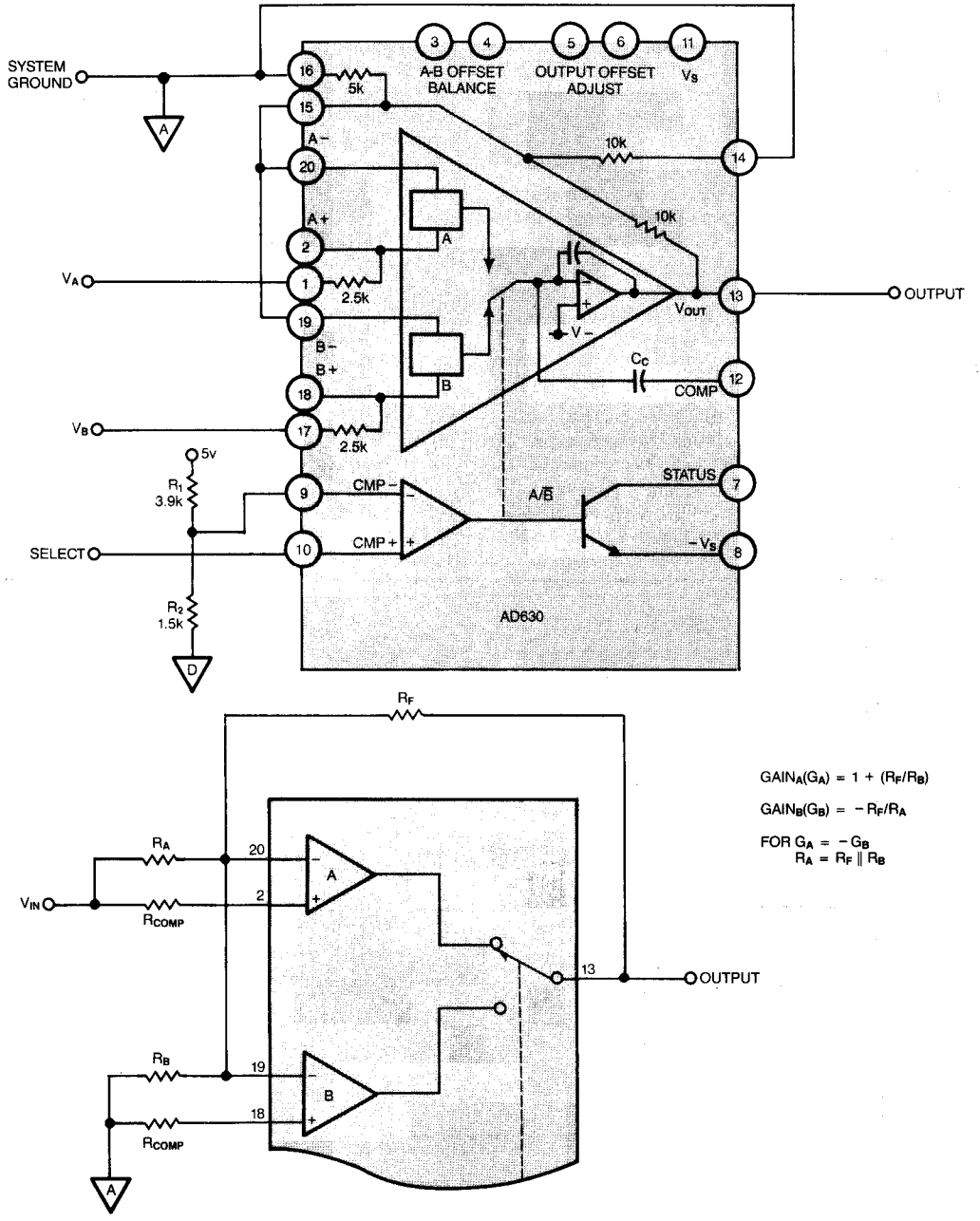


Fig 10—A dual-channel gain block *can be built using the AD630's internal resistors* ***(a)*** *or with external resistors* ***(b)*** *for a greater range of gains. In either case, you can select the desired port with a TTL-level input by adding the R_1-R_2 network* ***(a)*** *to the negative input of the chip's comparator.*

eration needed for transducers such as LVDTs and ac bridges, instrumentation applications typically need a general-purpose programmable-gain block. A commutating modem such as the AD630 can also fill this need, reducing the variety of parts needed for an application. It can be configured for either common or separate signal inputs to the A and B stages.

Use commutating modems as a gain blocks

Fig 10a shows the AD630 configured as a 2-channel, buffered, noninverting multiplexer with a gain of 4 on both channels. Jumper programming the on-chip gain resistors as shown yields the gain of 4; you can also jumper program gains of 1, 2 and 3 using the internal resistors only. Resistors R_1 and R_2 bias the on-chip comparator's negative input to +1.4V so that a TTL 1 at the positive input selects channel A and a logic 0 selects channel B.

Because this circuit is self-contained and can achieve both high ac and dc precision, it can be quite attractive as a basic "no-hassle" gain block. For example, the device makes a good audio-frequency gain block because it has a high slew rate and low input-stage noise, typically on the order of 10 nV/Hz$^{1/2}$.

With a few external resistors, a more extensive variety of gains is possible. **Fig 10b** shows this more general configuration. In this circuit R_F and R_B set a positive gain, G_A, and R_F and R_A set a negative gain, G_B. **Fig 10** notes the relationships for these gains, which can be equal on both channels or unequal.

Although it might not be obvious at first glance, the AD630 is also uniquely suited to precision timing applications that might be needed in instrumentation as well as other applications. It is so suited because it contains all the active circuitry needed to generate a square wave with amplitude and frequency characteristics.

Build precision timing circuits

With a commutating modem, a relatively straightforward approach to ensuring that the output has a predictable amplitude is to use a well-defined dc reference voltage as the input. Such an approach causes the output of the modulator (the square wave) to have an amplitude precisely ±K times the input reference voltage. Switching between these two states creates a square-wave output, and the switching rate (the frequency of the square wave) depends on the timing circuitry used to control switching.

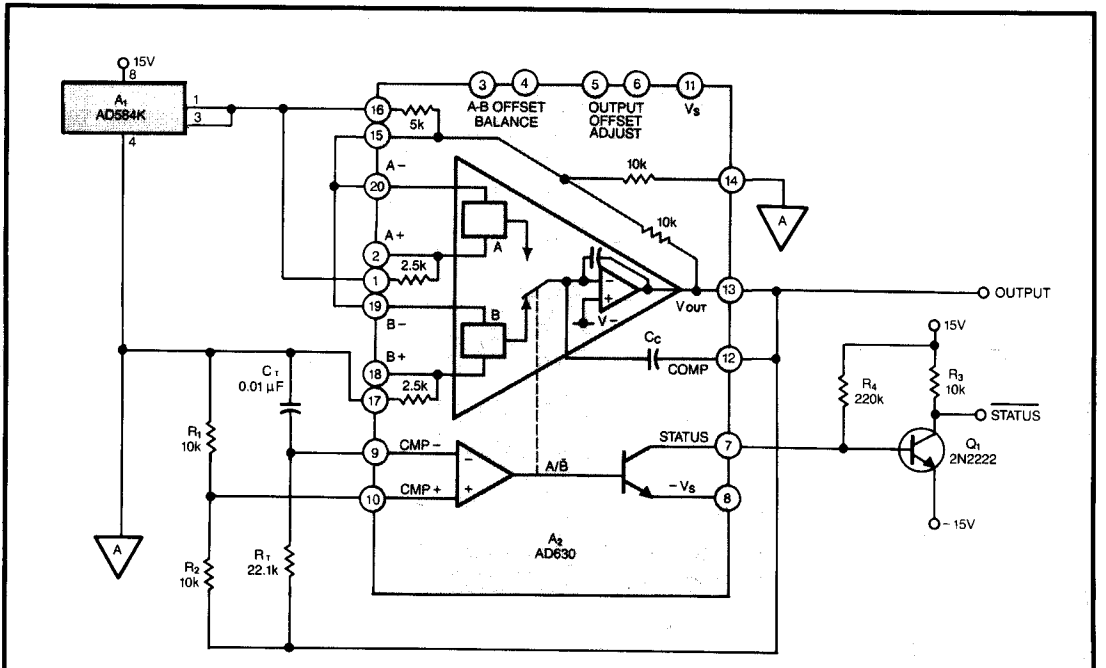


Fig 11—To produce a square wave *with a precise, 10V p-p amplitude, the AD630 switches the polarity of the AD584K's precision 2.5V dc output and multiplies it by a gain of 2. The square wave's frequency is set by C_T and R_T; in this case, it's about 2 kHz.*

Precise timing generation is also a commutating modem's forte

In **Fig 11**, the AD630 is hooked up as a switched-gain amplifier, with an absolute gain, K, of 2 set as in **Fig 4**. With the gain set at 2, the peak output is 2 times V_{REF}, and the peak-to-peak output equals $4V_{REF}$. An AD584 precision reference-voltage source furnishes V_{REF}; connecting its pin 1 to pin 3 straps it for a +2.5V dc level, yielding the 5V pk, or 10V p-p, circuit output. In choosing a V_{REF} source, be certain that it has a low output impedance to minimize possible side effects from the dynamic loading of the switched-input AD630.

The applied reference voltage, V_{REF}, and the particular gain setting programmed into the AD630 determine the accuracy and stability of the output's amplitude. The basic tolerance applicable to an AD584K reference is 0.12%. Using an AD630AD (or AD630JN) strapped for a gain of 2, the output's amplitude error is only 0.1% greater than that of the reference used, indicating less than 0.25% overall (untrimmed) output-amplitude tolerance for the circuit. This level of precision allows the circuit to be useful as an amplitude calibrator.

The two networks at pins 10 and 9 (the comparator inputs) define the circuit's switching characteristics. The R_1-R_2 resistor network provides positive feedback, and the R_T-C_T network determines the timing delay in switching between states. The timing expression for the circuit is:

$$f = 1/(2.2R_TC_T).$$

As with all such RC-time-constant oscillators, the predictability and stability of this circuit are only as good as those of the components used, particularly those in the external timing networks. Both the R_1-R_2 and the R_T-C_T networks should have low temperature-coefficient components; metal-film resistors should be used for R_1, R_2, and R_T, and C_T should be a low-dielectric-absorption polystyrene or polypropylene film capacitor **(Ref 5)**.

Using the components shown, the frequency of the output square wave is approximately 2 kHz. The circuit operates with the best predictability and accuracy below 10 kHz, but it can be used with minor degradation to frequencies as high as 100 kHz.

A virtue of the timing scheme used in this circuit is that a comparison is done between a fraction of the output voltage and an exponential timing ramp derived from it. This basic scheme, popularized by the ubiquitous 555 timer **(Ref 5)**, provides high immunity to changes in output frequency with changes in output amplitude. The practical advantage of this scheme is that the reference voltage can be programmed for different amplitudes, and the AD630 can be strapped for different gains without disturbing the nominal operating frequency.

Although the main square-wave output from the AD630 provides ±5V in this circuit, the status output of the AD630's comparator is also available. This output, buffered by a discrete npn transistor as shown, provides an inverted status signal, which swings from +15 to −15V and can be interfaced easily to logic stages.

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