ANALOG DEVICES

AN-935
APPLICATION NOTE

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Designing an ADC Transformer-Coupled Front End

by Rob Reeder

INTRODUCTION

The five step process in this application note helps the design of an optimum ADC front end for narrow-band applications based on a high intermediate frequency.

Analog signals are often digitized as quickly as possible in modern communications systems and test equipment in order to perform signal processing in the digital domain. However, designing the transformer front end circuitry for an analog-to-digital converter (ADC) can be challenging, especially in systems with high intermediate frequencies (IFs). Fortunately, this streamlined, five step process can help develop an optimum front end for an ADC. It can be applied easily and quickly to achieve the desired performance in almost any application.

The five step process is based on the following straightforward and logical procedure:

1. Know the system and the design requirements.
2. Determine the ADC input impedance.
3. Determine the ADC baseline performance.
4. Select transformer and passive components to match the load.
5. Bench test the design.

STEP 1: KNOW THE SYSTEM AND THE DESIGN REQUIREMENTS

The first step sounds obvious, but just knowing the requirements of a particular application can quickly cut down the number of iterations that must be done by selecting the right components from the start and quickly achieving the desired performance. Make a list of each design requirement, and set desirable boundaries to work within. This enables the selection of the ADC and transformer to go quickly.

For example, assume an application that requires a sampling rate of 61.44 MSPS to capture input signals across a 20 MHz band centered at 110 MHz (100 MHz to 120 MHz). The required signal-to-noise ratio (SNR) of better than 72 dB implies the use of a 14-bit ADC to provide the needed SNR performance. The power consumption should be less than 500 mW per channel. A quick search for an ADC that can meet these system-level performance requirements led to the 14-bit, 80 MSPS AD9246 ADC from Analog Devices, Inc., designed to run on supplies from 1.8 V to 3.3 V. The device was selected for its wide bandwidth and low power consumption (See Table 1).

In this example design, the ADC is fed with an input 110 MHz IF with 20 MHz bandwidth and 61.44 MSPS sampling rate. Because the bandwidth is narrow (one Nyquist band), a resonant match technique is used. This type of match provides less bandwidth, but allows excellent matching over the specified frequency range. This technique usually requires the addition of an inductor or ferrite bead directly across the analog inputs to resonate the parasitic capacitance away from what is seen by the ADC input stage. If the IF of interest is in baseband (first Nyquist), a low-pass filter can be derived using a simple RC network.

Table 1. Design Requirements Example

Boundaries	Input Impedance (Ω)	VSWR	Pass-Band Flatness (dB)	IF –3 dB BW (MHz)	SNR (dBc)	SFDR (dBc)	Input Drive Level (dBm)
Ideal Value	50	1	<0.5	150	72	85	4
Design Limit	30	1.5	<1	300	69	80	7

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STEP 2: DETERMINE THE ADC INPUT IMPEDANCE

The second step in the process involves finding the ADC input impedance (see Figure 1). The device in question, the AD9246, is an unbuffered or switched-capacitor ADC. This means that the input impedance is time varying and changes with respect to analog input frequency. To determine the input impedance for this device, the spreadsheet on the AD9246 product page can be used. From this spreadsheet, find the impedance measured at 110 MHz in the track mode. In this example, the ADC internal input load looks like a differential 6.9 kΩ resistor in parallel with a 4 pF capacitor. It is best to match in the ADC track mode, because this is when the ADC is actually taking the sample. Table 2 shows a portion of the spreadsheet from the AD9246 product page.

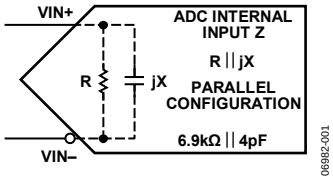

Figure 1. The Internal Input Impedance of an ADC can be Viewed as a Parallel Configuration of a Resistance with a Capacitance

Table 2. AD9246 Input Impedance in Parallel Configuration[1]

Frequency (MHz)	Track Mode		Hold Mode	
	R (kΩ)	C (pF)	R (kΩ)	C (pF)
109.02	7.012504	−4.023861	23.621962	−2.219631
109.64	7.001112	−4.020610	23.501558	−2.219192
110.27	**6.909521**	**−4.017265**	**23.226639**	**−2.218956**
110.89	6.806530	−4.013601	23.724023	−2.218073
111.52	6.750957	−4.012279	23.477964	−2.216845
112.14	6.695931	−4.010091	23.463246	−2.216127

[1] Bold line indicates values used in the example design.

STEP 3: DETERMINE THE ADC BASELINE PERFORMANCE

The third step involves determining the ADC baseline performance to better understand how the ADC behaves before trying to optimize all of its design parameters. To establish this reference, use the evaluation board as configured in its default condition. This is most likely how the ADC was characterized for the specifications shown on the product data sheet.

Next, start gathering the performance specifications. This can be achieved by collecting a fast Fourier transform (FFT) with a 110 MHz input frequency at −1 dB full scale (dBFS), yielding an SNR of 72 dB and an spurious-free dynamic range (SFDR) of 82.7 dBc, close to the data sheet specifications. Characterization should be performed with a high performance signal generator and filter to clean up any signal generator harmonics and spurious content when performing the testing.

Following this, the filter is removed and the ADC's evaluation board is reconnected to the test signal generator. The output level of the generator should be readjusted and noted, in this case 14 dBm, in order to collect the input drive number. The input frequency should be swept over enough bandwidth to see how the pass-band flatness changes and to achieve the –3 dB points[1]. In this case, the front end default configuration has a simple RC filter, which makes for a pass-band flatness of 1.2 dB and a bandwidth of about 100 MHz.

Now that this data has been collected, it is time to make some decisions. With a requirement of 72 dB SNR and 83 dBc SFDR, it is essential that an antialiasing filter (AAF) be used to improve the spurious performance and keep the signal harmonics low. However, this does not solve the input drive and pass-band flatness issues. The AAF on the default evaluation board quickly attenuates the pass band of interest. Using a simple shunt inductor can help, because it provides less attenuation at the frequency of interest, and it rolls off more graciously outside the band. For the input drive, a 1:4 transformer can be used to achieve the full scale of the ADC. This gains the signal by +6 dB, thus offsetting the input drive requirement even more. Finally, the input impedance and VSWR should be measured with a vector network analyzer (VNA). Dial in the frequency of interest to see how well the input matches. In this case, 35 Ω was measured at 110 MHz, yielding a VSWR of 1.44:1.

STEP 4: SELECT TRANSFORMER AND PASSIVE COMPONENTS TO MATCH THE LOAD

The fourth step in the procedure involves selecting the transformer and passive components to match the impedance of the load. In the previous step, the foundation was laid by creating a baseline. Next, the transformer and component values for both R and L must be selected to match the load and create a new AAF that achieves the desired overall performance between the ADC and secondary of the transformer (Figure 2).

[1] For more information on testing ADCs, refer to AN-835.

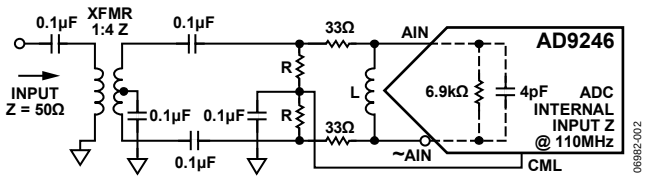

Figure 2. Front End Schematic Diagram; Resistor and Inductor Values Must be Selected to Match the Load

This is where experience or experimentation can come into play. Selecting the transformer can prove to be difficult, because the performance of different transformers can vary widely. The transformer for this example was chosen because it has been measured and its capabilities are understood. In general, it is important to choose a transformer with a good phase imbalance characteristic. This example application has a narrow bandwidth and requires a low input drive, so a known transformer with a 1:4 impedance ratio is used.

Some simple guidelines on choosing a transformer for an ADC include a close look at the specifications. For example, the return loss, insertion loss, and phase and magnitude imbalance specifications should be carefully compared. If these parameters are not specified on the data sheet, ask the manufacturer for this data, or measure it using a vector network analyzer. Choosing between a standard flux-coupled transformer or balun is really a matter of meeting the bandwidth requirements. Standard transformers tend to be in the 1 GHz or under region, whereas a balun can achieve much higher bandwidth.

Note that the termination could be split between the primary and secondary, but in this case, only the secondary was terminated in order to minimize the number of components required. Depending on the application, a split termination may make more sense.

Small series resistors should be used on the analog inputs, anywhere from 15 Ω to 50 Ω. In this case, two 33 Ω resistors were used. The reason for this is to limit the amount of charge injection from the unbuffered ADC back onto the analog inputs. This also helps to define a certain amount of source resistance from the preceding stage. In 90% of the cases, 33 Ω can be used, but in some cases, varying this value has proven to increase the performance slightly.

Next, solve for the differential termination on the secondary of the transformer. As the calculation shows, below 251 Ω is a good starting point for the secondary differential termination. 200 Ω would be used with an ideal 1:4 impedance ratio transformer. To start the calculation, use the return loss number at the specified center frequency to calculate the actual characteristic impedance (Z_0).

The following is an example of a calculation for the secondary termination of the transformer. The return loss is found as

$$Return\ Loss\ (RL) = -18.9\ \text{dB}\ @\ 110\ \text{MHz} = 20\log\left(\frac{50 - Z_0}{50 + Z_0}\right)$$

Using this value of the return loss, it is possible to solve for the characteristic impedance of the transformer's secondary.

$$10^{\left(\frac{-18.9}{20}\right)} = \frac{50 - Z_0}{50 + Z_0}$$

where Z_0 = 39.8 Ω.

In an ideal 1:4 impedance transformer, 200 Ω on the secondary should equal 50 Ω on the primary. This is not the case in a real system, however. To determine the real impedance reflected back to the primary, use the value of Z_0 found in the previous step, and follow the simple calculation

$$\frac{Z(Prim\ Reflected)}{Z(Sec\ Ideal)} = \frac{Z(Prim\ Ideal)}{Z(Sec\ Reflected)}$$

$$\frac{39.8}{200} = \frac{50}{X}$$

Solving for X, X = 251 Ω.

Because the transformer has some unaccounted losses, the 251 Ω secondary termination makes up for these losses. This sets up a better termination value to start with on the secondary to reflect back the correct impedance onto the primary of the transformer. In this case, 50 Ω is stated by the design requirements.

Next, the value of the inductance, L, must be determined to resonant away the internal ADC parasitic capacitance. This can easily be done by setting the value of capacitance, C (4 pF), to the value of L.

The following is an example calculation for the inductor, L:

$$X_C = \frac{1}{2\pi fC} = \frac{1}{2\pi \times 110\ \text{MHz} \times 4\ \text{pF}} = 361.7\ \Omega$$

$$X_L = 2\pi fL$$

$$X_C = X_L$$

With these values, it is now possible to solve for L:

$$L = \frac{X_C}{2\pi f} = \frac{361.7}{2\pi \times 110\ \text{MHz}} = 523\ \text{nH}$$

The reactance of L is set to be equal to C. In this case, the 4 pF capacitance turns into an inductance of 523 nH at 110 MHz. This sets a starting point for the value of L.

STEP 5: BENCH TEST THE DESIGN

The final step in the search for an optimum ADC transformer match is to bench test the design with the values of resistance and inductance that have been found in the earlier steps of the procedure. It is important to go back and measure each of the performance metrics, that is, SNR, SFDR, input drive, passband flatness, and input impedance, as was done previously in the default condition to establish the ADC baseline performance.

It is worth noting that both calculated R and L values can differ in order to get the best performance. The value of these components may vary vs. what was initially calculated depending on vendor preference and component size availability. As iterations occur, a spreadsheet helps keep track of the performance metrics as they change from iteration to iteration.

For this example, with the converter at nearly full scale, the SNR and SFDR performance levels were achieved within the goals specified (see Figure 3). At 110 MHz, the SNR is nearly 72 dB while the SFDR is 80 dBc. Figure 4 shows the final performance results measured for input drive, which was 3.1 dBm. It also shows pass-band flatness of less than 0.5 dB over a 50 MHz band. The –3 dB bandwidth of 150 MHz is sufficient for the requirements of the example and offers adequate spurious rejection for this design.

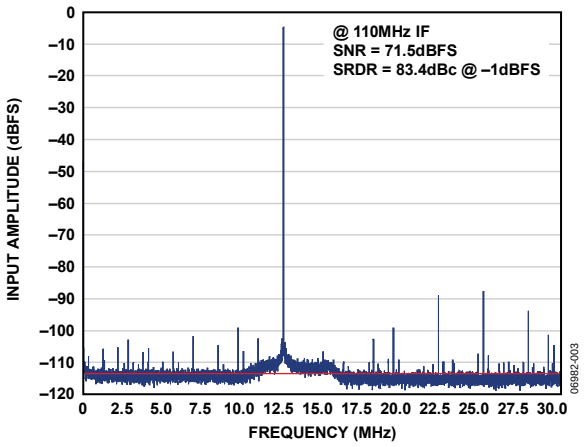

Figure 3. Final Measured Results of the ADC for SNR and SFDR Using the Example Transformer Circuitry

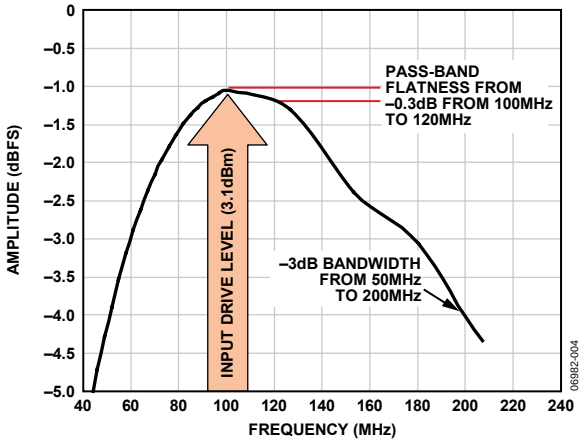

Figure 4. Final Measured Results of the ADC for Input Drive and Pass-Band Flatness Using the Example Transformer Circuitry

Figure 5 shows a combination Smith chart and VSWR plot of the input design as measured by the vector network analyzer. The input impedance is roughly 41 Ω at 110 MHz. The VSWR remains close to 1.2:1 and follows the filter characteristic appropriately.

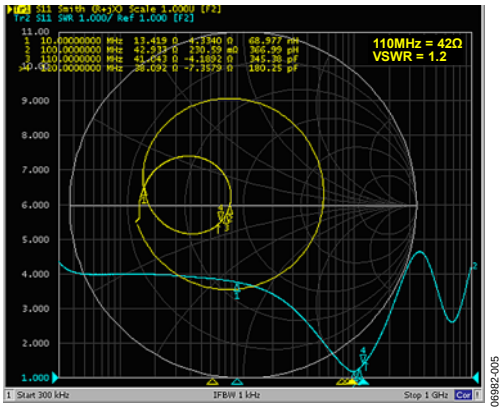

Figure 5. Measured Performance for the ADC Input Impedance and VSWR Using the Example Transformer Circuitry

In the end, this example shows that matching the input circuit or ADC analog front end improves input drive, pass-band flatness (in the IF pass band), and reflective power to the load (VSWR), while achieving the same ADC SNR and SFDR performance as specified in the data sheet.

OPTIONAL STEP 6

An optional sixth step in the procedure involves a comparison of calculated performance with the actual measured results. The impedance results can be calculated and compared to the measured values as a check. The following is an example calculation of the entire input match:

$$X_C = \frac{1}{2\pi fC} = \frac{1}{2\pi \times 110\ \text{MHz} \times 4\ \text{pF}} = -361.7\Omega\,,$$

ADC imaginary impedance

6.9 kΩ||4 pF or (6.9 kΩ + j0)||(0 – j361.7) = (18.9 – j361),
ADC impedance

$$X_C = \frac{1}{2\pi fL} = \frac{1}{2\pi \times 110\ \text{MHz} \times 523\ \text{nH}} = -361.5\,\Omega\,,$$

L imaginary impedance

(18.9 – j361)||(0 + j361.5) = (6.93 kΩ + j72.8)

(6.93 kΩ + j72.8) + (66 + j0) = (6.97 kΩ + j72.8),
Add two 33 Ω resistors

The termination seen at the secondary of the transformer is

(6.93 kΩ + j72.8)||(242 + j0) = (234 + j82.1m)

The magnitude can be found from

$(\text{Re}^2 + \text{jX}^2)1/2 = 234\ \Omega$

By taking the ratio again, as in the fourth step of the procedure,

$$\frac{234}{200} = \frac{50}{X}$$

Solving for X, X = 42.7 Ω. In this case, the measured and calculated impedances were very close.

CONCLUSION

Important points to note when handling a new design are to rank the important parameters in the design and take the time to establish good system and design requirements.

When choosing a transformer, it is important to note that transformers have their differences and the best way to compare different components is by fully understanding the transformer specifications. If specifications are not available, ask the manufacturer for parameters that are not given. High IF designs can be sensitive to transformer phase imbalance. Two transformers or baluns may be needed for very high IF designs to suppress the even order distortions.

When choosing an ADC, establish whether a buffered or unbuffered ADC is to be used. Unbuffered or switched-capacitor ADCs have a time-varying input impedance and are more difficult to design with at high IFs. If using an unbuffered ADC, always input match in the track mode and use the input impedance spreadsheets available on the manufacturer's website. Buffered ADCs tend to be easier to design with, even at high IFs, although they also consume more power than unbuffered ADCs. When calculating the R and L values, note that this proves to be a good starting point. Not all layouts and parasitics are equal on each application, so take note that some iteration may be required to finalize on the performance needed for the particular application.

FOR FURTHER READING

AN-742, Frequency Domain Response of Switched-Capacitor ADCs.

AN-827, A Resonant Approach to Interfacing Amplifiers to Switched-Capacitor ADCs.

ADC switched-capacitor input impedance (S-parameters) data for AD9215, AD9226, AD9235, AD9236, AD9237, AD9244, and AD9245. Go to their product pages, click Evaluation Boards, and upload the Microsoft Excel spreadsheet.

Rob Reeder, "Transformer-Coupled Front-End for Wideband A/D Converters," *Analog Dialogue* 39-2, 2005, pp. 3-6.

Rob Reeder, Mark Looney, and Jim Hand, "Pushing the State of the Art with Multichannel A/D Converters," *Analog Dialogue* 39-2, 2005, pp. 7-10.

Walt Kester, "Which ADC Architecture is Right for Your Application?" *Analog Dialogue* 39-2, 2005, pp. 11-18.

Rob Reeder and Ramya Ramachandran, "Wideband A/D Converter Front-End Design Considerations—When to Use a Double Transformer Configuration," *Analog Dialogue* 40-3, 2006, pp. 19-22.

Rob Reeder and Jim Caserta, "Wideband A/D Converter Front-End Design Considerations: Amplifier- or Transformer Drive for the ADC," *Analog Dialogue* 41-1, 2007, pp. 6-12.

Analog Devices (www.analog.com), AD9246, 80 MSPS/ 105 MSPS/125 MSPS, 14-bit, 1.8 V, switched-capacitor ADC data sheet.

Mini-Circuits, model ADT1-1WT data sheet.

M/A-COM, model ETC4-1T-7 and model ETC1-1-13 data sheets.

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