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APPLICATION NOTE

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Practical Thermal Modeling and Measurements in High Power ICs

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INTRODUCTION

Accurate and precise temperature monitoring of integrated circuits (ICs) is crucial for a wide variety of applications. However, measuring IC temperature is not trivial, as it is not uniform across the device, and it does not just depend on ambient temperature. The active regions of silicon within operating ICs consume power and are consequently responsible for self heating.

Improper temperature, too high or even too low, presents a potential hazard to safe operation and performance. Temperature, if too high, accelerates the aging and thus increases the probability of degenerative processes like metal migration and related failures, for example, bond wire separation from die pads. High temperature can also have negative ramifications on analog performance, operating speed, and timing consistency between components. Furthermore, high temperature can cause unwanted device behavior, such as latch-up.

For this reason, component temperature has historically been a predictor of device failure and overall reliability. Specifically, there is a relationship between frequency and magnitude of temperature change, caused by the power of a device cycling on and off, and failures. Accurate temperature estimation is, therefore, essential for increased performance and consistency.

This application note provides an intuitive understanding by giving a quick overview of the basic theory, established standards, and practice behind estimating junction temperature using a temperature sensitive parameter (TSP) of a circuit, such as the forward voltage drop of a diode, within the device under test (DUT). It explains the temperature testing methodology of ICs and provides the results for contemporary high speed analog-to-digital converters (ADCs).

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REVISION HISTORY

10/2016—Revision 0: Initial Version

BRIEF BACKGROUND ON THERMAL MODELS

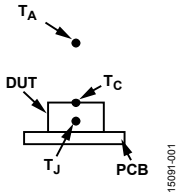

Figure 1. Simple Thermal System with an Active Component

Figure 1 shows the ideal thermal setup. The DUT is encapsulated in a protective layer, the package or case, which can be metal or plastic. The DUT is mounted on a printed circuit board (PCB), resulting in the active region of the silicon being located somewhere in the package. The temperature of the active region is referred to as the junction temperature, T_J. The top of the package is called the case temperature, T_C. The environment surrounding the system is air at a constant ambient temperature, T_A.

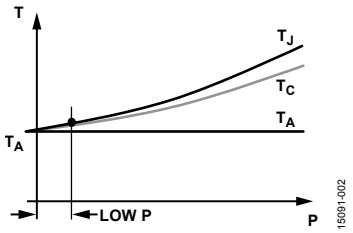

Figure 2. Increase in Temperature Connected to Increasing Power Consumption

Increased power consumption is closely tied with increased junction temperature, as shown in Figure 2. The exact nature of this relationship can be complicated: it can be nonlinear, and cause and effect are not trivial.

The following is an example of the latter case. An increase in power can increase the junction temperature, because the DUT is self heating. However, an increase in temperature can improve conductivity in semiconductors, thereby increasing the power consumption. This is a positive feedback, referred to as thermal runaway, and can have extreme consequences.

An example for the nonlinear behavior can be observed in CMOS devices. Dynamic (switching) currents tend to be more affected by clock speed and less by temperature changes, while static (leakage) currents directly depend on the transistor off state, which is defined by the transistor threshold voltage that depends on temperature. Thus, an exponential connection between power and temperature is more frequently seen in circuits dominated by static currents.

For practical purposes, this application note uses a linear approximation; however, the validity of this simplification must be carefully evaluated for every case.

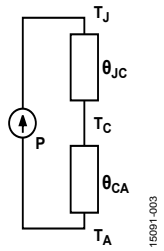

Figure 3. Thermal Circuit Model

The linear approach allows many similarities to be made to electrical circuits, and concepts like thermal resistance can be introduced to model the thermal system. Figure 3 shows such a model.

$$P = \frac{T_J - T_C}{\theta_{JC}} = \frac{T_C - T_A}{\theta_{CA}} = \frac{T_J - T_A}{\theta_{JA}}$$

Where the consumed power (P) takes the role of a current source, the circuit nodes represent the established points of the structure with temperatures (T_J, T_C, T_A) and behave like voltage nodes, and thermal resistances (θ_{JC}, θ_{CA}) are the load. A linear connection between temperature and power yields constant thermal resistance values.

According to various standards organizations, such as Semiconductor Equipment and Materials International (SEMI), Electronic Industries Alliance (EIA) and the Joint Electron Device Engineering Council (JEDEC), if the heat flow path between two points of the structure is unambiguous and well defined, the Greek letter theta (θ) can be used to represent the thermal resistance of the path. However, there are many scenarios where heat flows along alternative paths as well, and only the total power consumption is known, not the path specific power consumption. In such cases, the Greek letter psi (Ψ) is used to indicate this uncertainty. For example, the model in Figure 3 suggests that heat only flows from the active region to the case, where it is dissipated to the surrounding air. However, it is possible for the heat to flow to the PCB as well, where it can also be dissipated. Therefore, the path through the case can only technically be defined as

$$\frac{T_J - T_A}{P} = \Psi_{JA} \approx \theta_{JA}$$

For the sake of simplicity, it is assumed that there are no alternative paths, and theta is used.

As a side note, thermal capacitances can also be defined along the same lines to account for and model transient behavior; however, devising such models requires complex system identification, which is beyond the scope of this document.

STATIC MODE AND CASE TEMPERATURE

Historically, the junction temperature has been estimated by directly measuring the case temperature, for example, using thermocouples, given that the difference between T_J and T_C was negligible, as shown in Figure 1. The underlying assumption is that P and θ_{CA} are low. With P, T_C, and T_A measured, the overall θ_{JA} can be established as well, which is referred to as the static mode approach in the EIA/JEDEC standard "Integrated Circuits Thermal Measurement Method—Electrical Test Method (Single Semiconductor Device)".

This approach may not yield reproducible results because of the sensitive nature of thermocouple placement. Furthermore, as power increases, T_C and T_J likely diverge. Recently, device power consumption has been steadily increasing because of the increase in overall complexity, for example, multiple channels and digital signal processing (DSP) blocks in newer ADCs. These new ICs may not have a low power mode, thus rendering the approach infeasible.

DYNAMIC MODE AND TEMPERATURE SENSITIVE PARAMETER

Contemporary devices follow the dynamic mode approach outlined in the EIA/JEDEC standard and include dedicated temperature measurement units (TMUs). These specialized circuits feature a temperature sensitive parameter (TSP), for example a temperature dependent voltage value, which is used to estimate junction temperature and thermal resistances.

Part of this standard is to take two measurements, as opposed to taking only one measurement as in static mode approach. The system goes from one steady state to another.

$$P_1 - P_2 = \frac{T_{J1} - T_A}{\theta_{JA}} - \frac{T_{J2} - T_A}{\theta_{JA}} = \frac{T_{J1} - T_{J2}}{\theta_{JA}}$$

$$\Delta P = \frac{\Delta T_J}{\theta_{JA}}$$

Utilizing the assumption in the standard, a linear connection between T_J and a TSP is declared:

$$T_J = KV_{TSP} + T_0$$

where:
V_{TSP} is the TSP.
K is the linear coefficient.
T_0 is the intersection point for the linear model.

The temperature analysis can then be rewritten as follows:

$$\Delta P = \frac{\Delta T_J}{\theta_{JA}} = \frac{T_{J1} - T_{J2}}{\theta_{JA}} = \frac{KV_{TSP1} + T_0 - KV_{TSP2} - T_0}{\theta_{JA}}$$
$$= \frac{K\left(V_{TSP1} - V_{TSP2}\right)}{\theta_{JA}} = \frac{K\Delta V_{TSP}}{\theta_{JA}}$$

The dynamic mode approach immediately mitigates the problem of thermocouple placement and lack of low power mode. The results are more repeatable and more accurate. Furthermore, θ_{IC} and the thermal capacitances and resistances of the surrounding environment can be measured using only the built-in TSP, as outlined in the JEDEC Standard "Transient Dual Interface Test Method for the Measurement of the Thermal Resistance Junction-to-Case of Semiconductor Devices with Heat Flow Through a Single Path".

However, this analysis depends on precise junction temperature to TSP characterization, meaning a good estimate for K. The standard suggests a temperature sweep in low power mode for this purpose; however, that defeats one of the key reasons for moving away from the static mode: lack of a low power mode. This application note describes the solution for this exact problem, but first, commonly used TMUs need to be discussed.

DIODE-BASED TEMPERATURE MEASUREMENT UNITS

Most electrical parameters depend on temperature in one form or another. However, in practice, the forward voltage drop of diodes under constant current, as shown in Figure 4, are employed as TSP in most cases.

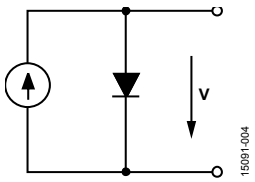

Figure 4. Constant Current Through a Single Diode

Most ICs already contain several diodes in the form of electrostatic discharge (ESD) protection circuits on pins. However, it is not obvious how these can be utilized under normal operating conditions. Instead, dedicated diodes are at the heart of TMUs.

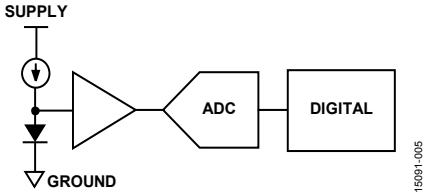

Figure 5. Complete Temperature Measurement Unit Solution

A complete TMU solution might also feature a voltage buffer, an ADC, and digital logic as well, as shown in Figure 5. This TMU solution can provide temperature values during normal operation for other parts of the system via various interfaces, like I^2C, SPI, or APB. The real-time results can be utilized to tune or correct the operation of other circuits. However, this application note focuses only on the diode circuit portion.

The forward voltage drop follows a well established temperature dependence. The current through the diode is expressed as follows:

$$I = I_S(T)\left(e^{\frac{V}{V_T}} - 1\right) = I_S(T)\left(e^{V\frac{q}{kT}} - 1\right) \approx I_S(T)e^{V\frac{q}{kT}}$$

where:
$I_S(T)$ is the reverse saturation current.
V is the voltage drop.
q is the unit charge of an electron.
k is the Boltzmann constant.
T is temperature.

The equation seems deceptively simple at first glance, and the user might be tempted to express the temperature in terms of the voltage. However, the reverse saturation current is also temperature dependent. Even a theoretical analytical expression for T is too complicated for practical purposes.

However, the complete picture is even more complicated. The TMU is necessarily made up of other components, like current sources and resistors, which likely also depend on temperature. Experience shows that just adding the base and emitter resistances of a diode connected transistor in contemporary silicon process technology can lead to tens of degrees error.

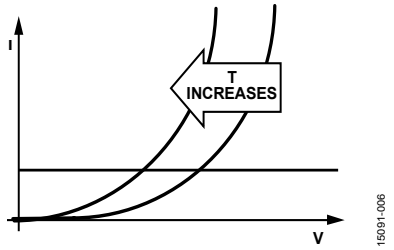

Figure 6. Diode I-V Curve—As Temperature Increases, Forward Voltage Drop Decreases for a Given Current

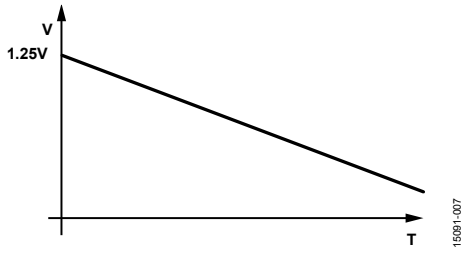

Figure 7. Diode Temperature Curve—As Temperature Increases, Forward Voltage Drop Decreases for a Given Current

Therefore, deriving a precise analytical expression for T is practically impossible. Only through extensive characterization is the relationship between the temperature and the voltage revealed; however, one observation can be made: an increase in temperature results in a decrease in voltage, as shown in Figure 6 and Figure 7. This is referred to as complementary to absolute temperature (CTAT) behavior, and is assumed to be linear in practice. As a side note, at absolute zero (that is, T = 0 K), the forward voltage drop of an ideal diode equals the bandgap voltage parameter of silicon, which is approximately 1.25 V.

However, even if a single diode is thoroughly characterized, the behavior of semiconductor devices can vary greatly from device to device because of uncontrollable process variations. The steepness of the ideal, linear voltage to temperature relationship, as shown in Figure 7, likely varies from diode to diode, because of varying physical parameters, like size, which can affect the reverse saturation current.

The circuit diagram of one possible solution to this issue is shown in Figure 8. The voltage drop on two diodes is compared, one of them significantly larger, for example, N = 20 times. Using the same current source, a process independent TSP can be derived. The random effects of process variation and, consequently, device dependent T_J estimation can be mitigated.

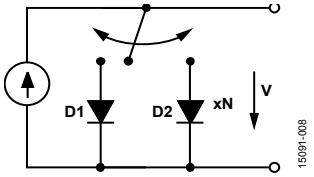

Figure 8. Constant Current Through a Diode Pair

The current through diode one,

$$I = I_1 \approx I_S(T)e^{V_1\frac{q}{kT}}$$

and the current through diode two,

$$I = I_2 \approx NI_S(T)e^{V_2\frac{q}{kT}}$$

can be used to find the voltage difference at point T,

$$V_{TSP} = V_2 - V_1 = \Delta V \approx \frac{kT}{q}\ln N$$

which is not dependent on the reverse saturation current and process specific characteristics.

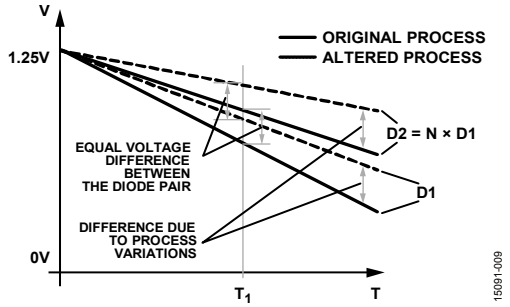

Figure 9. Diode Pairs Have the Same Difference in Voltage for a Given Temperature Regardless of Process Variations

Figure 9 shows how any diode pair can have different absolute voltages at some temperature, T_1, but experience the same voltage difference between the pair.

As a final note, the reverse saturation current can also be eliminated using a single diode but two different current sources. This method may be even better, because current ratios can be accurately set up with current mirrors. The equation for this case is exactly the same as for the diode pair solution.

ESTABLISHING THE RELATIONSHIP BETWEEN TEMPERATURE AND TSP

A diode voltage-based approach is a viable solution; however, the main problem remains that there was no way to characterize the junction temperature to TSP relationship in devices with no low power mode. Also keep in mind that the TSP can be any parameter (directly measured or derived); voltage values are used only as an example.

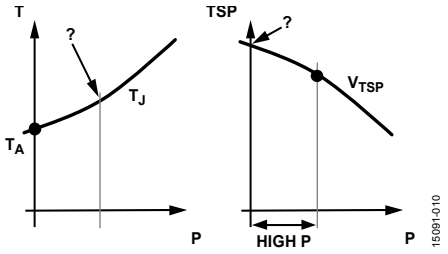

Figure 10. Connection Between T_J and TSP

Figure 10 highlights the fundamental issue. The left side shows that the junction temperature increases with power; however, only one single point on the curve is known: the ambient temperature if the power consumption is zero. The right side shows that the TSP for high power states can be measured; however, the low or zero power readouts are not available. Therefore, there is no state of the system where both the junction temperature and the TSP are known.

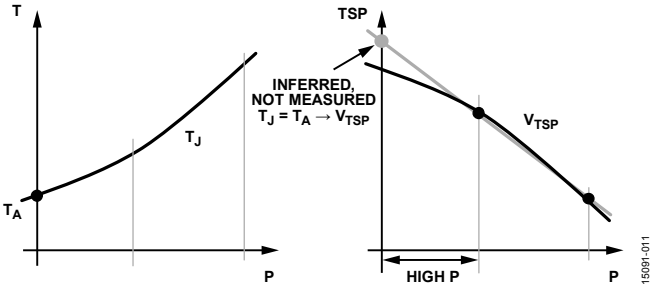

Figure 11. Inferred Voltage Level for TSP at Zero Power

To resolve this issue, the previously discussed assumption in the EIA/JEDEC standard is employed, and a linear connection between TJ and VTSP is assumed: $T_J = K\ V_{TSP} + T_0$. This way the DUT needs to be placed in only a few (at least two) high power states, and the line fitted to the points can be extrapolated. The line intersects the vertical axis for the TSP, as shown in Figure 11 on the right side. This point corresponds to a power consumption of zero on the right coordinate system. However, T_J at zero power consumption is exactly the ambient temperature according to the left coordinate system. Therefore, a connection has been established.

The process is repeated at different ambient temperatures, as shown in Figure 12, to approximate K and T_0.

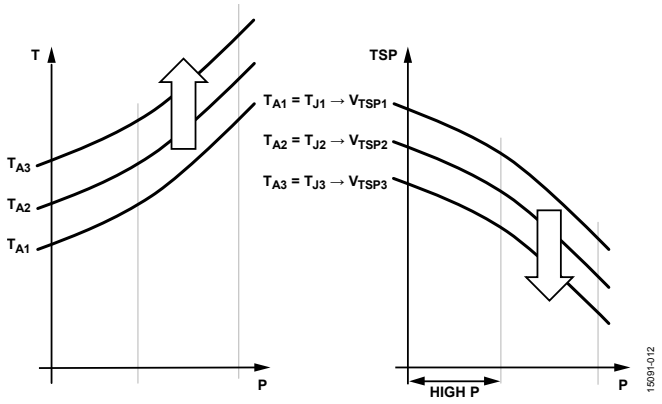

Figure 12. Establishing Voltage vs. Power Curves for Different Ambient Temperatures

RESULTS

Figure 13 shows actual measurements for a contemporary, state of the art, high speed ADC evaluated with this method. The device was placed in nine different power modes, although some of these modes overlapped. The TSP was based on the forward voltage drop difference of a diode pair, one of the diodes being 20 times the size, $V_{TSP} = \Delta V$.

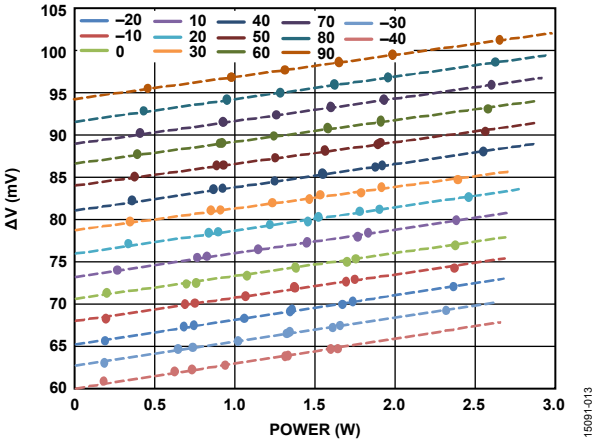

Figure 13. Diode Pair-Based Voltage Difference vs. Power Curves at Different Ambient Temperatures

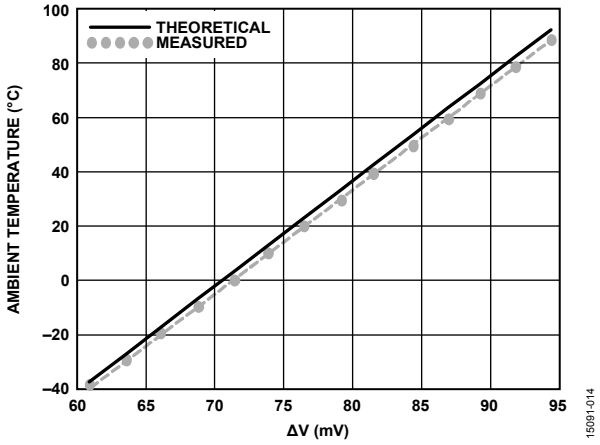

Figure 14. Characteristic TSP—Temperature Relationship

Figure 14 shows the TSP characteristics based on the inferred intersection points. The results for the linear approximation are shown in Table 1. Recall that the theoretical results for a diode pair were also derived; therefore, the measured values can be compared to the theoretical values.

Table 1. Comparison of Measured and Theoretical Results for the Linear Approximation

Values	K (°C/mV)	T_0 (°C)
Measured	3.836	−273.48
Theoretical	$3.874\left(\approx \frac{q}{k\ln 20}\right)$	−273.15 (absolute zero)

PRACTICAL SETUP—THERMAL CHAMBER MODEL

Ambient temperature plays an important role in characterizing the T_J to TSP relationship. In addition, the DUT is conventionally characterized in data sheets at different ambient temperatures, although there is a case for moving away from ambient and towards junction temperature. The latter is independent of PCB design, while the former is not. For example, a 10-layer Rogers Theta material PCB designed for thermal performance can achieve a thermal resistance of approximately 10 K/W (see Table 2).

Table 2. Thermal Resistance Results for Multiple Device and Package Combinations

Product	Package	θ_{JA} (K/W)
AD9625	196-ball BGA	10.0
AD9684	196-ball BGA	9.0
AD9680	64-lead LFCSP	8.8
AD9691	88-lead LFCSP	9.5
AD6684	72-lead LFCSP	9.74

These results required approximately 100 cm^2 surface area, solid, uninterrupted, copper pours (ground and supply) on all layers, which were connected with vias throughout the board, especially under the DUT to conduct away heat. For example, there were 196 vias, 8 mil in diameter for the 196-ball BGA packages, and 225 vias for the 64-lead LFCSP packages. These recommendations may contradict electrical considerations, and are likely not met for actual system designs, which likely result in higher junction temperatures for the same ambient temperature.

In light of these facts, system evaluation must incorporate ambient controlled tests. Professional ovens and oil-based calibration baths are employed in precision tests; however, these tests can be prohibitively expensive. A more straightforward approach is to fabricate a thermal chamber with temperature controlled air inflow, especially considering that many product designs already involve a chassis with one or more fans. Because this is such a common practice and because ambient temperature plays such an important role, the following section examines a simple thermal chamber setup with air inflow and outlet.

However, keep in mind that rigorous thermal analysis involving, for example, complex fluid mechanics analysis is well beyond the scope of this document. This application note only improves the previously defined simple model to the extent it is capable of providing an intuitive understanding.

MODEL

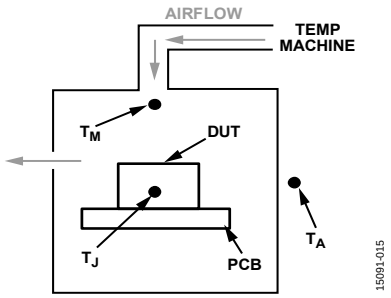

Figure 15. Model of a Typical DUT Setup Within a Closed Environment

Figure 15 shows a typical setup with a closed environment. In this setup, a two way heat transfer is modeled: first, between T_J and T_A, the ambient outside the thermal chamber; and second, between T_J and T_M, the ambient temperature inside as set by a temperature machine, which acts as a constant source of temperature.

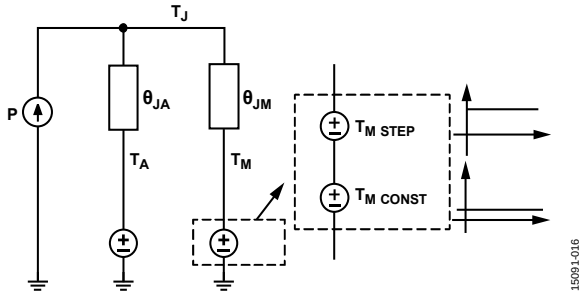

Figure 16. Circuit Diagram Representing Thermal Exchange in the Setup Shown in Figure 15

The circuit diagram in Figure 16 models the transfer of thermal energy.

As a side note, for system identification purposes carried out with step impulses, it makes sense to further divide sources. In case of a linear model, such as this, linear superposition allows T_M to be partitioned into a constant value, equal to the original steady-state temperature and a step value, which is nonzero when the temperature machine is set to a value different from the ambient temperature.

The thermal resistances represent the two ways of heat transfer. The power source represents the power consumed by the DUT.

$$T_J = \theta\left(P + \frac{1}{\theta_{JM}}T_M + \frac{1}{\theta_{JA}}T_A\right)$$

where θ is the equivalent thermal resistance, and is defined as

$$\theta = \frac{\theta_{JM}\theta_{JA}}{\theta_{JM} + \theta_{JA}}$$

However, recall that power consumption and junction temperature can mutually affect each other, which can result in a nonconstant power value and a nonlinear connection.

For example, Figure 17 shows a typical relationship between power and junction temperature for the AD6684 high speed ADC.

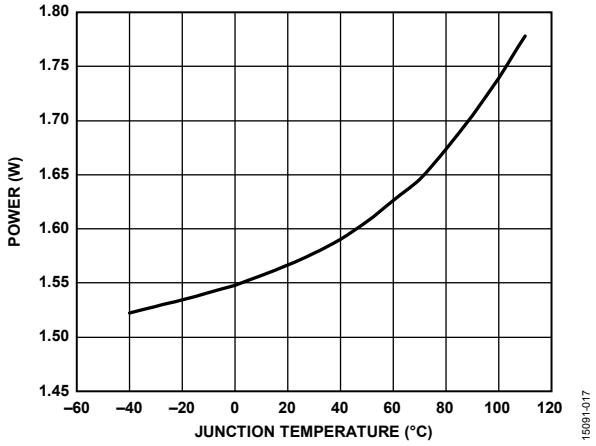

Figure 17. Power vs. Junction Temperature

Parts of the curve can be linearly approximated as

$$P = \alpha T_J + P_0$$

where:
α is the linear coefficient.
P_0 is the intersection point for the linear model.

This complicates the system equation:

$$T_J = \frac{\theta}{1-\alpha\theta}\left(P_0 + \frac{1}{\theta_{JM}}T_M + \frac{1}{\theta_{JA}}T_A\right)$$

CALCULATIONS

The only two unknowns in the model are θ_{JM} and θ_{JA}; therefore, the system can be solved with only two measurements.

A new variable, A, is defined as the slope of T_M vs. T_J.

$$A = \frac{T_{M2} - T_{M1}}{T_{J2} - T_{J1}}$$

Similarly, the following is known:

$$\alpha = \frac{P_2 - P_1}{T_{J2} - T_{J1}}$$

$$P_0 = P_1 - \alpha T_{J1} = P_2 - \alpha T_{J2}$$

θ_{JM} can then be defined as follows:

$$\theta_{JM} = \frac{(T_{M1} - T_A) - A(T_{J1} - T_A)}{\alpha(T_{J1} - T_A) - P_1}$$

And θ_{JA} can be defined in terms of θ_{JM} as follows:

$$\theta_{JA} = \frac{1}{\alpha + \dfrac{A-1}{\theta_{JM}}}$$

RESULTS

The model, as shown in Figure 16, lacks thermal capacitances; therefore, transient behavior is not discussed, only steady states. These are the initial and final states of the system in the step responses. Also recall that the results presented in this document are only meant to provide a rudimentary, intuitive overview. They are only meant to showcase the limitations of the simple, thermal resistance-based models.

Testing was completed on two different AD6684 setups with thermal chambers of approximately 6000 cm^3 volume made of different materials: styrofoam and acrylic glass. Acrylic glass is easy to handle and is commonly used to quickly prototype chassis. Styrofoam is a great insulator because of the trapped air within the material. Additionally, different airflow rates were tested (see Figure 18). The results of testing and the calculated thermal resistances are shown in Table 3.

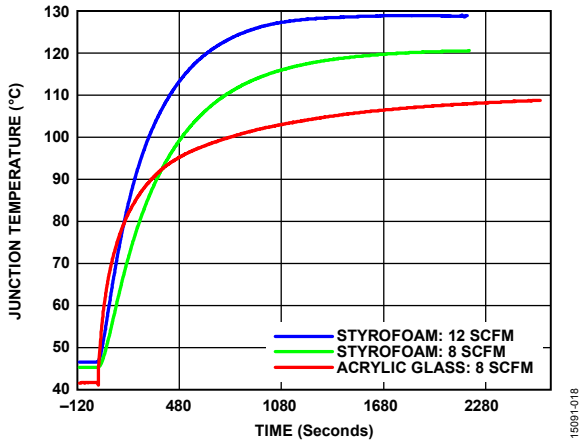

Figure 18. Junction Temperature vs. Time for a Step in T_M

The junction temperature results are along the lines of the model. Styrofoam allows the junction to reach higher temperatures, because the material insulates the DUT and its immediate environment better from the relatively cool ambient. The power numbers show some difference, which is a setup to setup variation; however, even with higher power intake, the acrylic chamber did not achieve the same high junction temperatures. The junction to ambient thermal resistance, θ_{JA}, is also partially in agreement with the model, because it identifies styrofoam as a better insulator. However, airflow has a significant influence on this value, weaknesses are seen in the model that was conceived with conductive heat transfer in mind as opposed to convective (airflow-based).

Table 3. Results of Thermal Chamber Temperature Testing

Material	Airflow (SCFM)	T_{M1} (°C)	T_{M2} (°C)	T_{J1} (°C)	T_{J2} (°C)	P_1 (W)	P_2 (W)	θ_{JA} (K/W)	θ_{JM} (K/W)
Styrofoam	8	25	120	45.4	120.5	1.67	1.94	50.1	16.1
	12	25	120	46.6	128.9	1.67	1.98	73.9	15.8
Acrylic	8	25	120	41.7	108.8	1.74	1.98	30.2	14.1

Finally, the junction to machine temperature resistance, θ_{JM}, is in clear contradictions with the values established in Table 2. In Table 2 a thermal resistance of 10 K/W or less was shown to be possible; however, in Table 3 the resistance from junction to immediate surrounding air is much higher. This discrepancy shows the shortcomings of the linear model commonly used in the industry. A lower thermal resistance is expected due to improved heat dissipation; however, the airflow within the thermal chambers was not optimized, and had unintended and unpredictable effects on the model.

REFERENCES

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