AN-1464
APPLICATION NOTE

One Technology Way • P.O. Box 9106 • Norwood, MA 02062-9106, U.S.A. • Tel: 781.329.4700 • Fax: 781.461.3113 • www.analog.com

AD7172-2, AD7172-4, AD7173-8, AD7175-2, AD7175-8, AD7176-2, AD7177-2, AD7124-4, and AD7124-8 Calibration

by Jonathan Colao

INTRODUCTION

The precision sigma delta (Σ-Δ) products from Analog Devices, Inc., include calibration on-chip, with support for both internal calibration and system calibration. The Σ-Δ products integrate many of the additional building blocks needed in a system; gain and internal reference. Internal calibration minimizes internal offset errors and gain errors. The calibration methods used on the devices calibrate the offset and gain error of all internal blocks; for example, the error of the gain stage is calibrated.

System offset error and gain error calibrations are supported by the converters where external components are calibrated by the analog-to-digital converter (ADC) along with the internal error sources.

This application note discusses in detail the calibration methods used in the AD7172-2, AD7172-4, AD7173-8, AD7175-2, AD7175-8, AD7176-2, AD7177-2, AD7124-4, and AD7124-8.

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REVISION HISTORY

7/2017—Revision 0: Initial Version

OFFSET ERROR AND GAIN ERROR

The ADCs discussed in this application note allow both unipolar and bipolar modes of operation. This section discusses unipolar mode in conjunction with offset and gain errors.

The offset error is the voltage deviation from the ideal value when the ADC code is 000. Figure 1 shows the ADC transfer function.

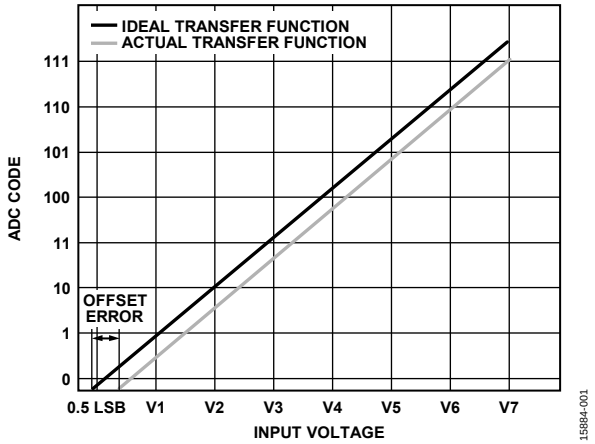

Figure 1. ADC Transfer Function

The gain error of an ADC is the maximum voltage error from the ideal; it is the error at the maximum and minimum input voltage, which is shown in Figure 2.

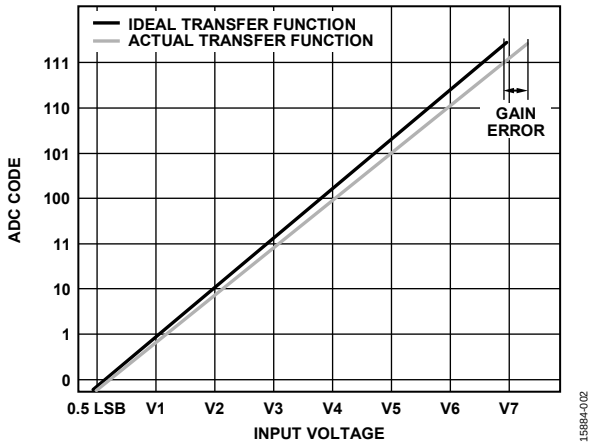

Figure 2. ADC Gain Error

The ADC transfer function in Figure 2 can be equated to a straight line equation of Y = MX + B, which corresponds to

$$ADC\ Code = (Gain\ Error \times Input\ Voltage) + Offset\ Error$$

$$Gain = 2^N \div Reference\ Voltage$$

The offset errors and gain errors of the entire signal chain can be fine tuned, which leads to an overall improved system accuracy. The offset error can be adjusted by performing offset calibration or zero-scale calibration, whereas the gain error implements a gain calibration or a full-scale calibration.

In general, after an analog to digital conversion, the result shows how much error the conversion has. Perform a calibration to ensure that any errors are adjusted. Calibration can be implemented using predefined software on a microcontroller unit (MCU) where the calibration factors are stored in the MCU memory. These calibration factors scale the overall ADC conversion result to remove the gain and offset errors. When this technique is used there is a time penalty, which means that the ADC conversion needs postprocessing on the MCU to ensure the correct value is obtained.

The precision Σ-Δ ADC portfolio from Analog Devices has embedded calibration modes that can adjust the ADC conversion results of the ADC due to the gain and offset errors. These Σ-Δ ADCs have on-chip registers to store the calibration coefficients.

As part of the overall ADC conversion process, these coefficients automatically correct the ADC conversion result for both gain and offset errors. The offset calibration coefficient subtracts from the result prior to multiplication by the gain error coefficient.

CALIBRATION MODES

The AD7124-4, AD7124-8, AD7172-2, AD7172-4, AD7173-8, AD7175-2, AD7175-8, AD7176-2, and AD7177-2 Σ-Δ ADCs use a similar method to perform calibrations.

The AD7124-4 and AD7124-8 are a family of low power, Σ-Δ ADCs that have a completely integrated analog front end used for high precision measurement applications. The AD7124-4 and AD7124-8 support the following four calibration modes:

- Internal zero-scale calibration
- Internal full-scale calibration
- System zero-scale calibration
- System full-scale calibration

The AD7172-2, AD7172-4, AD7173-8, AD7175-2, AD7175-8, AD7176-2, and AD7177-2 are low noise, fast settling, multiplexed Σ-Δ ADCs that support the following three calibration modes:

- Internal zero-scale calibration
- System zero-scale calibration
- System full-scale calibration

These calibration modes are software programmable and can be accessed through the ADC_CONTROL register on the AD7124-4 and AD7124-8 and via the ADC mode register on the AD7172-2, AD7172-4, AD7173-8, AD7175-2, AD7175-8, AD7176-2, and AD7177-2.

Offset (zero-scale) and gain (full-scale) calibrations are conversions with a known analog input. In all cases, $\overline{\text{RDY}}$ goes high when the calibration initiates, and it returns to low when calibration completes.

INTERNAL ZERO-SCALE OFFSET CALIBRATION

For an internal zero-scale offset calibration, the selected positive input pin automatically disconnects and internally connects to the selected negative analog input pin. Therefore, ensure that the voltage on the selected negative pin does not exceed the allowed limits and ensure that any excess noise and interference are not present. Figure 3 shows a block diagram of the internal connection, positive analog input (AINP) and negative analog input (AINM).

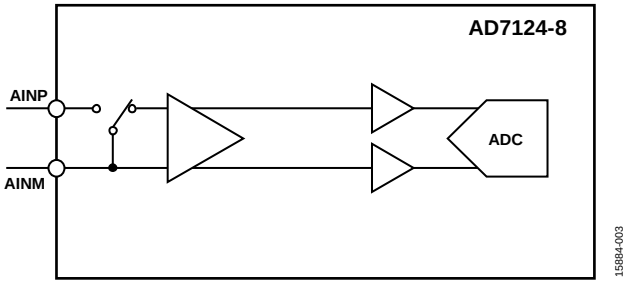

Figure 3. Internal Zero-Scale Offset Calibration

SYSTEM ZERO-SCALE OFFSET CALIBRATION

For a system zero-scale offset calibration, the voltage for calibration must be applied to the ADC input pins. With this type of calibration, the offset of the external circuitry, along with the ADC offset, is diminished from the signal chain. With an input module, for example, the user can short the inputs at the connector terminal so the calibration removes any error due to the signal conditioning as well as the ADC offset. Figure 4 shows the set up of the EVAL-AD7124-4SDZ evaluation board with AIN0 and AIN1 shorted together. The EVAL-AD7124-4SDZ is powered by the ADP1720 and uses the ADR4525 as reference and the EVAL-SDP-CB1Z as the evaluation controller board, which is based on the ADSP-BF527 processor.

The EVAL-AD7124-4SDZ evaluation board and the AD7124-4/AD7124-8 Eval+ Software was used. The AD7124-4 was configured as follows:

- Channel: AIN0 and AIN1
- Pin AIN0 and Pin AIN1 are shorted using LK5 on evaluation board
- V_{BIAS} is enabled
- Gain = 2
- Power mode: full power mode
- Output data rate: 50 SPS

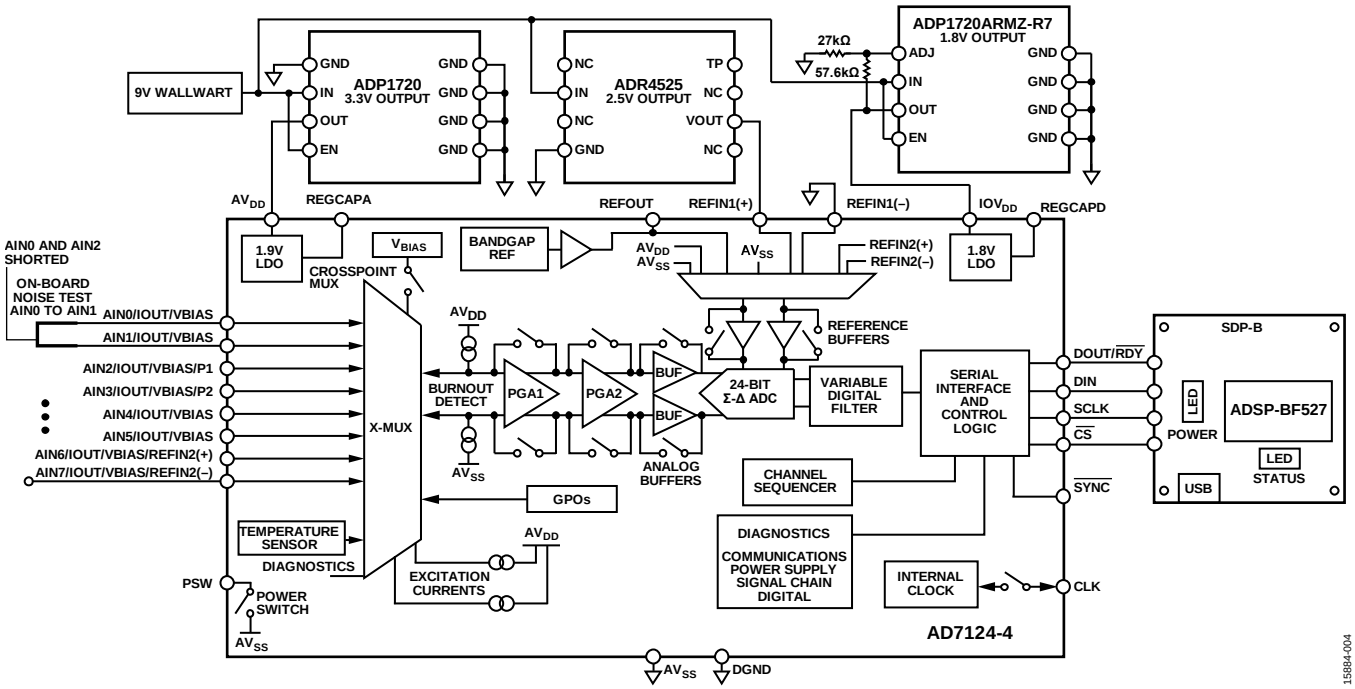

Figure 4. EVAL-AD7124-4SDZ Evaluation Board System Zero-Scale Calibration Set Up

Figure 5 shows the performance of precalibration and post calibration results of the AD7124-4 with AIN0 and AIN1 shorted together. After performing external offset calibration, the offset error was reduced and the conversion results were approximately zero volts. The result from the ADC showed 0x7FFF60 or 24 μV offset without calibration. See the AD7124-4 data sheet for more information.

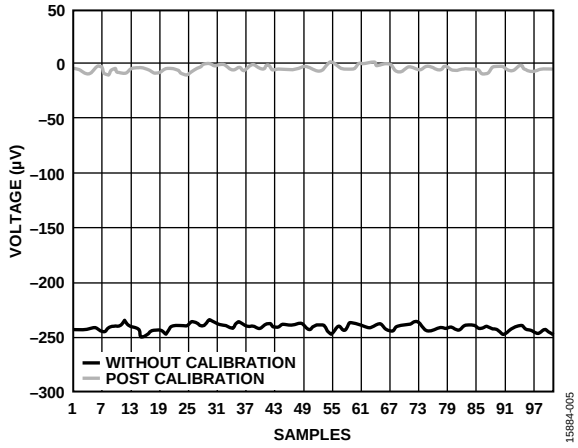

Figure 5. Without Calibration vs. Post System Zero-Scale Calibration

After performing a system zero-scale calibration in low power mode, the offset register was updated to 0x7FFF89. Performing a conversion, the ADC result was 0x7FFFFC (approximately 120 nV average), which is in the order of the noise, approximately 330 nV RMS.

INTERNAL FULL-SCALE GAIN CALIBRATION

An internal full-scale gain calibration ensures that a near full-scale input voltage automatically connects to the selected analog input.

The AD7124-4 and AD7124-8 include a resistor network, which enables the ADC to generate a signal of magnitude V_{REF} ÷ gain. This allows the device to support internal full-scale calibration at each gain.

Note that internal full-scale (gain) calibrations cannot be performed on the AD7124-4 and AD7124-8 in full power mode; low or mid power mode must be used. It is acceptable to perform internal full-scale gain calibration in low or mid power mode and switch back to full power during the conversion. The calibration coefficient still applies if the same reference and gain are used.

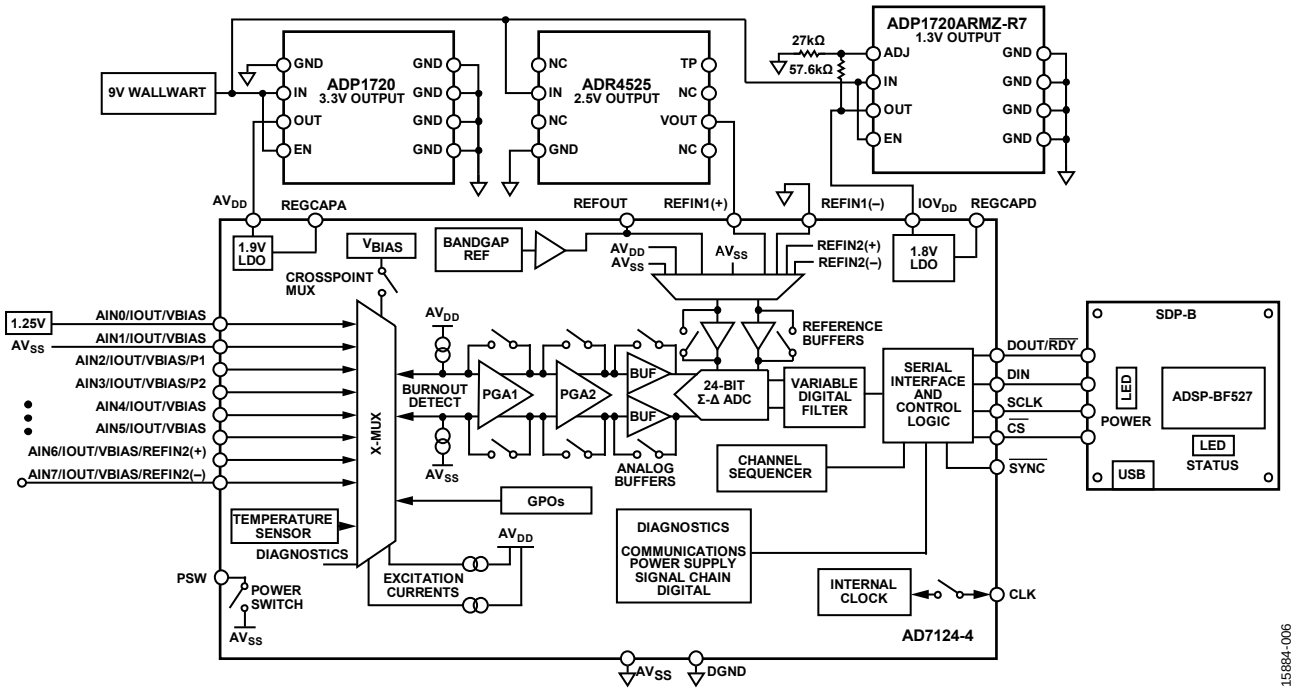

Figure 6. EVAL-AD7124-4SDZ System Full-Scale Calibration Set Up

SYSTEM FULL-SCALE GAIN CALIBRATION

A system level full-scale gain calibration requires a full-scale voltage to be applied to the inputs. The result of this type of calibration reduces any gain errors that are external to the ADC, along with the gain error of the ADC. Using an input module as an example, the full-scale signal can be applied to the module inputs rather than the ADC inputs for the duration of the calibration so that the gain error of the complete module calibrates. Figure 6 is a block diagram of the AD7124-4 system full-scale calibration using the EVAL-AD7124-4SDZ evaluation board. To perform a system full-scale calibration, a full-scale voltage is input on the AIN0 (1.25 V at gain = 2) with AIN1 connected to AV_{SS}.

Figure 7 shows the performance of the AD7124-4 and AD7124-8 system gain calibration routine. Again, the EVAL-AD7124-4SDZ evaluation board and software was used, and the AD7124-4 was configured as follows:

- Channel: AIN0 and AIN1
- Bipolar mode
- Gain = 2
- Power mode: full power mode
- Output data rate: 50 SPS

With AIN1 connected to AV_{SS}, a 1.25 V voltage is applied to AIN0 via connector J6. Prior to calibration, it generates an ADC output code of 0xFF13C (16,744,765).

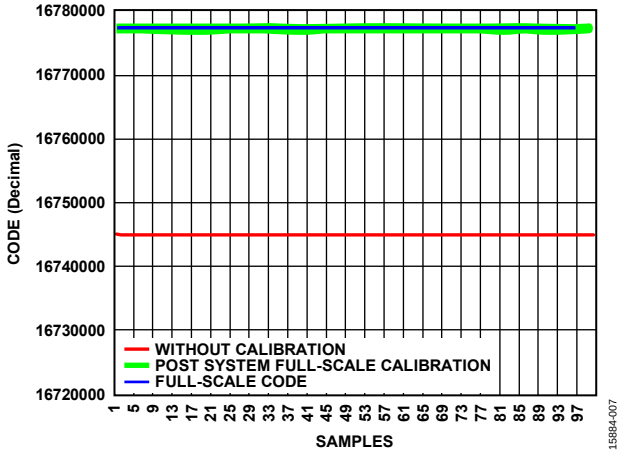

Figure 7. EVAL-AD7124-4SDZ Without Calibration vs. Post System Full-Scale Calibration

Following a system full-scale calibration, the gain register updates 0x55A2D3. Using the same input voltage, the ADC average result was 0xFFFF9D (16,777,118). Therefore, the resulting gain error was reduced to the following:

$$((16777216 - 16777118) \div 16777216) \times 100 = 0.0006\%$$

FACTORY CALIBRATION

The default value of the offset register is 0x800000 and the nominal value of the gain register is 0x5XXXXX. The gain error is factory calibrated at a gain of 1. Therefore, the AD7124-4, AD7124-8, AD7172-2, AD7172-4, AD7173-8, AD7175-2, AD7175-8, AD7176-2, and AD7177-2 contain a default gain coefficient, which varies from device to device. The AD7124-4 and AD7124-8 do not support the internal full-scale calibration at a gain of 1.

SYSTEM CALIBRATION VOLTAGES

Note that the AD7124-4, AD7124-8, AD7172-2, AD7172-4, AD7173-8, AD7175-2, AD7175-8, AD7176-2, and AD7177-2 have an input range from 0.8 × V_{REF} ÷ gain to 2.1 × V_{REF} ÷ gain (gain = 1 to 128 for the AD7124-4 and AD7124-8; gain = 1 only for the AD7172-2, AD7172-4, AD7173-8, AD7175-2, AD7175-8, AD7176-2, and AD7177-2). Therefore, the user can tune the input range. This is useful because some designs may not use the complete ADC input range. For example, a sensor may generate a signal, which is only 95% of the allowed input range for the ADC. In this case, an input signal that is 0.95 × V_{REF} ÷ gain can be applied to the ADC, and the ADC is capable of performing a system full-scale calibration with this magnitude of signal.

PERFORMING CALIBRATIONS

Calibrations are initiated by writing the relevant value to the ADC mode bits in Register ADC_CONTROL of the AD7124-4 and AD7124-8 or Register ADC mode of the AD7172-2, AD7172-4, AD7173-8, AD7175-2, AD7175-8, AD7176-2, and AD7177-2. When a calibration initiates, the DOUT/$\overline{RDY}$ pin and the $\overline{RDY}$ bit in the status register goes high. When the required calibration completes, the contents of the corresponding offset or gain register updates, the $\overline{RDY}$ bit in the status register is low, and the DOUT/$\overline{RDY}$ pin returns to low (if $\overline{CS}$ is low). Therefore, the user does not have to monitor the calibration time because the $\overline{RDY}$ falling edge or the $\overline{RDY}$ status bit indicates the end of the calibration.

The order of the calibrations is dependent on the ADC. For the AD7172-2, AD7172-4, AD7173-8, AD7175-2, AD7175-8, AD7176-2, and AD7177-2, it is recommended to perform zero-scale calibrations before full-scale calibrations when both offset and gain calibrations are being performed.

For the AD7124-4 and AD7124-8, an internal full-scale calibration can only be performed when the offset register is at its default value of 0x800000. Therefore, when performing both internal zero-scale and internal full-scale calibrations, the following routine is recommended:

- Reset the offset register to 0x800000.
- Perform the internal full-scale calibration.
- Perform the internal zero-scale calibration.

For system calibrations, the system zero-scale calibration must be performed before the system full-scale calibration.

All calibrations require a time equal to the settling time of the selected filter and output data rate to be completed, except for the internal full-scale calibration, which requires a time equal to one settling period for a gain of 1 and a time of four settling periods for gains greater than 1.

Calibrations are supported in low or mid power mode only on the AD7124-4 and AD7124-8.

Note that both gain error and offset error calibrations can be performed at any gain or output data rate. Calibrations are conversions with a known analog input. However, it is recommended to calibrate at lower output data rate because a lower output data rate has lower noise and thus the AD7124-4, AD7124-8, AD7172-2, AD7172-4, AD7173-8, AD7175-2, AD7175-8, AD7176-2, and AD7177-2 performance is at its best. The calibration coefficient obtained then is used in any output data rate.

USING THE CALIBRATION COEFFICIENTS

The ADC output coding represents an analog input voltage for the AD7124-4, AD7124-8, AD7172-2, AD7172-4, AD7173-8; AD7175-2, AD7175-8, AD7176-2, and AD7177-2. An offset binary code is used for both families.

Therefore, in unipolar operation, the ideal relationship is

$$Code = (2^N \times V_{IN} \times Gain) \div V_{REF}$$

In bipolar operation, the equation becomes

$$Code = 2^{N-1} \times [(A_{IN} \times Gain \div V_{REF}) + 1]$$

where:
N = 24, number of bits (resolution).
V_{IN} is the analog input voltage.
V_{REF} is the reference voltage.
Gain is the gain setting (1 to 128 for the AD7124-4 and AD7124-8, 1 only for the AD7172-2, AD7172-4, AD7173-8, AD7175-2, AD7175-8, AD7176-2, and AD7177-2).

In practice, the ADC output coding is slightly different because the offset and gain correction must be included in the ADC conversion result.

The relationship for unipolar mode is

$$Data = \left\{\frac{0.75\times V_{IN}}{V_{REF}}\times 2^{23} - (Offset - 0x800000)\right\}\times\frac{Gain}{0x400000}\times 2$$

The relationship for bipolar mode is

$$Data = \left\{\frac{0.75\times V_{IN}}{V_{REF}}\times 2^{23} - (Offset - 0x800000)\right\}\times\frac{Gain}{0x400000} + 0x800000$$

where:
Offset is the offset coefficient.
Gain is the gain coefficient.

These equations use the offset and gain coefficients to scale the ADC digital output.

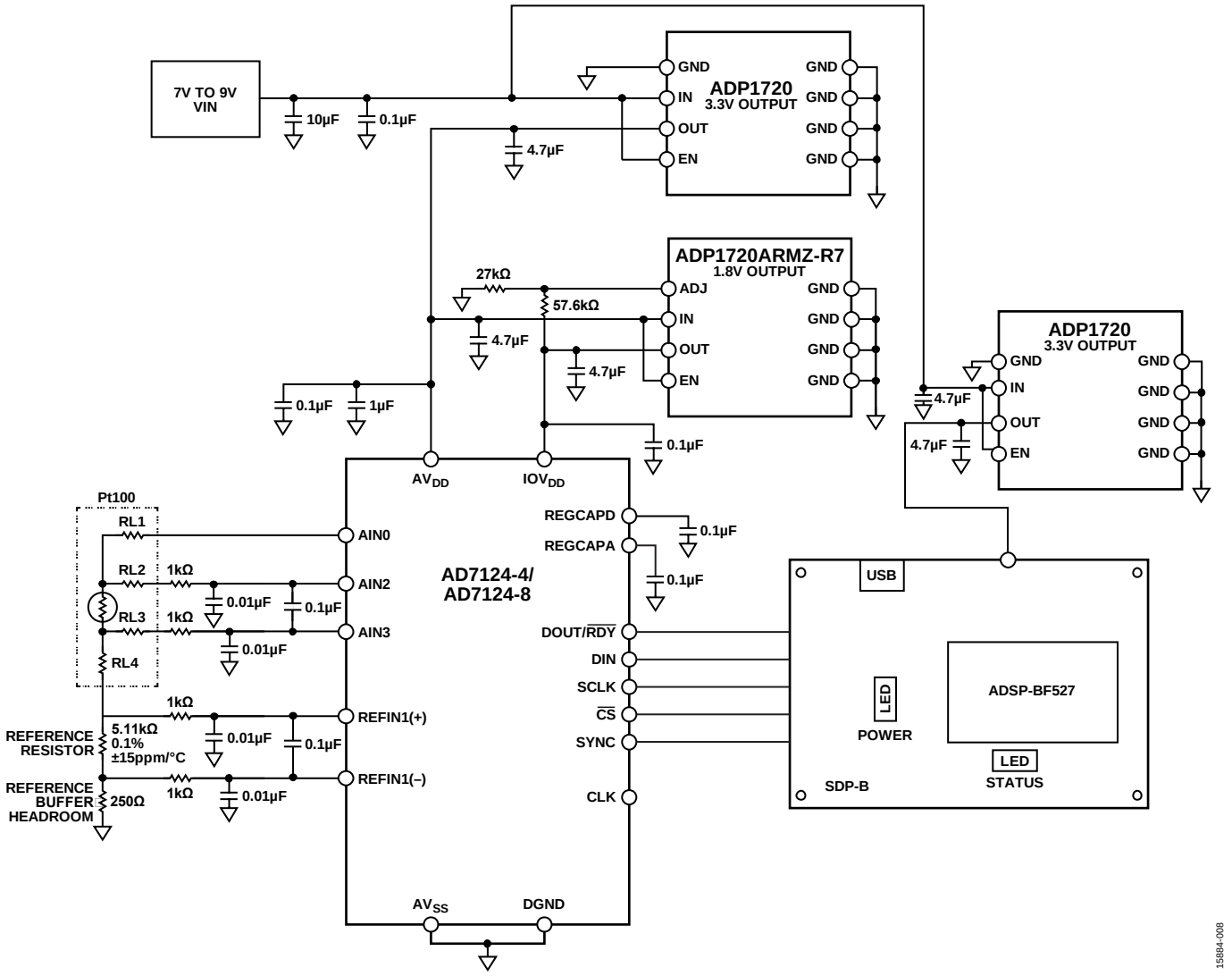

Figure 8. CN-0381 Schematic Diagram

Note that the sampled analog input is reduced by 25% within the ADC. This scaling is performed so that a full-scale signal is never applied to the Σ-Δ modulator and, therefore, ensures that the modulator is never saturated. It is important to note that the attenuation is corrected by the factor of gain ÷ 0x400000 in the overall calculation.

The CN-0381 highlights the improvements in accuracy when gain and offset calibrations are performed on the AD7124-8.

The CN-0381 schematic is shown in Figure 8. This system uses the AD7124-8 with a Pt100 temperature sensor resistance temperature detector (RTD) interfaced to the ADC. The linearization of the sensor is performed on the ADC conversions.

When the RTD temperature is swept over a temperature range of −50°C to +150°C with the AD7124-8 at ambient temperature, the accuracy of the results are outside the expected range when using the default gain and offset coefficients.

However, a one time internal offset and gain calibration at 25°C improves the accuracy and the system results are well within the expected profile of the Pt100 RTD. Figure 9 shows the result of a Pt100 RTD sensor using the AD7124-8.

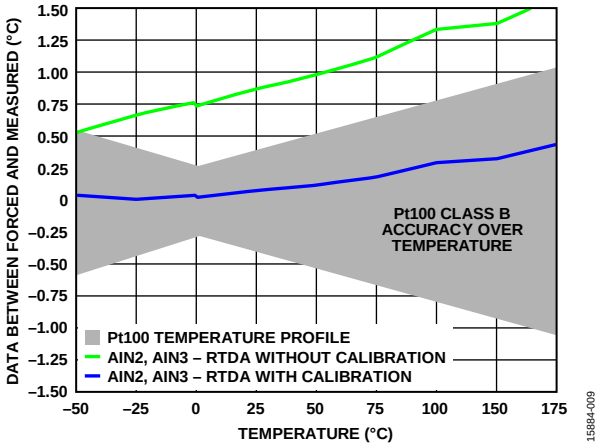

Figure 9. AD7124-8 With Calibration vs. Without Calibration vs. Pt100 Profile Delta Between Forced and Measured and Pt100 Class B Accuracy Over Temperature vs. Temperature

WHEN TO PERFORM CALIBRATIONS

Calibrations must be performed after power-up. Therefore, as part of the initialization routine, each channel in use must be selected, and the channel must be configured. For example, select the reference source and set the gain. An offset and gain calibration must then be performed on the channel. Only one channel can be enabled when calibrations are being performed. If multiple channels are enabled, the ADC only calibrates the first channel in the sequence. The channel must be recalibrated if the gain is changed to another gain value.

Some users prefer to perform periodic calibrations to minimize the offset and gain error drift. The frequency at which these additional calibrations are performed depends on the rate of temperature change of the application of the user.

However, the AD7124-4, AD7124-8, AD7172-2, AD7172-4, AD7173-8, AD7175-2, AD7175-8, AD7176-2, and AD7177-2 have low offset drift and gain drift; therefore, for many applications, a one time calibration after power up is sufficient.

Internal calibration is usually performed to adjust the offset error and gain error because of the ADC drift performance. The CN-0381 shows how to use the internal calibration to fine tune the offset and gain error of the AD7124-8 when it is exposed across temperature ranges.

Perform system calibrations to compensate for the offset and gain error contribution by the front end or external circuitry of the ADC system. The system calibration is best applied on a weigh scale application because the load cell accuracy drifts. To fine tune the accuracy caused by the drift, the user must perform system calibration.

CONCLUSION

Gain error and offset error calibrations, as well as internal and system level calibration are available on the Σ-Δ ADCs from Analog Devices. Having these calibrations on-chip improve the overall accuracy available from a system and remove any requirements from the user to implement calibration of the samples, which simplifies the overall design and saves time.

REFERENCES

Kester, Walt. 2005. *The Data Conversion Handbook*. Analog Devices. Chapter 3 and Chapter 7.