# AN-1084
## APPLICATION NOTE

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# Channel Switching: AD7190, AD7192, AD7193, AD7194, AD7195
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## INTRODUCTION

$\Sigma$-$\Delta$ ADCs are generally specified in terms of output data rate. The output data rate is the rate at which conversions are performed when a single channel is selected and the ADC is continuously converting. In a multichannel application such as a data acquisition system, conversions from several channels are read; that is, each channel is selected in turn and a conversion is performed for that channel. In such an application, the rate at which conversions are performed can be different from a single channel system. This application note describes the switching procedure used by the AD7190, AD7192, AD7193, AD7194, and AD7195 parts (hereafter referred to as AD719x).

## MULTICHANNEL SYSTEM

In applications such as PLC systems, several input channels are required to process the multitude of signals or outputs from sensors. With its PGA and wide range of programmable output data rates, the AD719x can be used to convert signals of different amplitudes and at different output data rates.

The application generally requires a certain throughput, that is, a given number of channels need to be read within a given period of time. The throughput achieved is dependent on the number of channels to be read and the time taken by the ADC to convert each channel. The ADCs referred to in this application note have several modes of operation:

- $Sinc^4$ filter or $Sinc^3$ filter
- Chop enabled/disabled
- Zero latency
- Single conversion mode
- Automatic channel sequencing

The output data rates allowed and/or the settling time (the time taken to generate the first conversion after a channel change) is different for each mode of operation. Therefore, the throughput also depends on the operating mode.

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## REVISION HISTORY

**9/10—Revision 0: Initial Version**

## SINC⁴ FILTER (CHOP DISABLED)

When the sinc[4] filter is selected and chop is disabled, the output data rate when continuously converting on a single channel ($f_{ADC}$) is equal to

$$f_{ADC} = f_{CLK}/(1024 \times FS[9:0])$$

where $f_{CLK}$ is the master clock frequency and $FS[9:0]$ is the filter word loaded into the mode register. The time required to generate the first conversion after a channel change is approximately equal to

$$t_{SETTLE} = 4/(f_{CLK}/(1024 \times FS[9:0]))$$

$$= 4096 \times FS[9:0]/f_{CLK}$$

This equation is sufficiently accurate when low output data rates are used. The complete equation for settling time equals

$$t_{SETTLE} = 4/(f_{CLK}/(1024 \times FS[9:0])) + 507/f_{CLK}$$

$$= (4096 \times FS[9:0] + 507)/f_{CLK}$$

Therefore, when the channel is changed, the settling time is required to generate the first conversion. Subsequent conversions on this channel occur at the programmed output data rate ($f_{ADC}$). In an application where several channels are used and one conversion is read from each channel, the settling time is required for every conversion. Therefore, the number of channels read per second equals

$$Throughput = f_{CLK}/(4 \times 1024 \times FS[9:0] + 507)$$

$$= f_{CLK}/(4096 \times FS[9:0] + 507)$$

When a conversion is complete on a channel, a write to the configuration register is required to select the next channel to be converted. This SPI communication reduces the throughput. Table 1 gives a summary of the output data rate, settling time, and throughput for some sample FS[9:0] values (ignoring the time required for the SPI communications).

**Table 1. Output Data Rate, Settling Time, and Throughput for Sinc⁴ Filter, Chop Disabled**

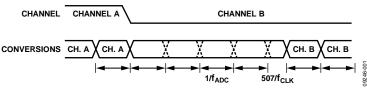| FS[9:0] | $f_{ADC}$ (Hz) | $t_{SETTLE}$ (ms) | Channels per Second |
|---------|---------|---------|---------------------|
| 96 | 50 | 80.1 | 12 |
| 80 | 60 | 66.8 | 14 |
| 1 | 4800 | 0.936 | 1067 |



Figure 1. Channel Switching (Sinc⁴ Filter, Chop Disabled)

## SINC³ FILTER (CHOP DISABLED)

The digital filter can be changed to a sinc³ filter by setting the SINC3 bit in the mode register. Choosing the sinc³ filter does not affect the output data rate. Therefore, the output data rate when continuously converting on a single channel is again

$$f_{ADC} = f_{CLK}/(1024 \times FS[9:0])$$

However, the time required to generate a valid conversion after a channel change is reduced.

$$t_{SETTLE} = 3/(f_{CLK}/(1024 \times FS[9:0])) + 507/f_{CLK}$$
$$= (3072 \times FS[9:0] + 507)/f_{CLK}$$

At low output data rates, this equation can be approximated to

$$t_{SETTLE} = 3072 \times FS[9:0]/f_{CLK}$$

In a multichannel application where one conversion is read per channel, the throughput of the system is

$$Throughput = f_{CLK}/(3 \times 1024 \times FS[9:0] + 507)$$
$$= f_{CLK}/(3072 \times FS[9:0] + 507)$$

Table 2 gives a summary of the output data rate, settling time, and throughput for some sample FS[9:0] values. In practice, the throughput becomes lower as each channel is selected manually.

**Table 2. Output Data Rate, Settling Time, and Throughput for Sinc³ Filter, Chop Disabled**

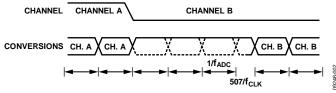| FS[9:0] | $f_{ADC}$ (Hz) | $t_{SETTLE}$ (ms) | Channels per Second |
|---------|--------|----------|---------------------|
| 96 | 50 | 60.1 | 16 |
| 80 | 60 | 50.1 | 19 |
| 1 | 4800 | 0.728 | 1373 |



*Figure 2. Channel Switching (Sinc³ Filter, Chop Disabled)*

## CHOPPING ENABLED

### Sinc⁴ Filter

With the sinc⁴ filter selected and chop enabled, the output data rate when continuously converting on a single channel, $f_{ADC}$, is

$$f_{ADC} = f_{CLK}/(1024 \times FS[9:0] \times 4 + 16)$$

$$= f_{CLK}/(4096 \times FS[9:0] + 16)$$

The time required to generate a conversion following a channel change (settling time) equals

$$t_{SETTLE} = 2/(f_{CLK}/(1024 \times FS[9:0] \times 4 + 16)) + 491/f_{CLK}$$

$$= (8192 \times FS[9:0] + 523)/f_{CLK}$$

For low output data rates, these equations can be approximated to

$$f_{ADC} = f_{CLK}/(4096 \times FS[9:0])$$

$$t_{SETTLE} = 8192 \times FS[9:0]/f_{CLK}$$

When several channels are used in an application with one conversion being read per channel, the throughput is

$$f_{CLK}/(2 \times (1024 \times FS[9:0] \times 4 + 16) + 491)$$

$$= f_{CLK}/(8192 \times FS[9:0] + 523)$$

A write to the configuration register to select each channel reduces the throughput further.

Table 3 gives a summary of the output data rate, settling time, and throughput for some sample FS[9:0] values.

**Table 3. Output Data Rate, Settling Time, and Throughput for Sinc⁴ Filter, Chop Enabled**

| FS[9:0] | $f_{ADC}$ (Hz) | $t_{SETTLE}$ (ms) | Channels per Second |
|---------|---------|----------|---------------------|
| 96 | 12.49 | 160.1 | 6 |
| 80 | 14.99 | 133.4 | 7 |
| 1 | 1195.3 | 1.773 | 563 |

### Sinc³ Filter

When the sinc³ filter is selected and chop is enabled, the output data rate when continuously converting on a single channel is

$$f_{ADC} = f_{CLK}/(1024 \times FS[9:0] \times 3 + 16)$$

$$= f_{CLK}/(3072 \times FS[9:0] + 16)$$

The settling time is

$$t_{SETTLE} = 2/(f_{CLK}/(1024 \times FS[9:0] \times 3 + 16)) + 491/f_{CLK}$$

$$= (6144 \times FS[9:0] + 523)/f_{CLK}$$

For low output data rates, these equations can be approximated to

$$f_{ADC} = f_{CLK}/(3072 \times FS[9:0])$$

$$t_{SETTLE} = 6144 \times FS[9:0]/f_{CLK}$$

Therefore, the first conversion after a channel change requires a time of $t_{SETTLE}$, and subsequent conversions on this channel occurs at $1/f_{ADC}$.

With chop enabled and several channels being used in a system, the throughput is

$$f_{CLK}/(2 \times (1024 \times FS[9:0] \times 3 + 16) + 491)$$

$$= f_{CLK}/(6144 \times FS[9:0] + 523)$$

The SPI communication required to select each channel reduces the throughput further.

Table 4 gives a summary of the output data rate, settling time, and throughput for some sample FS[9:0] values.

**Table 4. Output Data Rate, Settling Time, and Throughput for Sinc3 Filter, Chop Enabled**

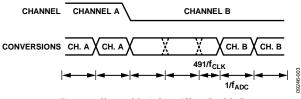| FS[9:0] | $f_{ADC}$ (Hz) | $t_{SETTLE}$ (ms) | Channels Per Second |
|---------|---------|----------|---------------------|
| 96 | 16.67 | 120.1 | 8 |
| 80 | 19.99 | 100.1 | 9 |
| 1 | 1591.7 | 1.356 | 737 |



*Figure 3. Channel Switching (Chop Enabled)*

## ZERO LATENCY

These $\Sigma$-$\Delta$ ADCs can also operate in zero latency mode. This mode is enabled by setting Bit MR11 (Bit Single) in the mode register to 1. When this mode is enabled, the conversion time when continuously converting on a single channel approximately equals the settling time. The benefit of this mode is that a similar period of time elapses between all conversions irrespective of whether the conversions occur on one channel or whether several channels are used.

When switching channels, there is an extra delay of $491/f_{CLK}$ or $507/f_{CLK}$ in the first conversion. At low output data rates, this extra delay has little impact on the value of the settling time. However, at high output data rates, the delay should be considered. Table 5 summarizes the output data rate when continuously converting on a single channel and when switching between channels for the different filter configurations.

When switching between channels, the AD719x allows the complete settling time to generate the first conversion after the channel change. Therefore, the ADC automatically operates in zero latency mode when several channels are enabled—setting the single bit has no benefits.
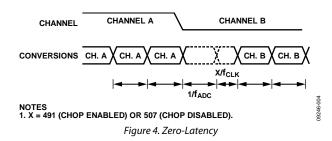
For example, if the sinc[4] filter is selected, chop is disabled and zero latency is enabled, the output data rate equals 12.5 Hz when FS = 96. Therefore, the conversion time is 80 ms. The settling time is 80.1 ms. Up to 12 channels can be sampled per second when FS = 96. Therefore, the throughput is the same as for the sinc[4], chop disabled, zero latency disabled configuration.

## SINGLE CONVERSION MODE

These ADCs also have a single conversion mode whereby the device performs a conversion and then goes into power-down mode. This mode is not relevant for applications such as PLC where the ADC is continuously converting. However, if an application uses several input channels and conversions are read back periodically from the channels, then this mode is useful.

The user can begin a conversion by writing to the MD2, MD1, and MD0 bits in the mode register. When these bits are set appropriately, the ADC is powered up. The internal clock, if used, requires some time to power up. The complete settling time is then required to generate the conversion. The ADC places this conversion in the data register, takes DOUT/$\overline{RDY}$ low, and then returns to power-down mode. The throughput in this case is dependent on the number of channels being used, the output data rate selected, and the time required to communicate with the ADC.

**Table 5. Output Data Rate and Settling Time (Zero Latency)**

| Filter | Chop | $f_{ADC}$ | $t_{SETTLE}$ |
|---|---|---|---|
| Sinc[4] | No | $f_{CLK}/(4096 \times FS[9:0])$ | $(4096 \times FS[9:0] + 507)/f_{CLK}$ |
| Sinc[3] | No | $f_{CLK}/(3072 \times FS[9:0])$ | $(3072 \times FS[9:0] + 507)/f_{CLK}$ |
| Sinc[4] | Yes | $f_{CLK}/(8192 \times FS[9:0] + 32)$ | $(8192 \times FS[9:0] + 523)/f_{CLK}$ |
| Sinc[3] | Yes | $f_{CLK}/(6144 \times FS[9:0] + 32)$ | $(6144 \times FS[9:0] + 523)/f_{CLK}$ |



NOTES
1. X = 491 (CHOP ENABLED) OR 507 (CHOP DISABLED).

*Figure 4. Zero-Latency*

## CHANNEL SEQUENCER

This section is not relevant to the AD7194 because this part does not have a sequencer.

The value of the FS[9:0] bits and the operating mode used are the main factors that affect the throughput rate. However, in all the modes described thus far, the user must write to the configuration register between conversions to select the next channel for conversion. In single conversion mode, the user must write to the mode register in addition to the configuration register to initiate another single conversion.

These ADCs have an on-chip channel sequencer that simplifies the use of the parts in multichannel applications. All channels being used in the application are enabled. The sequencer then steps through the enabled channels and performs a conversion on each channel. The channel sequencer can be used only if all channels use the same PGA gain and output data rate. If each channel has a different PGA gain, for example, then the sequencer must be disabled.

The channels to be used are enabled by setting Bit CH0 to Bit CH7 in the configuration register. When the ADC converts, it automatically selects each of the enabled channels in turn and performs a conversion on each channel. The DOUT/$\overline{\text{RDY}}$ pin goes low each time a conversion is available from a channel. When Bit DAT_STA in the mode register is set to 1, the contents of the status register are appended to each conversion. The status register indicates which channel corresponds to the conversions. It also indicates whether the conversion is valid via the ERR bit.

With the channel sequencer enabled, the settling time per channel depends on the filter configuration used. However, the settling time is less when the sequencer is enabled compared with the previous configurations discussed where the sequencer was disabled. With the sequencer disabled, there is a delay of $491/f_{CLK}$ or $507/f_{CLK}$ in the settling time when the channel is changed. With the sequencer enabled, this delay only exists in the first channel converted. The settling time of the subsequent channels is reduced. Table 6 summarizes the settling time for each channel when the sequencer is enabled. The first conversion has an extra delay of $491/f_{CLK}$.
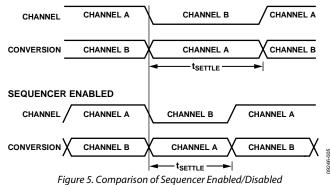
**Table 6. Settling Time (Sequencer Enabled)**

| Filter | Chop | $t_{SETTLE}$ |
|---|---|---|
| Sinc$^4$ | No | $(4096 \times FS[9:0] + 16)/f_{CLK}$ |
| Sinc$^3$ | No | $(3072 \times FS[9:0] + 16)/f_{CLK}$ |
| Sinc$^4$ | Yes | $(8192 \times FS[9:0] + 32)/f_{CLK}$ |
| Sinc$^3$ | Yes | $(6144 \times FS[9:0] + 32)/f_{CLK}$ |

**Table 7. Throughput (Sequencer Disabled/Enabled)**

| | Channels per Second (Sinc$^4$, Chop Disabled) | |
|---|---|---|
| **FS[9:0]** | **Sequencer Disabled** | **Sequencer Enabled** |
| 96 | 12 | 12 |
| 80 | 14 | 14 |
| 1 | 1067 | 1195 |

Table 7 compares the number of channels that can be converted per second for the sinc$^4$ filter with chop disabled when the sequencer is enabled and disabled. This comparison does not include the time required to interface with the ADC to select the next channel when the sequencer is disabled. At low output data rates, the channel count is the same. However, at high output data rates, the sequencer increases the channel count significantly.



Figure 5. Comparison of Sequencer Enabled/Disabled

## SUMMARY

The rate at which conversions are available is different between a single-channel application and a multichannel application. In a multichannel system, the settling time is required to generate the first conversion each time that a channel is selected. The settling time, in turn, is dependent on the mode in which the device is configured, for example, chop enabled/disabled and filter order. Therefore, the user needs to calculate the settling time required for the given configuration along with the number of channels being used in an application to determine the throughput of the device in a multichannel system.

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