AN-0979
APPLICATION NOTE

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Digital Filtering Options: AD7190, AD7192

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INTRODUCTION

The sigma-delta (Σ-Δ) ADCs listed feature a user-selectable sinc^3 and sinc^4 digital filter. This application note compares sinc^3 and sinc^4 filters, identifying the benefits of each type and the implications of using one type over the other.

SINC FILTERS

Sigma-delta ADCs consist of a sigma-delta modulator followed by a digital filter. The modulator continuously samples the analog input at a high sampling rate and outputs a 1-bit data stream. The quantity of ones in the bit stream corresponds to the analog input voltage. The digital filter then processes the bit stream and performs decimation to generate the 24-bit conversion.

Sinc filters are used as the digital filter on the products being discussed. The output data rate, f_{ADC}, which is the rate at which the ADC continuously converts on a single channel, is equal to

$$f_{ADC} = f_{CLK}/(1024 \times FS[9:0])$$

where:
f_{CLK} is the master clock (4.92 MHz nominal).
FS[9:0] is the decimal equivalent of the code in Bit FS9 to Bit FS0 of the mode register.

This is the equation for the output data rate when chop is disabled. Note that chop is assumed to be disabled in this application note, unless otherwise stated.

Figure 1 shows the frequency response of a sinc^3 filter for an output data rate of 10 Hz while Figure 2 shows the frequency response for a sinc^4 filter for a 10 Hz output data rate. The notch locations are determined by the output data rate. The width of the notches is dependent on the filter order. As the order is increased, the notches get wider. Therefore, the output data rate determines the location of the notches, but the filter order determines the rejection that can be obtained around the notches. As the filter order increases, the roll-off and stop-band attenuation are also affected along with settling time and noise.

50 Hz/60 Hz REJECTION

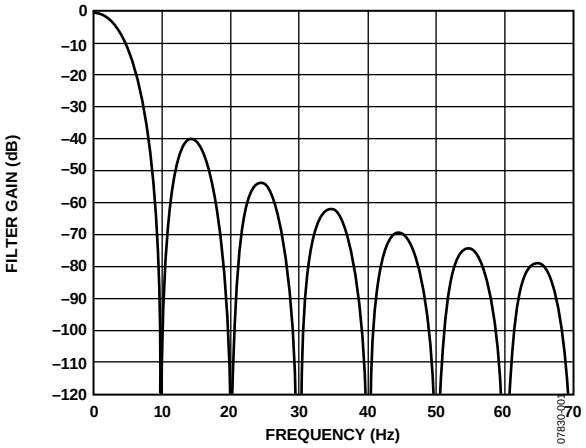

Figure 1. Sinc^3 Filter Response (f_{ADC} = 10 Hz)

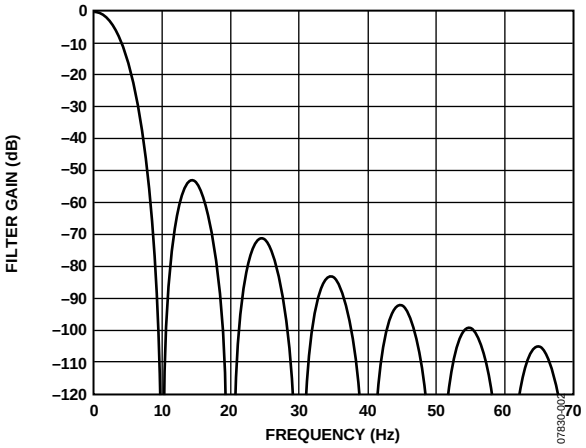

Figure 2. Sinc^4 Filter Response (f_{ADC} = 10 Hz)

Figure 1 shows the frequency response of a sinc^3 filter for an output data rate of 10 Hz. Notches are present at the output data rate and at multiples of the output data rate. Therefore, a notch is located at 10 Hz, 20 Hz, 30 Hz, and so on. This feature can be used to reject interference from the mains power supply, which is a key requirement in many applications. In some regions of the world, 50 Hz needs to be rejected while 60 Hz needs to be rejected in other regions. The notches of the sinc filter can be used to reject this interference. When the output data rate is 10 Hz, notches are located at 50 Hz and 60 Hz, therefore simultaneous 50 Hz and 60 Hz rejection is provided. This feature is required if the end system is to be sold in many different countries around the world.

From Figure 1, the rejection is in excess of 100 dB at 50 Hz ± 1 Hz and 60 Hz ± 1 Hz when the output data rate is equal to 10 Hz. This assumes that the system clock has low jitter and drift, for example, if a crystal is used to provide the system clock.

Figure 2 shows the frequency response of a sinc^4 filter for an output data rate of 10 Hz. As with the sinc^3 filter, the notches are located at 10 Hz and multiples of 10 Hz. However, due to the wider notches, the rejection at 50 Hz ± 1 Hz and 60 Hz ± 1 Hz is in excess of 120 dB.

If only 50 Hz or 60 Hz rejection is required, then the output data rate can be increased, thus, for 50 Hz only rejection, the maximum output data rate that can be used is 50 Hz. The first notch of the sinc filter is now located at 50 Hz. Similarly, an output data rate of 60 Hz places the first notch at 60 Hz.

When ADCs are operated with an output data rate of 50 Hz, there is a on-chip feature that also allows placement of a notch at 60 Hz also. When the REJ60 bit in the mode register is set to 1, a notch is placed at 60 Hz when the output data rate is 50 Hz. Therefore, the output data rate can be increased from 10 Hz to 50 Hz and simultaneous 50 Hz and 60 Hz rejection is still obtained. Figure 3 shows the filter response when the output data rate is 50 Hz and the REJ60 bit is set to 1. The worst-case rejection at 50 Hz ± 1 Hz and 60 Hz ± 1 Hz is 67 dB. When the sinc^4 filter is used (see Figure 4), the worst-case rejection at 50 Hz ± 1 Hz and 60 Hz ± 1 Hz is 82 dB.

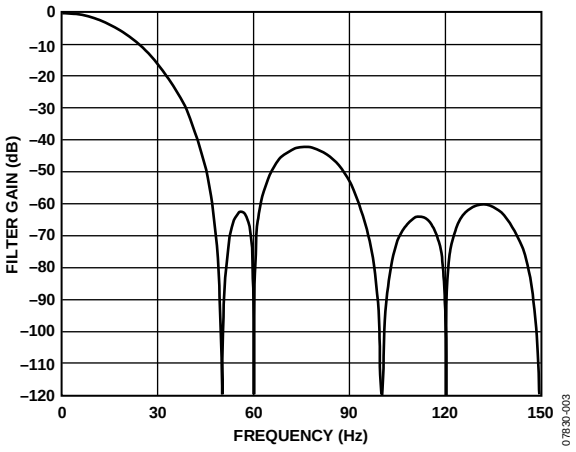

Figure 3. Sinc^3 Filter Response (f_{ADC} = 50 Hz, REJ60 = 1)

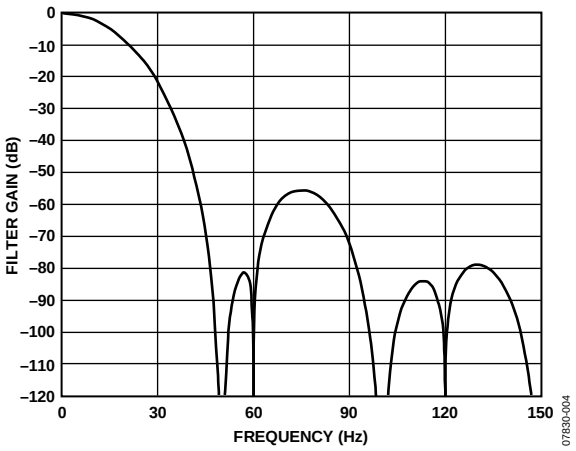

Figure 4. Sinc^4 Filter Response (f_{ADC} = 50 Hz, REJ60 = 1)

STOP-BAND ATTENUATION

The change in the filter response due to the order of the filter alters the stop-band attenuation and filter roll-off in addition to the notch width. Stop-band attenuation refers to the rejection provided by the digital filter for frequencies above the first notch (see Figure 5). The stop-band attenuation is improved as the filter order is increased. The stop-band attenuation is 40 dB for the sinc^3 filter and 53 dB for the sinc^4 filter.

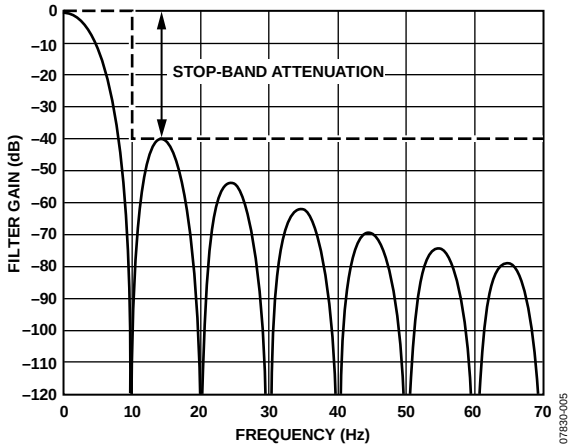

Figure 5. Stop-Band Attenuation

NOISE/RESOLUTION

These devices are specified to operate with a programmable output data rate from 4.7 Hz to 4.8 kHz. Along with the order of the filter, the output data rate affects the noise and, therefore, the resolution. At low output data rates, the rms noise is similar for the sinc^3 and sinc^4 filters (see Figure 6). However, at the higher output data rates (1 kHz or higher), the sinc^4 filter delivers superior rms noise. Figure 7 shows the noise-free (peak-to-peak) resolution at the different output data rates.

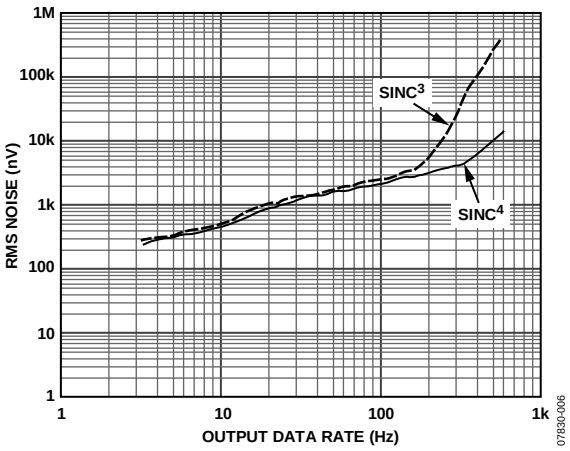

Figure 6. RMS Noise vs. Output Data Rate (Gain = 1, V_{RFE} = 5 V)

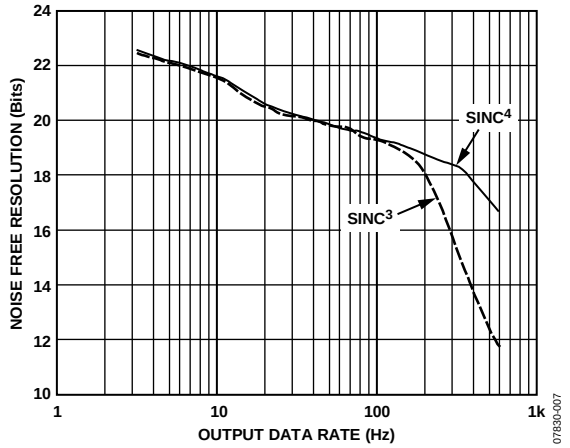

Figure 7. Noise-Free Resolution vs. Output Data Rate (Gain = 1, V_{REF} = 5 V)

SETTLING TIME

For any multichannel application, the settling time is another parameter to consider. When converting continuously on a single channel, valid conversions are output at the programmed output data rate when the analog input signal is continuous. However, if a configuration change occurs, such as changing channel, gain or output data rate, the first conversion after the configuration change requires additional time. Figure 8 shows the effect of a channel change when the ADC is operating with an output data rate of 10 Hz. When the channel change occurs, the modulator and filter are reset. The ADC then begins sampling the new analog input. The filter must be allowed to completely settle to generate the first valid conversion. With a sinc^3 filter, the settling time, t_{SETTLE}, is

$$t_{SETTLE} = 3/f_{ADC}$$

For the sinc^4 filter, the settling time is

$$t_{SETTLE} = 4/f_{ADC}$$

If the ADC is converting on a single channel but a step change occurs in the analog input signal, the ADC also needs to settle to the new analog input. If the step change is synchronous with the conversion process, then the settling time must elapse before a valid conversion is available. The ADC does not detect step changes in the analog input. Therefore, it continues to output conversions at the programmed output data rate. However, the intermediate conversions are not accurate—they reflect the change in the analog input, but the accuracy is reduced.

If the step change occurs in the middle of a conversion, then the current conversion must be completed and the ADC must then allow the appropriate settling time to generate a valid conversion. For a sinc^3 filter, the overall time is increased to $4/f_{ADC}$ while the time required to generate a valid conversion with the sinc^4 filter is $5/f_{ADC}$.

In summary, for the same output data rate, the sinc^3 filter settles faster than the sinc^4 filter. While a sinc^4 filter gives better rms noise and better noise-free resolution than the sinc^3 filter for the same output data rate, it has a longer settling time.

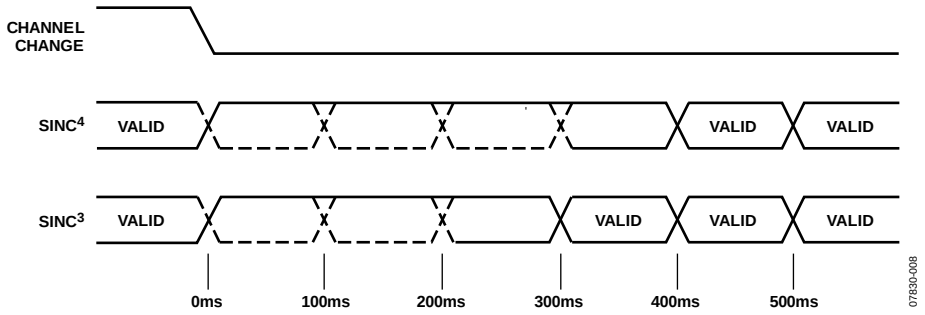

Figure 8. Settling Time (Synchronous Step Change)

CONCLUSION

The order of the sinc filter affects the performance that is achievable from the Σ-Δ ADC. Higher order sinc filters provide better rejection at the notches and offer better stop-band attenuation. They also give superior noise performance and resolution at high output data rates. The disadvantage is the increase in the settling time. A sinc^4 filter takes one conversion more than a sinc^3 filter to settle. Therefore, the selection of the filter depends on the combination of the 50 Hz and 60 Hz rejection required, the output data rate being used in the application and the required noise performance and resolution. Table 1 lists a number of the key performance parameters for the listed Σ-Δ ADCs which are affected by the digital filter selection.

Table 1. Comparison of Some Key Performance Parameters for the Sinc^3 and Sinc^4 Filters

Parameter	Sinc^3	Sinc^4
RMS Noise @ f_{ADC} = 10 Hz (Gain = 1)	350 nV	330 nV
Noise-Free Resolution @ f_{ADC} = 10 Hz (Gain = 1)	22	22
RMS Noise @ f_{ADC} = 4800 Hz (Gain = 1)	442 μV	14.3 μV
Noise-Free Resolution @ f_{ADC} = 4800 Hz (Gain = 1)	11.5	16.5
50 ± 1 Hz and 60 ± 1 Hz Rejection (f_{ADC} = 10 Hz)	−100 dB	−120 dB
Rejection at 50 ± 1 Hz and 60 Hz ± 1 Hz (f_{ADC} = 50 Hz, REJ60 = 1)	67 dB	82 dB
Stop-Band Attenuation	40 dB	53 dB
Settling Time	3/f_{ADC}	4/f_{ADC}