IBIS Quality Checklist

Part Name: **ad74413r**
IBIS File Name: **ad74413r_64l_lfcsp.ibs**
Top Level Schematic Location
Project Name: **ad74412**
Library Name: **ad74412**
Cell Name: **ad74412_top**
IBIS Model Maker: **Seth Manay (*seth.manay@analog.com*)**

✓/✗	Description	Remarks
✓	Does the IBIS File pass the IBIS syntax checker? (Note: Some models generate warnings for non-monotonicities that are actually part of the characteristics of the device. Other non-monotonicities are so small as to be irrelevant.)	
✓	Has the model maker performed a visual inspection of IV and VT curves to screen for non-monotonicity, discontinuities, and other obvious errors?	
✓	Has the model maker tested the IBIS File using a behavioral simulator?	
✓	Do MIN and MAX data exist for all keywords and sub-parameters?	
✓	Do the keywords Cref, Rref, Vref, and Vmeas match the values specified in the component datasheet for all output and bidirectional models?	
✓	Does the pin table match the component datasheet?	
✓	Do the keywords Vinl and Vinh match the values specified in the component datasheet?	
✓	Do the voltage and temperature range match the values specified in the datasheet?	
✓	Has the model maker verified the accuracy of the C_comp subparameter?	
✓	Has the model maker verified the accuracy of the R_pkg, L_pkg, and C_pkg subparameters?	
✓	For CMOS logic, do all MAX data represent maximum voltage, minimum temperature, and fast process?	
✓	For CMOS logic, do all MIN data represent minimum voltage, maximum temperature, and slow process?	
✗	For bipolar logic, do all MAX data represent maximum voltage, maximum temperature, and fast process?	N/A
✗	For bipolar logic, do all MIN data represent minimum voltage, minimum temperature, and slow process?	N/A
✓	Do the keywords dV/dt_r and dV/dt_f contain the correct 20%-80% edge rate data measured using a 50Ω load as specified in IBIS?	
✓	Do the rise time (t_R) and fall time (t_F) satisfy the specified value in the datasheet?	
✗	If the I/O buffer employs dynamic clamping, does the IBIS File contain the appropriate keywords and subparameters? (if applicable)	N/A
✗	If the I/O buffer employs a multi-stage driver, does the IBIS File contain the appropriate keywords and subparameters? (if applicable)	N/A
✗	If the I/O buffer design employs dynamic edge rate control, dynamic impedance control, or any form of feedback, has the modeling engineer assessed the impact of this circuitry on behavioral model accuracy? (if applicable)	N/A
✓	Has the model maker retained the necessary comments in the IBIS File?	