ANALOG DEVICES

AN-225
APPLICATION NOTE

ONE TECHNOLOGY WAY • P.O. BOX 9106 • NORWOOD, MASSACHUSETTS 02062-9106 • 617/329-4700

# 12-Bit Voltage-Output DACs for Single Supply 5 V & 12 V Systems

by John Wynne

The basic CMOS Multiplying DAC, pioneered by Analog Devices, is a voltage-in, current-out device. Intended as a two-quadrant multiplier, the output signal current, which is proportional to the product of the digital input word and the input voltage reference, is steered into a virtual earth summing junction of an external op amp, the loop being closed around the op amp by the on-chip feedback resistor RFB. This circuit inherently provides signal inversion, a positive input signal is translated into a negative output voltage. The AD75XX family of CMOS multiplying DACs all behave like this.

In single supply applications CMOS DACs are operated in what is known as the voltage-switching mode. Figure 1 shows an AD7545A, a 12-bit CMOS DAC, configured for such operation. Reference voltage $V_1$ is applied to the OUT1 terminal, reference voltage $V_2$ is applied to the AGND terminal, and the output voltage is available at the $V_{REF}$ terminal. No signal inversion occurs from input to output hence the attraction of the circuit for single-supply applications. However, some linearity degradation should be expected when using the AD75XX DACs in the voltage-switching mode. This is due to the imbalance of the drive voltages on the N-channel switches in the R-2R ladder. With increasing voltage levels on $V_1$ & $V_2$, Integral Linearity or Relative Accuracy degrades much more rapidly than Differential Nonlinearity. In a typical HDD servo loop it is more important for the DAC driving the voice coil motor to be monotonic rather than be accurate to 12-bits. Appendix 1 shows some typical linearity performance curves for the AD7243 and AD7545A for various V1, V2 combinations.

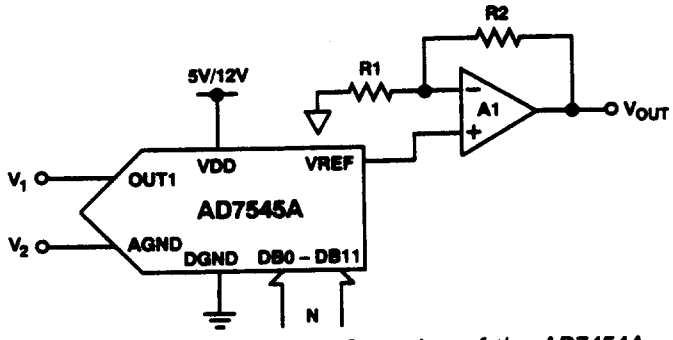



*Figure 1. Voltage-Switching Operation of the AD7454A with Buffer Amplifier*

Another family of CMOS DACs available from Analog Devices, the AD72XX family, produce a positive output voltage from a positive input voltage. Normal operation of these DACs is in fact the voltage-switching mode. The AD7237, a dual 12-bit DAC with 8+4 loading, and the AD7243, a serial loading 12-bit single DAC, are both suitable for use in the circuits presented here. Note that the AD7237 and AD7243 are not suitable for 5 V operation. In order to allow easy comparisons to be made between the various circuits in this application note the same $V_1$, $V_2$ nomenclature is used for all DACs. Thus for the AD7545A, $V_1$ is applied to OUT1, while for the AD7243 it is applied to REFIN.

### Voltage-Switching Mode Operation

There are several points worth noting about voltage-switching mode operation:

1. For the AD75XX DACs the output signal is a voltage at a constant output impedance equal to the ladder impedance. The circuit has no significant gain error as long as the current load at the $V_{REF}$ output is small, i.e., an output buffer amplifier is needed.

   For the AD7237 and AD7243 DACs the voltage output is already buffered by an on-board amplifier obviating the need for an additional external amplifier.

2. For the AD75XX DACs the reference voltage inputs $V_1$ and $V_2$ do not see constant input impedances but see input impedances which change with digital input code. Hence $V_1$ and $V_2$ must be low impedance sources. A somewhat similar situation exists with the AD7237 and AD7243 DACs, although with these devices the $V_1$ input is internally buffered by an op amp allowing a high source impedance for $V_1$. However $V_2$ must still be a low impedance source.

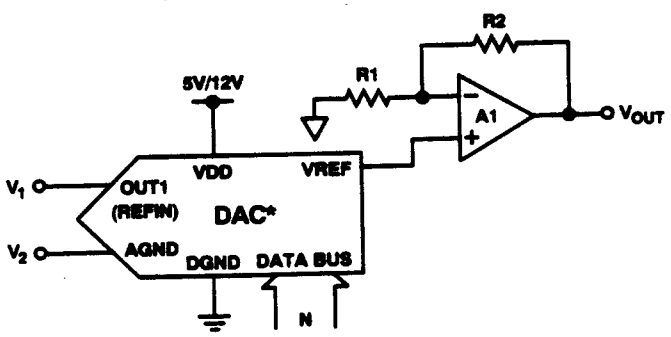
3. $V_1$ must always be more positive than $V_2$. If $V_1$ goes more than 0.3 V negative with respect to $V_2$, internal diodes and/or parasitic transistors will turn on leading to heavy current flow and possible device destruction. System power-on and power-off are the most obvious occasions when this reversal can take place, and these events should be carefully characterized.

4. For the AD75XX DACs the feedback resistor RFB is not generally used in the voltage-switching mode. For the circuits where it is not required tie it to $V_1$.

5. The output voltage expressions for Figures 2 to 4 sume that the DAC ladder termination resistor is at ne same potential as $V_2$. This assumption is valid for the AD7545A and AD7548, single 12-bit DACs, and AD7537, AD7547 & AD7549, dual 12-bit DACs.

6. In the output voltage expressions for Figures 2 to 5, D represents the fractional equivalent of the DAC digital input code in decimal. For a 12-bit DAC, D can vary from 0 to 4095/4096, i.e., D can almost, but never quite, equal unity. However, in order to allow easy comparisons between the different circuits the output voltage expression for each circuit is evaluated with D = 0, D = 1/2 and D = 1. It should be remembered that the output voltage expressions evaluated with D = 1 are in fact 1 LSB higher than is theoretically possible.

Figure 2 shows the classic voltage-switching mode circuit with a CMOS multiplying DAC and two reference voltage sources $V_1$ and $V_2$. When $V_2$ = 0 V the output voltage ranges from 0 V when D = 0 to $(1+R2/R1)V_1$ when D = 1. An obvious problem with having 0 V as one end of the output signal range in a single supply system is that, although the DAC output will get to 0 V, the single-supply op amp output almost certainly will not, especially if it is required to sink any appreciable load - rent. By applying a second reference voltage $V_2$ to AGND pin the all 0s code output voltage can be raised above 0 V. For 5 V systems $V_2$ must be kept quite small (≤0.5 V) since it reduces the drive on the DAC switches directly ($V_{DD} - V_2$) and generally increases the onset of linearity errors for a fixed value of $V_1$. For 12 V systems $V_2$ can be increased to 3 or 4 V, although for Figure 2 this is unlikely to be the case since $V_2$ is multiplied by the gain factor (1+R2/R1) to produce the all 0s end of the output signal range. This limits the usefulness of the circuit to applications where either $V_2$ is small or the required output signal range is small, i.e., a small gain factor. Note also that two low-output impedance voltage sources are required if the DACs are from the AD75XX family. With the AD7237 and AD7243 DACs, $V_1$ is buffered by on-chip buffer amplifiers obviating the low source impedance requirement on $V_1$.




*AD7545A, AD7237 OR AD7243
ADDITIONAL CIRCUITRY OMITTED FOR CLARITY

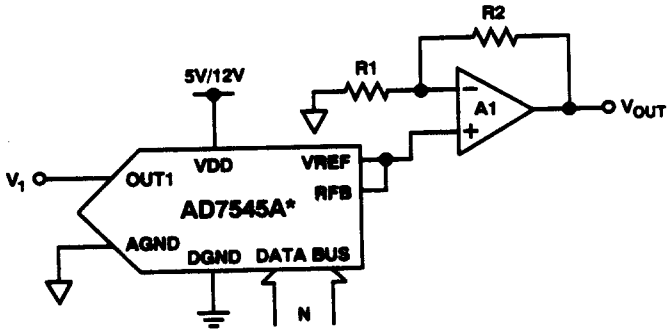
*Figure 2. Classic Voltage-Switching Mode Operation*

For the circuit of Figure 2 the output voltage is given as:

$$V_{OUT} = V_2(1+R2/R1) + (V_1-V_2)(1+R2/R1)D$$
where 1 LSB = $(V_1 - V_2)(1+R2/R1)(1/4096)$.

When D = 0,
$$V_{OUT} = V_2(1+R2/R1).$$
When D = 1/2,
$$V_{OUT} = V_2(1+R2/R1)+(V_1-V_2)(1+R2/R1)(1/2).$$
When D = 1,
$$V_{OUT} = V_2(1+R2/R1)+(V_1-V_2)(1+R2/R1)$$
$$= V_1(1+R2/R1)$$

Supplying two reference voltages, $V_1$ and $V_2$, to the circuit of Figure 2 is not the only method of moving the all 0s code output voltage above 0 V. Relevant only to the AD75XX family, Figure 3 shows the feedback resistor RFB, found on these DACs, wired to its own $V_{REF}$ output. This has the effect of moving the all 0s code output voltage to $(V_1/2)(1+R2/R1)$. Note that this is achieved without the need for a second reference voltage $V_2$. An interesting feature of this circuit is its voltage doubling nature—the all 1s code output voltage is double the all 0s code output voltage. Figure 3 is suitable for both 5 & 12 V systems. For 12 V systems, $V_1$ should be no more than 1.25 V above AGND in order to maintain 12-bit relative accuracy. For 5 V systems it is recommended that $V_1$ be no more than 0.25 V above AGND.



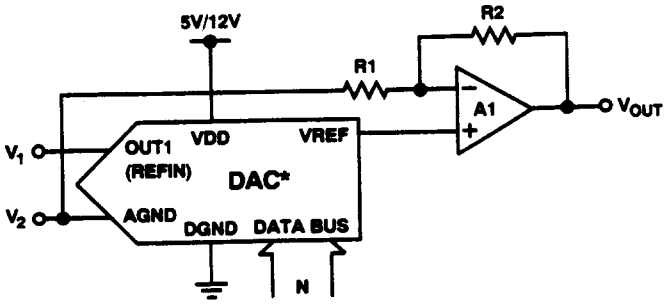

*ADDITIONAL CIRCUITRY OMITTED FOR CLARITY

*Figure 3. Using the Feedback Resistor $R_{FB}$ to Implement a Voltage Doubling Function*

For the circuit of Figure 3 the output voltage is given by:
$$V_{OUT} = (V_1/2)(1+R2/R1)+(V_1/2)(1+R2/R1)D$$
where 1 LSB = $(V_1/2)(1+R2/R1)(1/4096)$.

When D = 0,
$$V_{OUT} = (V_1/2)(1+R2/R1).$$
When D = 1/2,
$$V_{OUT} = (V_1/2)(1+R2/R1)+(V_1/2)(1+R2/R1)(1/2).$$
When D = 1,
$$V_{OUT} = V_1(1+R2/R1).$$

Figure 4 is a variation on Figure 2 and provides an all 0s code output voltage equal to $V_2$ and not $V_2(1+R2/R1)$ which Figure 2 provides. Hence, by appropriate choice of the gain setting resistors, R1 & R2, this circuit is suitable for producing wide output voltage ranges. The circuit requires two low output impedance voltage sources and is suitable for both 5 and 12 V systems.




*AD7545A, AD7237 OR AD7243
ADDITIONAL CIRCUITRY OMITTED FOR CLARITY

*Figure 4. Avoiding Any Gain Factor Multiplication of $V_2$*

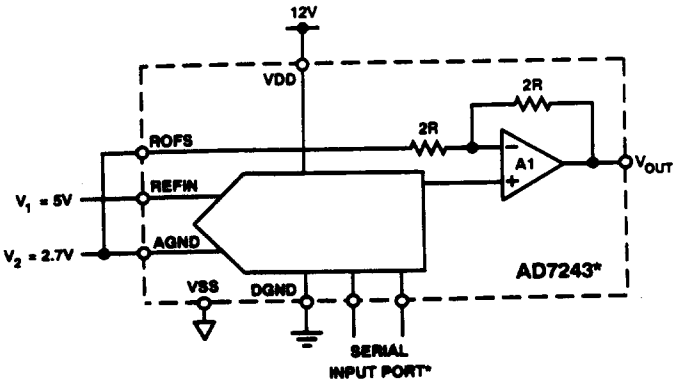
For the circuit of Figure 4 the output voltage is given by:

$V_{OUT} = V_2 + (V_1 - V_2)(1+R2/R1)D$
where 1 LSB = $(V_1 - V_2)(1+R2/R1)(1/4096)$.

When D = 0,
$V_{OUT} = V_2$.
When D = 1/2,
$V_{OUT} = V_2 + (V_1 - V_2)(1 + R2/R1)(1/2)$.

When D = 1,
$V_{OUT} = V_2 + (V_1 - V_2)(1 + R2/R1)$.

Figure 5 is a particular implementation of Figure 4 using an AD7243. This is a serial input, voltage-output 12-bit DAC which includes the output buffer amplifier A1 and matched, equal value, gain setting resistors. It is specified to operate from 12 V to 15 V $V_{DD}$. For 12-bit performance $V_1$ should be between 1.25 V and 3 V above $V_2$. With the equal value gain resistors giving a gain factor of 2, the output voltage range of this circuit is $2(V_1 - V_2)$ with one end of this voltage range being anchored at $V_2$ when D = 0. Input voltage $V_1$, which is applied to the REFIN input of the AD7243, is buffered by an on-chip buffer amplifier. This means that $V_1$ can be generated by a resistive divider from some higher voltage and does not need to be a low impedance source. Dependent upon the value of load resistance to ground, the output op amp in the AD7243 can experience headroom problems if the output voltage is required to swing within several volts of the $V_{DD}$ line. With $V_{DD}$ = 12 V ± 10%and a load of 2 kΩ to ground headroom problems, causing signal limiting, can occur above an 8 V output signal. Increasing the value of load resistance defers the onset of headroom problems.




*ADDITIONAL CIRCUITRY OMITTED FOR CLARITY

*Figure 5. Voltage-Switching Operation with the AD7243*

For the circuit of Figure 5 the output voltage is given by:

$V_{OUT} = 2.7 + (2.3)2D$
where 1 LSB = 4.6/4096 = 1.1 mV.
When D = 0,
$V_{OUT}$ = 2.7 V.
When D = 1/2,
$V_{OUT}$ = 5 V.
When D = 1,
$V_{OUT}$ = 7.3 V.

Another feature of the circuit (in common with Figure 4) is that the output voltage at the half-scale code, i.e., D = 1/2, is equal to $V_1$ and will follow $V_1$ as $V_1$ changes. Thus $V_1$ behaves as a quasi-ground and can be used by the signal conditioning circuitry to refer the analog output signal to a point other than 0 V. This is more obvious if the output voltage expression for Figure 5 is rewritten as shown

$V_{OUT} = V_1 + (V_1 - V_2).(2D-1)$
$= 5\text{ V} + (2.3).(2D-1)$.

**Appendix 1**

Figures A1–A4 show typical linearity plots of the AD7243 while Figures A5–A9 show linearity plots for the AD7545A.

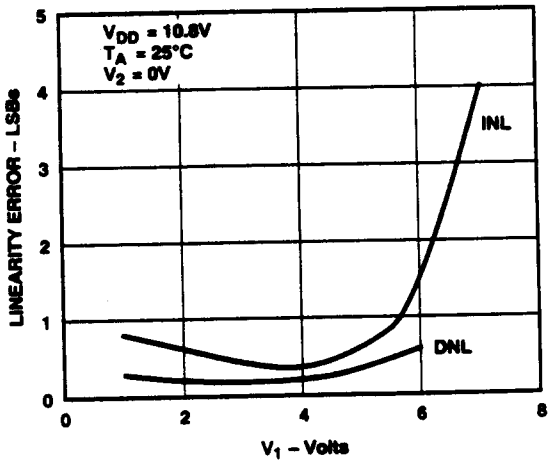



*Figure A1. AD7243 Linearity Error, $V_2$ = 0 V*

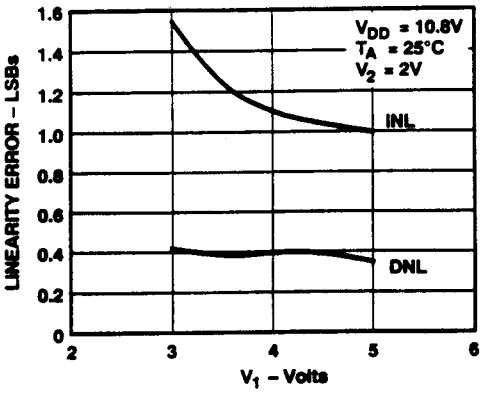



*Figure A2. AD7243 Linearity Error, $V_2$ = 2 V*

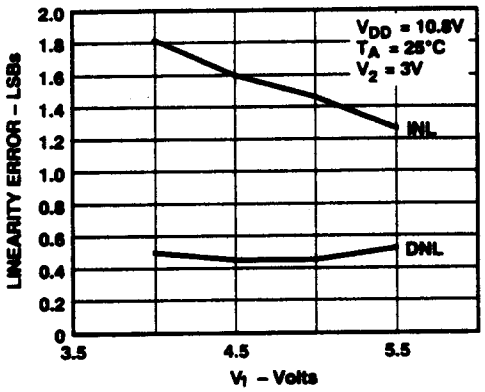



*Figure A3. AD7243 Linearity Error, $V_2$ = 3 V*

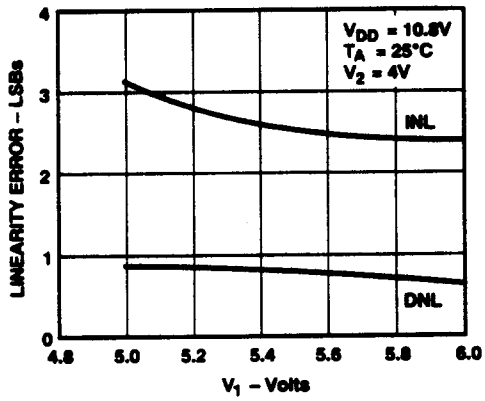



*Figure A4. AD7243 Linearity Error, $V_2$ = 4 V*

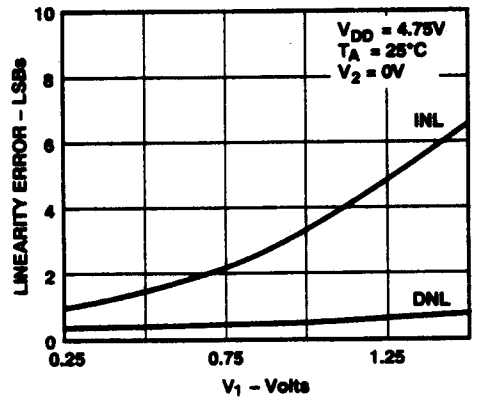



*Figure A5. AD7545A Linearity Error, $V_{DD}$ = 4.75 V, $V_2$ = 0 V*

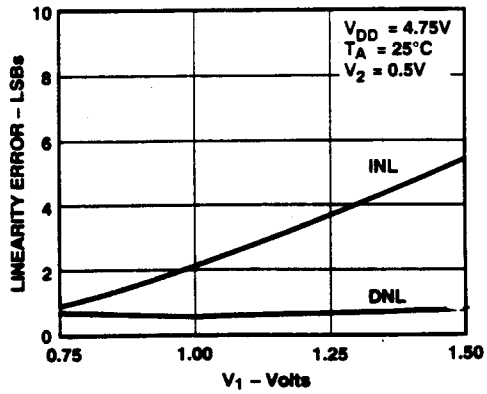



*Figure A6. AD7545A Linearity Error, $V_{DD}$ = 4.75 V, $V_2$ = 0.5 V*

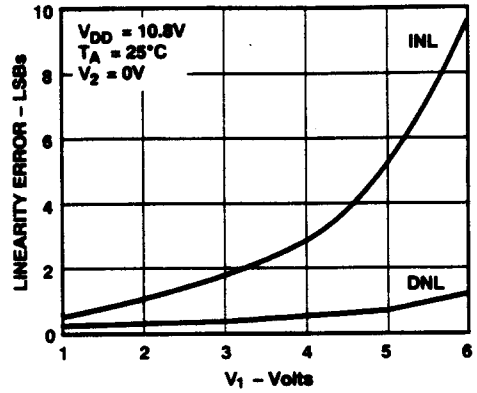



*Figure A7. AD7545A Linearity Error, $V_{DD}$ = 10.8 V, $V_2$ = 0 V*

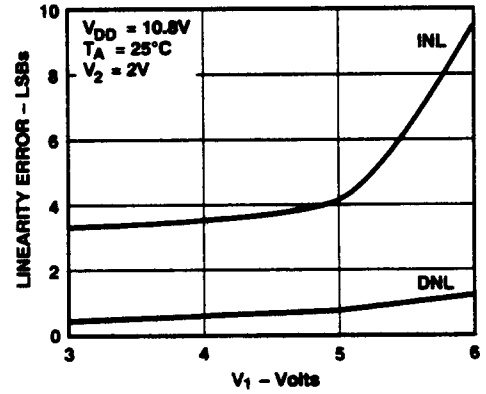



*Figure A8. AD7545A Linearity Error, $V_{DD}$ = 10.8 V, $V_2$ = 2 V*

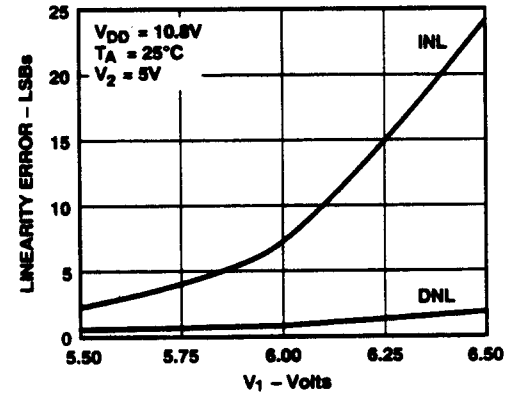



*Figure A9. AD7545A Linearity Error, $V_{DD}$ = 10.8 V, $V_2$ = 5 V*