

**12-Bit Analog I/O Port Uses  
AD7549 and 8051 Microcomputer**

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**INTRODUCTION**

In the process control industry, many slowly varying analog signals need to be measured and controlled. Examples of these are temperature, pressure, position, etc. This application note describes the design of an analog Input/Output port based on the AD7549 dual DAC and the 8051 microcomputer which will meet this requirement. The I/O port measures analog signals and also provides an analog output voltage which may be used in various system control loops (e.g., control voltage on a hydraulic servo valve).

**HARDWARE DESCRIPTION**

The two main components in the I/O port are the AD7549 dual DAC and the 8051 microcomputer. The AD7549 is a dual 12-bit DAC. Figure 1 illustrates the block diagram. For further information consult the AD7549 Data Sheet, available from Analog Devices. One DAC of the AD7549 provides the analog output voltage while the other performs the D/A function in a Successive Approximation ADC. The 8051 provides the interfacing signals to load DACB with the data for the analog output. It also performs the successive approximation routine with DACA to measure the analog input,  $A_{IN}$ .

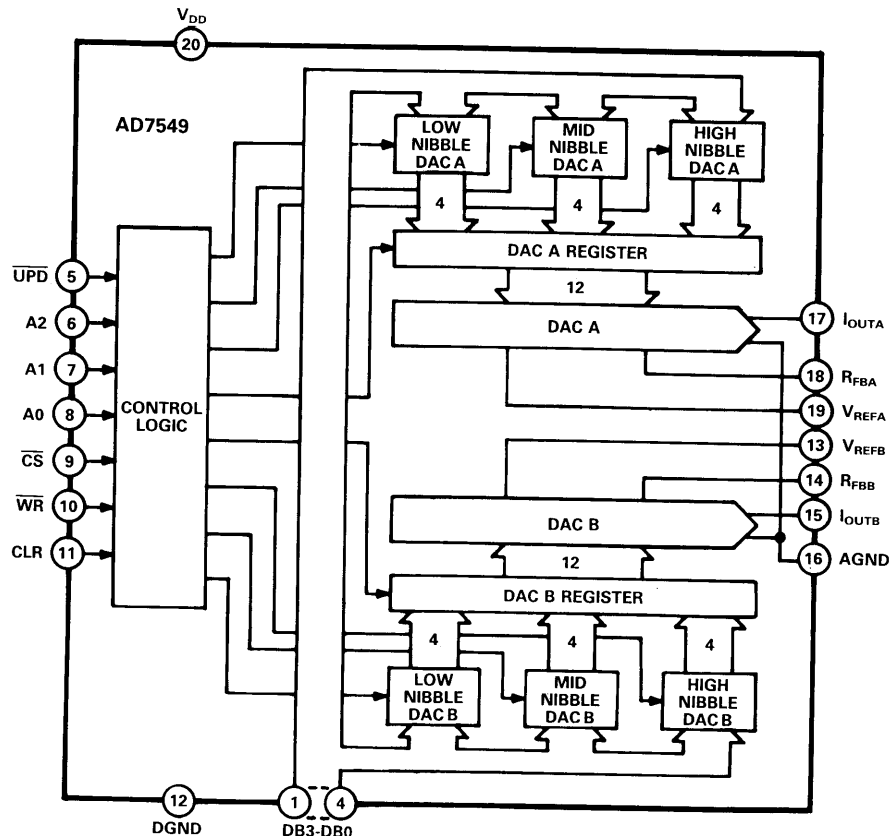


Figure 1. AD7549 Functional Block Diagram

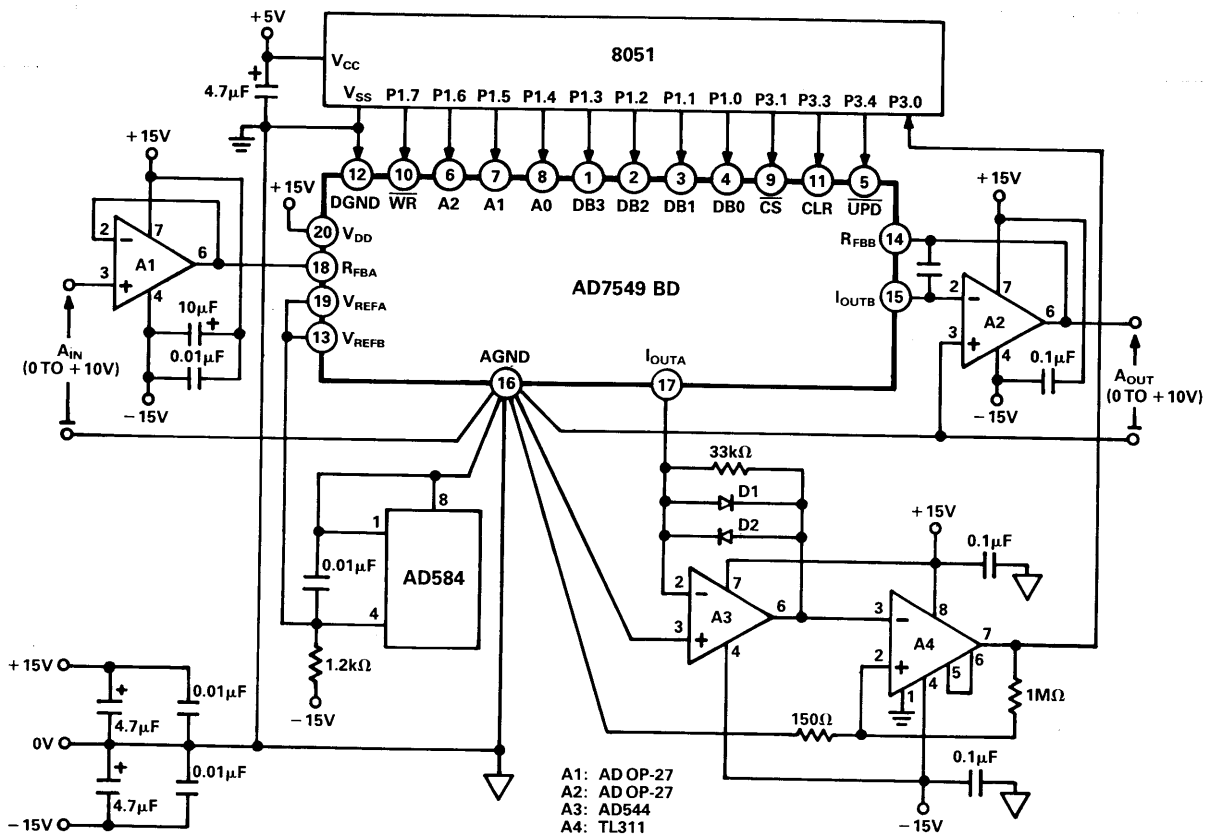


Figure 2. Analog I/O Port Circuit Diagram

The I/O port circuit diagram of Figure 2 also incorporates the AD584 voltage reference, an input buffer for  $A_{IN}$ , comparator circuit for the ADC and output amplifier for  $A_{OUT}$ .

The AD584 is connected to give a voltage reference of  $-10V$  to both DACs. This means that the  $A_{IN}$  range is  $0V$  to  $+10V$  and the  $A_{OUT}$  range is also  $0V$  to  $+10V$ . A1 (AD OP-27) buffers the analog input. Since the currents in the DAC are being switched at something less than  $100kHz$ , it is important that the buffer amplifier have a high loop gain at this frequency. The loop gain determines the output impedance and so the ability of the amplifier to maintain  $A_{IN}$  at a 12-bit level. The AD OP-27 open loop gain at  $100kHz$  is  $40dB$  (100). This means that the buffer output impedance is  $0.7\Omega$  (Open Loop Output Impedance divided by loop gain) which is driving a  $10k\Omega$  load. Error due to this is  $0.007\%$  and is well below the 12-bit level.

The ADC comparator section has two stages. A3 is an AD544 with a gain resistor of  $33k\Omega$  and back-to-back diodes (H5SCH-1001) to reduce settling time constraints. It is possible to trim the AD544  $V_{OS}$  (Input Offset Voltage) to take out offset in the ADC. The deciding factor in the choice of the AD544 is its extremely low input bias and offset currents. Currents of more than  $100nA$  can contribute errors of  $1/2LSB$  to the answer. A4 is a TL311 comparator with some hysteresis. Note that there is no pull-up resistor at the output of A4 even though it is an open collector type output. This is because P3.0, when configured as an input, provides an internal pull-up resistor.

A2 (AD OP-27) is the output amplifier for DACB and is connected to perform the current-to-voltage conversion for the DAC.

0100	A <sub>OUT</sub> :	CLR	P3.3	Disable the CLR line	226	SETB	P1.3	Set DAC 1st (5th,9th) MSB
102		SETB	P3.4	Set $\overline{UPD}$ high	228	CLR	P1.7	Bring $\overline{WR}$ low
104		CLR	P3.1	Bring $\overline{CS}$ low and select the AD7549	22A	CLR	P3.4	
106		MOV	R2, #04	Load Register R2 with 04. This will be used to set the device address lines	22C	SETB	P3.4	Strobe $\overline{UPD}$ pin
					22E	SETB	P1.7	Bring $\overline{WR}$ high
					230	JNB	P3.0,290	Test comparator A4 output. If 0, jump to routine to clear bit
108		ACALL	ADDRS	Register address loaded to AD7549				
10A		MOV	R0, #21		233	SETB	P1.2	Set DAC 2nd (6th,10th) MSB
10C		MOV	A, @R0	Load data (W) into DAC B low nibble register	235	CLR	P1.7	Bring $\overline{WR}$ low
10D		ACALL	DATA		237	CLR	P3.4	
10F		INC	R2	Set up next register address and load to the AD7549	239	SETB	P3.4	Strobe $\overline{UPD}$ pin
110		ACALL	ADDRS		23B	SETB	P1.7	Bring $\overline{WR}$ back high
112		MOV	A, @R0		23D	JNB	P3.0,294	Test comparator A4 output. If 0, jump to routine to clear bit
113		SWAP	A	Load data (V) into DACB mid nibble register				
114		ACALL	DATA		240	SETB	P1.1	Set DAC 3rd (7th,11th) MSB
116		INC	R2	Set up next register address and load to the AD7549	242	CLR	P1.7	Bring $\overline{WR}$ low
117		ACALL	ADDRS		244	CLR	P3.4	
119		DEC	R0		246	SETB	P3.4	Strobe $\overline{UPD}$ pin
11A		MOV	A, @R0	Load data (U) into DACB high nibble register	248	SETB	P1.7	Bring $\overline{WR}$ back high
11B		ACALL	DATA		24A	JNB	P3.0,298	Test A4 output. If 0, jump to routine to clear bit
11D		INC	R2	Set up DACB Register address and load to the AD7549	24D	SETB	P1.0	Set DAC 4th (8th,12th) MSB
11E		ACALL	ADDRS		24F	CLR	P1.7	Bring $\overline{WR}$ low
120		CLR	P1.7	Strobe the $\overline{WR}$ line to load data (UVW) to DAC B	251	CLR	P3.4	
122		SETB	P1.7		253	SETB	P3.4	Strobe $\overline{UPD}$ pin
124		SETB	P3.1	Bring $\overline{CS}$ high to deselect AD7549	255	SETB	P1.7	Bring $\overline{WR}$ back high
126		RET		Return to main program	257	JNB	P3.0,29C	Test A4 output. If 0, jump to routine to clear bit
0140	ADDRS:	MOV	A,R2	This subroutine takes the register address in R2, formats it and loads it out to the AD7549. It then returns to A <sub>OUT</sub> routine	25A	CLR	P1.7	Bring $\overline{WR}$ low
141		SWAP	A		25C	CLR	P3.4	
142		ORL	A, #80		25E	SETB	P3.4	Strobe $\overline{UPD}$ pin
144		MOV	P1,A		260	SETB	P1.7	Bring $\overline{WR}$ back high
146		RET			262	INC	R0	
0150	DATA:	ANL	A, #0F	This subroutine transfers the data nibble in the lower half of A to the AD7549 data bus and strobes the $\overline{WR}$ line low to load the appropriate register, before returning to A <sub>OUT</sub>	263	MOV	A, #0F	
152		ORL	P1,A		265	ANL	A,P1	Read nibble from port, and place result in address specified by R0
154		CLR	P1.7		267	MOV	@R0,A	
156		SETB	P1.7		268	JNB	P1.5,271	
158		RET			26B	CLR	P1.5	Set up address for DAC A mid nibble
0200	A <sub>IN</sub> :	MOV	R0, #21		26D	SETB	P1.4	
202		SETB	P3.0	Set up port line P3.0 as an input	26F	AJMP	226	
204		CLR	P3.3	Disable the CLR line	271	JNB	P1.4,278	
206		SETB	P3.4	Set $\overline{UPD}$ high	274	CLR	P1.4	Set up address for DAC A low nibble
208		CLR	P3.1	Bring $\overline{CS}$ low and select the AD7549	276	AJMP	226	
20A		MOV	P1, #00	Load DAC A low nibble register with all 0's	278	MOV	A,23	Take the 2 least significant nibbles and combine them in data memory location 23
20D		SETB	P1.7		27A	SWAP	A	
20F		SETB	P1.4		27B	ORL	A,24	
211		CLR	P1.7	Load DAC A mid nibble register with all 0's	27D	MOV	23,A	
213		SETB	P1.7		27F	SETB	P3.1	Bring $\overline{CS}$ high to deselect AD7549
215		CLR	P1.4		281	RET		Return to main program
217		SETB	P1.5					
219		CLR	P1.7	Load DAC A high nibble register with all 0's	290	CLR	P1.3	These instructions clear the AD7549 data bits and return to the successive approximation routine
21B		SETB	P1.7		292	AJMP	233	
21D		SETB	P1.4		294	CLR	P1.2	
21F		CLR	P1.7		296	AJMP	240	
221		SETB	P1.7	DAC A is now loaded with all 0's	298	CLR	P1.1	
223		MOV	P1, #0A0	Set up address for DAC A high nibble	29A	AJMP	24D	
					29C	CLR	P1.0	
					29E	AJMP	25A	

Table I. 8051 Routines for Programming the I/O Port

## SOFTWARE DESCRIPTION

Table I lists the complete analog I/O port software sub-routines. The I/O port should be considered as part of a larger control system. Whenever an analog input is to be measured or an analog output to be delivered, the program jumps to the appropriate subroutine. These sub-routines are A<sub>OUT</sub> and A<sub>IN</sub>. A<sub>OUT</sub> takes the 12 bits of data UVW contained in data memory locations 20, 21 and loads this data to DACB. So, the output of A2 (A<sub>OUT</sub>), is the analog value of the digital word, UVW.

A<sub>IN</sub> is the successive approximation routine for converting the analog signal, A<sub>IN</sub>, into its digital value XYZ and

placing the result in data memory locations 22 and 23. The routine initializes port outputs, clears the contents of DACA and then proceeds into the successive approximation routine proper. In this, it makes extensive use of the bit-handling instructions available on the 8051. Individual port bits may be cleared or set with a single instruction (CLR or SETB). Also, a single instruction (JNB) can test the state of port bits and jump to another location depending on the bit state. The use of these instructions simplifies the complete successive approximation routine. Table II shows the memory organization for the Analog I/O Port.

DATA MEMORY	CONTENTS
020	0U
021	VW
022	0X
023	YZ

Table II. Memory Organization for Analog I/O Port

**PERFORMANCE**

To perform the Analog Output function, the user jumps from the main program to subroutine A<sub>OUT</sub>. This occupies 55 bytes of memory and has an execution time of 74μs. This means that within 74μs of jumping to the subroutine, A<sub>OUT</sub> has reached the analog equivalent of UVW (Data in 20, 21). Since A2 (AD OP-27) has excellent input offset voltage characteristics, A<sub>OUT</sub> specifications will match those on the AD7549 data sheet. When the AD7549KN (BD, TD) is used, the integral linearity error is 1/2LSB.

Differential linearity is less than 1LSB, ensuring guaranteed monotonicity over temperature. Full-scale error (gain error) is 3LSBs max which corresponds to 0.073% F.S.R.

A<sub>IN</sub> is contained in 145 bytes of memory, and has an execution time which varies between 140μs and 180μs, depending on the value of A<sub>IN</sub>. This is the ADC conversion time. For the slowly varying signals which occur in process control systems, this speed is adequate. However, for a user who needs to measure higher frequency signals, increased bandwidth can be obtained by using an AD585 Sample/Hold amplifier instead of the input buffer, A1. This allows sampling of signals up to 2.7kHz.

Figure 3 shows how the output of A3 (top trace) varies during the A/D conversion cycle. At the end of the cycle, DAC is loaded with the digital value of A<sub>IN</sub>, causing the currents flowing into A3 inverting terminal to balance and bringing the voltage at the output of A3 to zero. The bottom trace is the start of conversion signal. This particular conversion is completed in approximately 160μs.

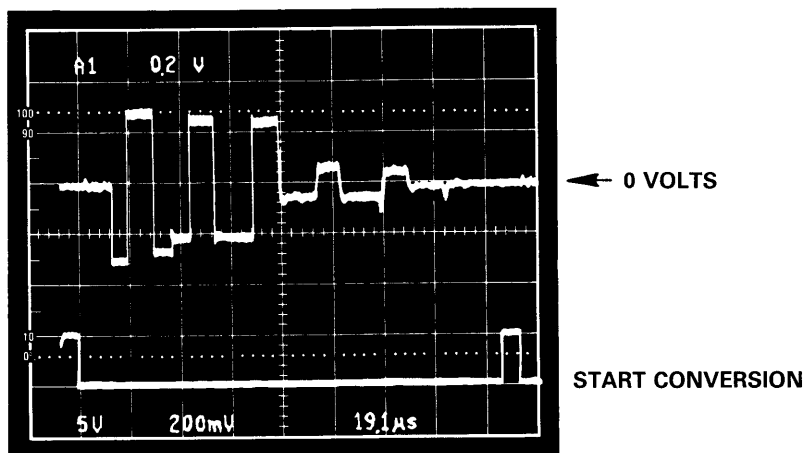


Figure 3. Voltage at A3 Output During the Conversion Cycle