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Driving a Center-Tapped Transformer with a Balanced Current-Output DAC

by Ken Gentile

The use of a center-tapped transformer as the output interface for a balanced current-output DAC offers several benefits. First, transformer coupling offers dc isolation between the DAC output and the final load. It can also aid in the rejection of common-mode signals present at the DAC output. Furthermore, transformer coupling can mitigate the even harmonics that result from an imbalance between the DAC outputs. Finally, all transformers have a limited bandwidth, which can be used to advantage for suppressing the Nyquist images that typically appear in a DAC output spectrum.

The goal of this application note is two-fold. The first goal is to provide an explanation of the functionality of a balanced output in the context of a current-output DAC. The second goal is to provide formulas that relate the transformer turns ratio (N), the transformer load (R_L), the DAC load resistors (R_O), and the maximum DAC output current (I_{MAX}).

BALANCED CURRENT-OUTPUT DAC

Balanced current-output DACs come in two varieties: those with current source outputs and those with current sink outputs. DACs with current source outputs always inject current into the external load, while DACs with current sink outputs always draw current from the external load. In both cases, the DAC output consists of two pins: a normal pin and a complementary pin. The arrows that indicate direction of current flow in the diagrams that follow assume conventional current flow (that is, current flows from a positive potential toward a negative potential).

Note that Figure 1 assumes that the DAC is of the current sourcing variety. In the case of a current sinking DAC, the direction of I_A and I_B is reversed. Also, a connection to V_{SUPPLY} should replace the ground connections at the transformer center tap and the R_O resistors.

In this application note, the current flowing through the normal and complementary pins is referred to as I_A and I_B, respectively. The maximum current that the DAC can deliver is denoted as I_{MAX} and represents the upper limit for both I_A and I_B. The exact value of I_A (or I_B) depends on the digital code present at the DAC input. The behavior of I_A and I_B is such that when the digital code is zero, then $I_A = 0$ and $I_B = I_{MAX}$. Conversely, when the digital code is full scale, then $I_A = I_{MAX}$ and $I_B = 0$. For intermediate digital codes, the two output currents are between zero and I_{MAX}, but are balanced such that $I_A + I_B = I_{MAX}$ at all times. Thus, I_A and I_B can be expressed as

$$I_A = \alpha I_{MAX} \qquad (1)$$

$$I_B = (1-\alpha)I_{MAX}$$

where α is the fractional digital code value, that is, the input digital code value to the DAC divided by the full-scale code value.

For example, given a 10-bit DAC with an input code of 200 and an I_{MAX} value of 10 mA, then $\alpha = 200/1023$ (where 1023 is the full-scale code value given by $2^{10} - 1$). This yields $I_A \approx 1.955$ mA and $I_B \approx 8.045$ mA. Also, notice that I_B can be expressed in terms of I_A as $I_B = I_{MAX} - I_A$.

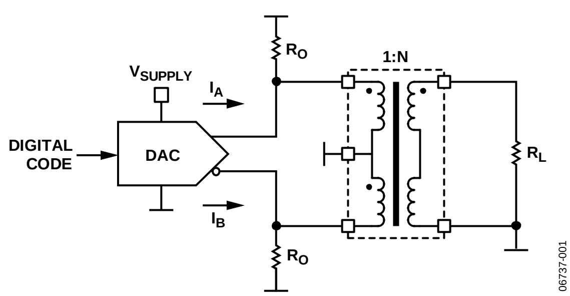

Figure 1. A Balanced Current-Output DAC with Transformer Coupling

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DC ANALYSIS

With an understanding of the operation of a balanced current-output DAC, a dc analysis of a center-tapped transformer coupled to the DAC output can now be examined. Figure 1 simplifies to the dc equivalent circuit shown in Figure 2, by replacing the DAC with two current sources (one for the normal output and the other for the complementary output). The magnitude of the current delivered by each source is code dependent, as indicated by Equation 1. The current sources have arrows that indicate the direction of current flow. It is assumed that the DAC outputs are of the current source variety. The arrows would be reversed for the current sink variety. In Figure 2, the center-tap connection is redrawn to clearly show that the DAC output circuits are independent current loops (note that the transformer polarity dots have been reoriented to maintain functional equality with Figure 1).

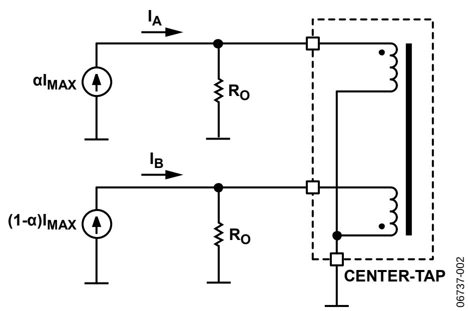

Figure 2. DC Equivalent Model

Typically, the resistance of the transformer windings is much less than the resistance of the DAC termination resistors (R_O). In most applications, this low winding resistance implies that the vast majority of the dc current associated with I_A (or I_B) flows through the transformer windings instead of through the termination resistors. Thus, the dc power rating for the DAC termination resistors is practically nil.

In general, consider a simple magnetic circuit consisting of a single winding with an arbitrary number of turns of wire (N) wrapped on the winding and a static current (I) flowing through the wire. The current flowing in the wire creates a magnetic flux (Φ) concentrated within the winding core that is proportional to the product of the number of wire turns and the current flowing through the wire (that is, $\Phi = kNI$, where k is the constant of proportionality). In the case of the tapped transformer, which has two primary windings, the magnetic flux in the core is the sum of the contributions of each winding (that is, $\Phi = k(N_AI_A + N_BI_B)$). Given that this analysis is based on a center-tapped transformer, the number of turns in each primary winding is the same (that is, $N_A = N_B$), which means that the magnetic flux can be expressed as $\Phi = kN(I_A + I_B)$. Thus, the total magnetic flux in the transformer core is proportional to the sum of the primary currents.

It is important to note in Figure 2 that I_A flows into the primary winding that is marked with a dot, while I_B flows into the primary winding that is opposite the dot. The placement of the dots indicates that the magnetic flux produced by I_A is opposed to the magnetic flux produced by I_B. The orientation of the dots implies that $\Phi = kN(I_A - I_B)$, instead of $kN(I_A + I_B)$ as previously stated, for the configuration shown in Figure 1 and Figure 2. Therefore, for the particular center-tapped configuration shown in Figure 1 and Figure 2, the net magnetic flux is proportional to the difference between I_A and I_B rather than the sum. This is a consequence of the physical connection between the complementary current source and the lower primary winding.

Combining this result with Equation 1, the magnetic flux in the transformer core can be expressed as $\Phi = kNI_{MAX}(2\alpha - 1)$. The importance of this result is that for the special case of $\alpha = ½$ (that is, the middle DAC code), the magnetic flux in the core is 0, whereas any other DAC code results in a build-up of static magnetic flux in the core. The significance of this fact is made apparent in the AC Analysis section that follows.

AC ANALYSIS

For ac analysis, consider the specific case in which a DAC generates a sinusoidal output signal. In such a case, a time series of digital codes drives the DAC and produces an output current that varies in sinusoidal fashion. The range of the digital input codes is split such that the lower half of the codes (0 to ½ full scale) generates the lower half of the sinusoid and the upper half of the codes (½ full scale to full scale) generates the upper half of the sinusoid. The average value of the DAC-generated sinusoid, therefore, is ½ full scale. The peak amplitude of the sinusoid is also ½ full scale, since this is the amount by which the signal can swing from the midpoint to either zero or full scale.

The sinusoidal current waveform at the normal output of the DAC can be expressed as

$$I_A = \tfrac{1}{2} I_{MAX} + \tfrac{1}{2} I_{MAX} \sin(\theta) \qquad (2)$$

where θ represents the instantaneous phase of the sinusoid.

Similarly, because of the relationship between I_A and I_B, the current waveform at the complementary output of the DAC can be expressed as

$$I_B = \tfrac{1}{2} I_{MAX} - \tfrac{1}{2} I_{MAX} \sin(\theta) \qquad (3)$$

Inspection of Equation 2 and Equation 3 indicates that I_A and I_B are both centered at $½I_{MAX}$. That is, $½I_{MAX}$ is the dc term of the sinusoidal waveform. Furthermore, when the magnitude of sine function increases, then I_A increases, whereas I_B decreases equally. Notice, too, that the sum of the normal and complementary output currents is always I_{MAX} (that is, $I_A + I_B = I_{MAX}$, as mentioned previously in the Balanced Current-Output DAC section). Such is the nature of a balanced output signal.

Note that Equation 2 and Equation 3 ignore the quantized nature of the sinusoidal DAC output current.

This result has interesting consequences when the DAC is driven by a digital sinusoidal generator like a direct digital synthesizer (DDS), for instance, that can be programmed to deliver either a sine signal or a cosine signal. When a sine signal is generated, Equation 2 and Equation 3 apply directly. When a cosine signal is generated, Equation 2 and Equation 3 become, respectively,

$$I_A = \tfrac{1}{2} I_{MAX} + \tfrac{1}{2} I_{MAX} \cos(\theta)$$

and

$$I_B = \tfrac{1}{2} I_{MAX} - \tfrac{1}{2} I_{MAX} \cos(\theta)$$

Given the special case of $\theta = 0$, the sine case yields $I_A = ½I_{MAX}$ and $I_B = ½I_{MAX}$, whereas the cosine case yields $I_A = I_{MAX}$ and $I_B = 0$. In the DC Analysis section, it was shown that $\Phi = kN(I_A - I_B)$. Thus, if the digital generator stalls at $\theta = 0$, the transformer core carries no magnetic flux for the sine case and kNI_{MAX} for the cosine case. The implication is that if the digital generator is stalled at $\theta = 0$, and is then switched from sine to cosine (or vice versa), the magnetic flux in the core jumps from 0 to kNI_{MAX} (or vice versa). This results in a voltage spike across all of the transformer windings due to the nearly infinite rate of change of flux in the transformer core.

The previous paragraphs explore the transient behavior of the transformer when switching between sine and cosine waveforms. To explore the steady state behavior of the transformer in the context of ac analysis, it is necessary to understand how a transformer behaves under the stimulus of a sinusoidal signal. This is covered in the appendices. Appendix A describes the basic ac behavior of an ideal transformer, while Appendix B builds on Appendix A to show the ac operation of a tapped transformer.

Figure 3 is the ac equivalent model assuming an ideal, center-tapped transformer. Also given in Equation 4 to Equation 7 is a list of the pertinent equations that relate the various circuit parameters. Both the diagram and the equations are a result of the concepts described in Appendix B.

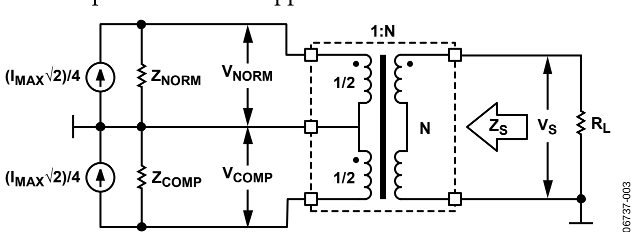

Figure 3. AC Equivalent Model Using a Center-Tapped Transformer

$$Z_{NORM} = Z_{COMP} = \frac{R_O R_L}{2R_L + 4R_O N^2} \tag{4}$$

$$Z_S = 2N^2 R_O \tag{5}$$

$$v_{NORM} = v_{COMP} = \left(\frac{\sqrt{2} I_{MAX}}{8}\right)\left(\frac{R_O R_L}{R_L + 2R_O N^2}\right) \tag{6}$$

$$v_S = \left(\frac{\sqrt{2} I_{MAX}}{2}\right)\left(\frac{N R_O R_L}{R_L + 2R_O N^2}\right) \tag{7}$$

Equation 4 through Equation 7 can be used to predict the impedance seen by each DAC output (Z_{NORM} and Z_{COMP}), the voltage generated by each of the DAC current sources (v_{NORM} and v_{COMP}), the impedance presented at the transformer secondary (Z_S), and the voltage across the secondary (v_S). It is important for the reader to understand that v_{NORM} and v_{COMP} do not represent the voltage that appears across each primary winding, but rather the voltage produced by each current source (I_A or I_B) as it flows through the reflected impedance of the associated primary winding (Z_{NORM} or Z_{COMP}).

The actual voltage that appears across each primary winding is referred to as v_A for the upper primary winding and v_B for the lower. The value of v_A and v_B can be derived from v_S and the associated turns ratio between the secondary and each primary winding. Thus, v_A and v_B can be expressed as

$$v_A = v_B = v_S\left(\frac{\frac{1}{2}}{N}\right) = \left(\frac{\sqrt{2} I_{MAX}}{4}\right)\left(\frac{R_O R_L}{R_L + 2R_O N^2}\right)$$

Note that v_A and v_B are twice as large as v_{NORM} and v_{COMP}. What is the reason for the discrepancy? The answer lies in the fact that the two primary windings interact with each other. Consider Figure 4 where a switch has been added to provide a means to disconnect the normal DAC output pin from the circuit.

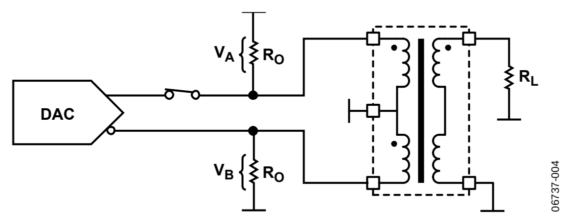

Figure 4. Balanced Current-Output DAC with Isolation Switch

If the switch is open (see Figure 5), there is effectively no change from an impedance point of view, because the current source internal to the DAC exhibits a very high impedance (ideally infinite). Thus, the complementary output drives the same load regardless of the state of the switch. The voltage at the complementary output (v_{COMP}) is that given by Equation 6. However, the upper and lower primary windings are mutually coupled with a turns ratio of 1:1. This causes a voltage of the same magnitude to also appear at the upper primary winding (as shown in Figure 5).

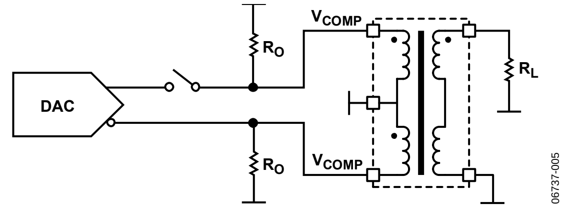

Figure 5. Isolated DAC output

The importance of this fact cannot be overstressed. With the normal output of the DAC completely disconnected, there is still a voltage present (v_{COMP}) across the upper DAC termination resistor (R_O). Its presence is due to the mutual coupling of the two primary windings and the voltage produced by the complementary DAC output driving its associated load (Z_{COMP}).

With the switch closed as in Figure 4, the current generated by the normal DAC output produces a voltage across its equivalent load (Z_{NORM}). The magnitude of this voltage is v_{NORM} and is the same as v_{COMP}. By superposition, this signal sums with the signal produced by the complementary output, that is $v_A = v_{NORM} + v_{COMP}$. But $v_{NORM} = v_{COMP}$, so $v_A = 2v_{NORM}$, which is why v_A is twice as large as v_{NORM}. Likewise, v_B is twice as large as v_{COMP}.

This yields another pair of equations useful for analyzing the center-tapped circuit:

$$v_A = 2v_{NORM} \text{ and } v_B = 2v_{COMP} \tag{8}$$

IMPEDANCE MATCHING

In many applications, it is desirable that Z_S be equal to R_L. This is especially true when a reconstruction filter is inserted between the secondary and the load, as shown in Figure 6.

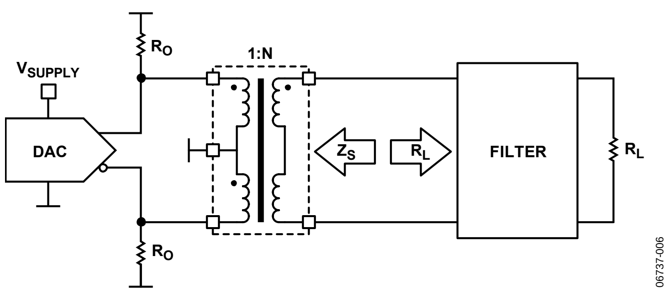

Figure 6. DAC with Reconstruction Filter

Generally, the filter is designed to accommodate equal source and load impedances, which implies that $Z_S = R_L$. Equation 32 in Appendix B shows that $Z_S = 2N^2R_O$. If it is desired that $Z_S = R_L$, then R_L can be substituted for Z_S. Solving for R_O yields

$$R_O = \frac{R_L}{2N^2} \tag{9}$$

With this choice of R_O, Equation 4 through Equation 7 can be simplified as follows:

$$Z_{NORM}\Big|_{Z_S=R_L} = Z_{COMP}\Big|_{Z_S=R_L} = \frac{R_L}{8N^2} \tag{10}$$

$$Z_S = R_L \tag{11}$$

$$v_{NORM}\Big|_{Z_S=R_L} = v_{COMP}\Big|_{Z_S=R_L} = \frac{\sqrt{2}I_{MAX}R_L}{32N^2} \tag{12}$$

$$v_S\Big|_{Z_S=R_L} = \frac{\sqrt{2}I_{MAX}R_L}{8N} \tag{13}$$

Also, Equation 8 can be rewritten for the special case of $Z_S = R_L$ as

$$v_A\Big|_{Z_S=R_L} = v_B\Big|_{Z_S=R_L} = \frac{\sqrt{2}I_{MAX}R_L}{16N^2} \tag{14}$$

Furthermore, the power delivered to the load is a function of v_S, so Equation 7 can be used to express the power delivered to the load as

$$P_L = \frac{{v_S}^2}{R_L} = \frac{R_L}{2}\left(\frac{I_{MAX}R_ON}{R_L + 2R_ON^2}\right)^2 \tag{15}$$

In the case of impedance matching (that is, $Z_S = R_L$, which implies R_O, as given in Equation 9), the P_L equation reduces to

$$P_L\Big|_{Z_S=R_L} = \frac{R_L}{2}\left(\frac{I_{MAX}}{4N}\right)^2 \tag{16}$$

Equation 16 defines the power delivered to the load for the impedance matched case and Equation 15 for the general case. It is interesting to compare Equation 15 and Equation 16 and to consider the effect on P_L in Equation 15 when R_O is varied. Recall that there is only one particular value of R_O that provides impedance matching; namely, $R_O = R_L/(2N^2)$. If, however, impedance matching is not a requirement, then there is the freedom to choose any arbitrary value for R_O. By rewriting Equation 15 in a slightly different form (as shown in Equation 17), the effect on P_L due to varying R_O becomes apparent. In this form, it is evident that a decrease in R_O results in a decrease in the squared term, and vice versa.

$$P_L = \frac{R_L}{2}\left(\frac{I_{MAX}N}{\frac{R_L}{R_O} + 2N^2}\right)^2 \tag{17}$$

In fact, P_L is at a minimum when $R_O = 0$ (that is, $P_L = 0$, as expected) and at a maximum when $R_O = \infty$. For the latter,

$$P_{L_{MAX}} = \lim_{R_O \to \infty}\left\{\frac{R_L}{2}\left(\frac{I_{MAX}N}{\frac{R_L}{R_O} + 2N^2}\right)^2\right\} = \frac{R_L}{2}\left(\frac{I_{MAX}}{2N}\right)^2 \tag{18}$$

Comparison of Equation 16 and Equation 18 indicates that four times more power (+6 dB) is delivered to the load when $R_O = \infty$ as compared to the impedance matched case.

EXAMPLE CALCULATIONS

Here, the previous formulas are used to determine the component values for two different transformer applications. In Example 1, a transformer with a 1:1 turns ratio (N = 1) is employed, while in Example 2, a transformer with a 1:2 turns ratio (N = 2) is employed. Both examples use I_{MAX} = 20 mA, R_L = 50 Ω, and assume that impedance matching is employed (that is, $Z_S = R_L$).

Example 1: I_{MAX} = 20 mA, R_L = 50 Ω, and N = 1

From Equation 9,

R_O = 25 Ω (the value of the two DAC termination resistors)

From Equation 10,

$Z_{NORM} = Z_{COMP}$ = 6.25 Ω (the load driven by each DAC output pin)

From Equation 14,

$v_A = v_B$ = 88.39 mV rms (the voltage across each primary)

From Equation 13,

v_S = 176.8 mV rms (the voltage across the secondary)

From Equation 16,

P_L = 0.625 mW (the power in the load)

Example 2: I_{MAX} = 20 mA, R_L = 50 Ω, and N = 2

From Equation 9,

R_O = 6.25 Ω (the value of the two DAC termination resistors)

From Equation 10,

$Z_{NORM} = Z_{COMP}$ = 1.5625 Ω (the load driven by each DAC output pin)

From Equation 14,

$v_A = v_B$ = 22.10 mV rms (the voltage across each primary)

From Equation 13,

v_S = 88.39 mV rms (the voltage across the secondary)

From Equation 16,

P_L = 0.156 mW (the power in the load)

REDUCTION OF EVEN HARMONICS

The degree of dc balance between the normal and complementary DAC current sources has a direct impact on the magnitude of even harmonics in the DAC output spectrum. Using a transformer as the output coupling mechanism for the DAC effectively masks any dc imbalance in the DAC outputs. This results in a significant reduction of even harmonics when the spectrum is observed at the output of the transformer.

Transformer coupling can also mask the effects of a dynamic imbalance between the DAC outputs. However, the ability of the transformer to mask an ac imbalance depends on the inherent longitudinal balance of the transformer. Transformers with a high degree of longitudinal balance require that the manufacturer pay special attention to the physical design of the transformer. The most common factor limiting the longitudinal balance of a transformer is parasitic capacitive coupling within the windings. The transformer must be designed in such a way that the parasitic capacitance is evenly distributed relative to the external contacts of the windings.

CONCLUSION

A center-tapped transformer can be used to advantage as the coupling element for a balanced current-output DAC. Formulas have been presented to determine the load (Z_{NORM} and Z_{COMP}) and voltage (v_A and v_B) at each DAC output pin, the voltage (v_S) across the load (R_L), and the power (P_L) delivered to the load (R_L). Furthermore, the relationship between the DAC termination resistors (R_O), the load resistance (R_L), and the transformer turns ratio (N) was defined.

APPENDIX A

Transformer Basics

The basic behavior of a transformer is governed by its turns ratio (or winding ratio). The turns ratio, N, is the ratio of the number of turns of wire in the secondary windings (N_S) to the number of turns of wire in the primary windings (N_P); that is, $N = N_S/N_P$. The turns ratio is often denoted on schematics by two colon-separated numbers (for example, 3:5). An example appears in Figure 7 in which an arbitrary turns ratio of A:B is shown. This leads to the relationship $N = N_S/N_P = B/A$.

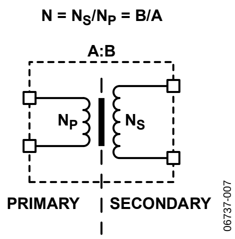

Figure 7. Basic Transformer

In Figure 8, a transformer is shown with its primary winding driven by a voltage source of V_{SRC} (volts rms) that has a series resistance of R_{SRC} (ohms). The secondary is terminated with an arbitrary resistance of R_{TERM}. When a transformer is driven by an ac signal, the ratio of the voltage across the secondary winding to the voltage across the primary winding is the same as the turns ratio; that is, $v_S/v_P = N$. This gives rise to the concept of voltage transformation. That is, the primary voltage is transformed to a secondary voltage (or vice versa) based on the turns ratio.

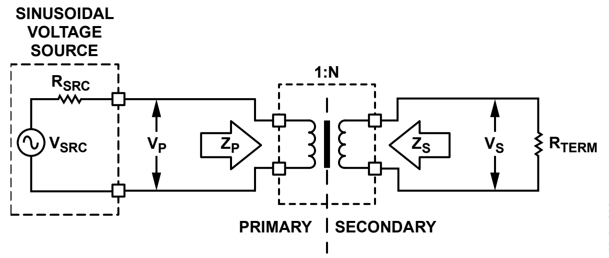

Figure 8. Transformer Driven by an AC Source

Furthermore, conservation of energy requires that the power exhibited in the primary winding must equal the power appearing in the load of the secondary winding (R_{TERM}). Alternatively, the power exhibited in the secondary winding must equal the power appearing in the load of the primary winding (R_{SRC}). This knowledge makes it possible to treat R_{TERM} as though it appears in the primary circuit as Z_P (that is, the secondary impedance is transformed to an equivalent primary impedance). On the other hand, R_{SRC} can be treated as though it appears in the secondary circuit as Z_S, (that is, the primary impedance is transformed to an equivalent secondary impedance). This property of impedance transformation is related to the turns ratio and is expressed as: $Z_P = (1/N^2)R_{TERM}$ and $Z_S = (N^2)R_{SRC}$. The concept of impedance transformation is demonstrated by the equivalent circuits shown in Figure 9.

Note that when selecting a transformer, the reader should be aware that some manufacturers specify the impedance transformation ratio rather than the turns ratio. The turns ratio (N) is found by taking the square root of the impedance transformation ratio.

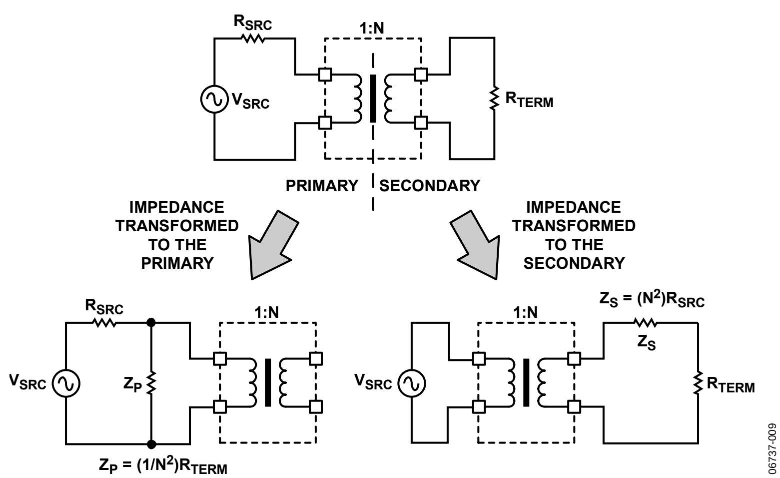

Figure 9. Transformed Impedance

APPENDIX B

A Balanced Current-Output DAC Driving a Tapped Transformer

Figure 10 shows the general case for a DAC coupled to a tapped transformer. For completeness, the two primary windings are not assumed to be symmetrical (that is, the primary tap does not split the primary winding into two equal halves) and the two DAC termination resistors are not assumed to be equal (R_A and R_B).

The primary winding is split into two separate circuits as a result of the ground connection at the primary tap. The upper winding is referred to as Primary A and the lower winding as Primary B. The windings are labeled A, B, and C to indicate the number of turns associated with each winding (Primary A, Primary B, and secondary, respectively). The overall turns ratio of the transformer is 1:N, where N = C/(A + B). The tapped transformer exhibits the following three independent ac-coupled networks (the associated turns ratios appear in parentheses):

- Primary A and the secondary (A:C)
- Primary B and the secondary (B:C)
- Primary A and Primary B (A:B)

Also shown in Figure 10 are the transformed impedances at Primary A (Z_A), Primary B (Z_B), and the secondary (Z_S) along with the voltages that appear across each winding (v_A, v_B, and v_S).

Since the DAC is assumed to be of the balanced, current-output variety, Figure 10 can be redrawn as shown in Figure 11. The DAC is replaced by current sources I_A and I_B. These represent sinusoidal current sources with a peak-to-peak amplitude of I_{MAX} (the maximum output current of the DAC). Also, the center-tap connection is drawn differently than in Figure 10 to clearly show that the signal sources exist as separate current loops.

Z_A consists of two parallel impedances. The first is the transformed impedance of the secondary resistor (R_L), which is referred to as Z_1. The second is the transformed impedance of R_B, which is referred to as Z_2. Note that the DAC output impedance can be ignored under the assumption that the internal current sources exhibit an infinite impedance (ideally), which means that the internal impedance of the DAC output does not impact the parallel combination of Z_1 and Z_2. Therefore, Z_A can be expressed as (see Appendix A regarding impedance transformation):

$$Z_A = Z_1 \,||\, Z_2 = \left\{\left(\tfrac{A}{C}\right)^2 R_L\right\} || \left\{\left(\tfrac{A}{B}\right)^2 R_B\right\}$$

$$= \left\{\frac{R_L A^2}{C^2}\right\} || \left\{\frac{R_B A^2}{B^2}\right\} = \frac{R_L R_B}{R_L\left(\frac{B}{A}\right)^2 + R_B\left(\frac{C}{A}\right)^2} \qquad (19)$$

Note that the symbol || in this and all subsequent equations can be read as "in parallel with."

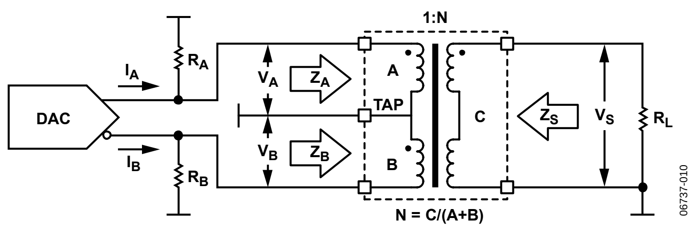

Figure 10. A Balanced Current-Output DAC Coupled to a Tapped Transformer

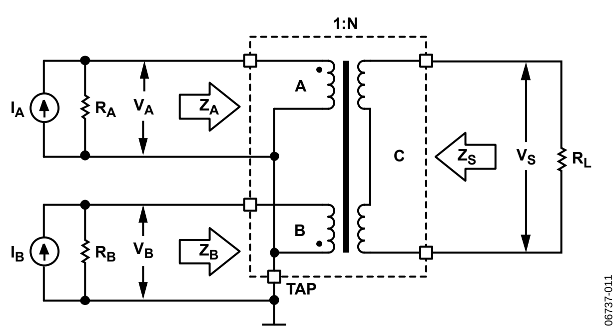

Figure 11. DAC Shown as a Dual Current Source

Likewise, the value of Z_B consists of two parallel impedances. The first is the transformed impedance of the secondary resistor (R_L), which is referred to as Z_3. The second is the transformed impedance of R_A, which is referred to as Z_4. Therefore, Z_B can be expressed as:

$$Z_B = Z_3 \parallel Z_4 = \left\{\left(\tfrac{B}{C}\right)^2 R_L\right\} \parallel \left\{\left(\tfrac{B}{A}\right)^2 R_A\right\}$$

$$= \left\{\frac{R_L B^2}{C^2}\right\} \parallel \left\{\frac{R_A B^2}{A^2}\right\} = \frac{R_L R_A}{R_L\left(\frac{A}{B}\right)^2 + R_A\left(\frac{C}{B}\right)^2} \tag{20}$$

Similarly, the value of Z_S consists of two parallel impedances. The first is the transformed impedance of R_A, which is referred to as Z_5. The second is the transformed impedance of R_B, which is referred to as Z_6. Therefore, Z_S can be expressed as:

$$Z_S = Z_5 \parallel Z_6 = \left\{\left(\tfrac{C}{A}\right)^2 R_A\right\} \parallel \left\{\left(\tfrac{C}{B}\right)^2 R_B\right\}$$

$$= \left\{\frac{R_A C^2}{A^2}\right\} \parallel \left\{\frac{R_B C^2}{B^2}\right\} = \frac{R_A R_B}{R_A\left(\frac{B}{C}\right)^2 + R_B\left(\frac{A}{C}\right)^2} \tag{21}$$

Referring to Figure 11, the sinusoidal current delivered by the normal and complementary DAC outputs is given by $I_A = ½I_{MAX} + ½I_{MAX}\sin(\theta)$ and $I_B = ½I_{MAX} - ½I_{MAX}\sin(\theta)$, respectively. However, for ac analysis, the dc term in both equations can be eliminated, yielding $I_A = ½I_{MAX}\sin(\theta)$ and $I_B = -½I_{MAX}\sin(\theta)$.

Furthermore, in the context of ac analysis, the sine function can be replaced by its rms equivalent, √2/2, which yields

$$I_A = \tfrac{\sqrt{2}}{4} I_{MAX} \text{ and } I_B = -\tfrac{\sqrt{2}}{4} I_{MAX} \tag{22}$$

Note that $I_B = -I_A$. From these results, Figure 11 can be redrawn by replacing I_A with its rms equivalent and by replacing I_B with $-I_A$ (see Figure 12).

The upper current source drives the side of Primary A marked with a dot, while the lower current source drives the side of Primary B that is not marked with a dot. However, the dot associated with Primary B can be moved to the other side of the Primary B winding without impacting the functionality as long as the connection to the signal source is reversed. Reversal of the signal source is equivalent to simply changing its sign. This is shown in Figure 13, where the sign of the lower current source is changed and the dot is moved to the other side of the Primary B winding.

With the modification in Figure 13 it is no longer necessary to treat I_A and I_B separately because it is now apparent that

$$I_A = I_B = \tfrac{\sqrt{2}}{4} I_{MAX} \tag{23}$$

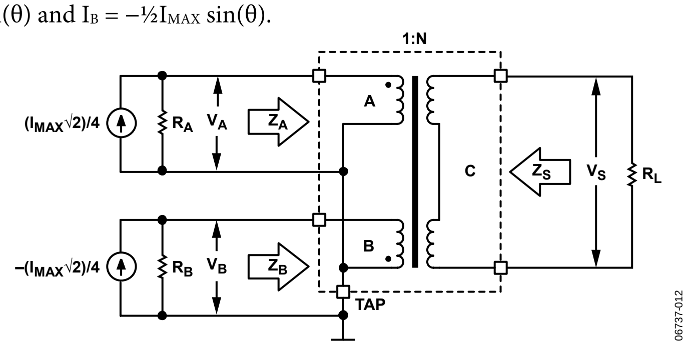

Figure 12. Modified AC Equivalent Model

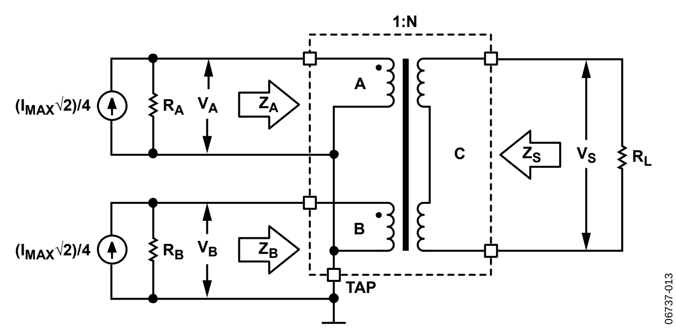

Figure 13. AC Equivalent Model with the Primary B Circuit Modified

Notice that the load as seen by the current source driving Primary A is the parallel combination of R_A and Z_A. Likewise, the load as seen by the current source driving Primary B is the parallel combination of R_B and Z_B. These loads are referred to as Z_{NORM} and Z_{COMP}, since they are the loads as seen by the normal and complementary outputs of the DAC, respectively, and are given as

$$Z_{NORM} = R_A \,||\, Z_A = \{R_A\} \,||\, \left\{\frac{R_L R_B}{R_L\left(\frac{B}{A}\right)^2 + R_B\left(\frac{C}{A}\right)^2}\right\}$$

$$= \frac{R_A R_B R_L}{R_A R_L\left(\frac{B}{A}\right)^2 + R_A R_B\left(\frac{C}{A}\right)^2 + R_B R_L} \quad (24)$$

$$Z_{COMP} = R_B \,||\, Z_B = \{R_B\} \,||\, \left\{\frac{R_L R_A}{R_L\left(\frac{A}{B}\right)^2 + R_A\left(\frac{C}{B}\right)^2}\right\}$$

$$= \frac{R_A R_B R_L}{R_B R_L\left(\frac{A}{B}\right)^2 + R_A R_B\left(\frac{C}{B}\right)^2 + R_A R_L} \quad (25)$$

This result makes it possible to express the voltage generated by each DAC output, which is the product of the DAC output current and the load as seen by the DAC output. The normal and complementary DAC output voltages are expressed as

$$v_{NORM} = I_A Z_{NORM}$$

$$= \left(\frac{\sqrt{2} I_{MAX}}{4}\right)\left(\frac{R_A R_B R_L}{R_A R_L\left(\frac{B}{A}\right)^2 + R_A R_B\left(\frac{C}{A}\right)^2 + R_B R_L}\right) \quad (26)$$

$$v_{COMP} = I_B Z_{COMP}$$

$$= \left(\frac{\sqrt{2} I_{MAX}}{4}\right)\left(\frac{R_A R_B R_L}{R_B R_L\left(\frac{A}{B}\right)^2 + R_A R_B\left(\frac{C}{B}\right)^2 + R_A R_L}\right) \quad (27)$$

where I_A and I_B have been replaced based on Equation 23.

The secondary voltage (v_S) is made up of the contribution of each of the primary voltages multiplied by the associated turns ratio. Specifically,

$$v_S = v_{NORM}\left(\frac{C}{A}\right) + v_{COMP}\left(\frac{C}{B}\right) = \left(\frac{\sqrt{2} I_{MAX}}{4}\right) \times$$

$$\left(\frac{R_A R_B R_L\left(\frac{C}{A}\right)}{R_A R_L\left(\frac{B}{A}\right)^2 + R_A R_B\left(\frac{C}{A}\right)^2 + R_B R_L} + \frac{R_A R_B R_L\left(\frac{C}{B}\right)}{R_B R_L\left(\frac{A}{B}\right)^2 + R_A R_B\left(\frac{C}{B}\right)^2 + R_A R_L}\right) \quad (28)$$

The two primary voltages (v_A and v_B) can be derived from v_S based on the respective turns ratios, as follows:

$$v_A = v_S\left(\frac{A}{C}\right) = \left(\frac{\sqrt{2} I_{MAX}}{4}\right) \times$$

$$\left(\frac{R_A R_B R_L}{R_A R_L\left(\frac{B}{A}\right)^2 + R_A R_B\left(\frac{C}{A}\right)^2 + R_B R_L} + \frac{R_A R_B R_L\left(\frac{A}{B}\right)}{R_B R_L\left(\frac{A}{B}\right)^2 + R_A R_B\left(\frac{C}{B}\right)^2 + R_A R_L}\right) \quad (29)$$

$$v_B = v_S\left(\frac{B}{C}\right) = \left(\frac{\sqrt{2} I_{MAX}}{4}\right) \times$$

$$\left(\frac{R_A R_B R_L\left(\frac{B}{A}\right)}{R_A R_L\left(\frac{B}{A}\right)^2 + R_A R_B\left(\frac{C}{A}\right)^2 + R_B R_L} + \frac{R_A R_B R_L}{R_B R_L\left(\frac{A}{B}\right)^2 + R_A R_B\left(\frac{C}{B}\right)^2 + R_A R_L}\right) \quad (30)$$

The equations derived thus far will work for any generalized case of a tapped transformer. However, in practice, there are two simplifications that significantly reduce the complexity of these equations. The first is to use a center-tapped transformer (that is, A = B). The second is to use equal DAC termination resistors (that is, $R_A = R_B$) of value R_O. Additionally, recall that N = C/(B + A). With the stipulation that A = B, it is possible to show that C/B = C/A = 2N. Applying these concepts to the previous equations yields the following simplified equations:

$$Z_{NORM} = Z_{COMP} = \frac{R_O R_L}{2R_L + 4R_O N^2} \quad (31)$$

$$Z_S = 2N^2 R_O \quad (32)$$

$$v_{NORM} = v_{COMP} = \left(\frac{\sqrt{2} I_{MAX}}{8}\right)\left(\frac{R_O R_L}{R_L + 2R_O N^2}\right) \quad (33)$$

$$v_S = \left(\frac{\sqrt{2} I_{MAX}}{2}\right)\left(\frac{N R_O R_L}{R_L + 2R_O N^2}\right) \quad (34)$$

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