CMOS Monolithic DC-DC Voltage Converter & Reference

AD7560

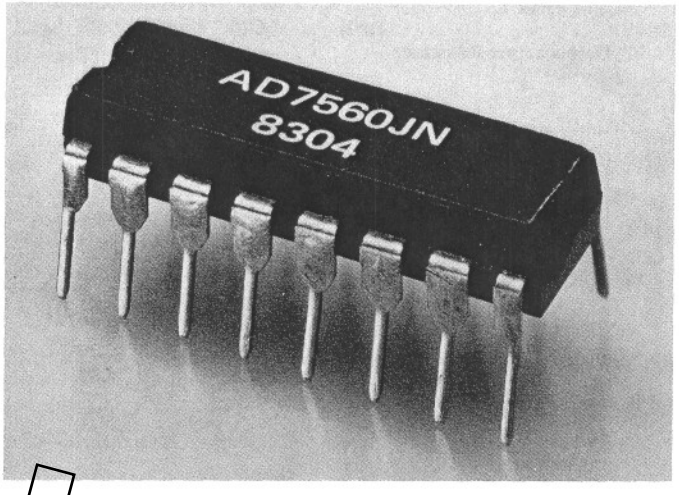
PRELIMINARY TECHNICAL DATA

FEATURES

- Efficient Series Stacked dc/dc Converters Which Provide Multiple Outputs From a Single +5V Supply (−5V, −10V, −15V, +10V, +15V)
- On-Chip −10V Reference Voltage Output
- High Reference Voltage Power Supply Rejection
- Minimum Circuit Requires Only Two Low Cost Capacitors

APPLICATIONS

- Negative Reference Voltage Generation for Data Acquisition Systems, from a Single +5V Supply
- Op-Amp Supply Generation; ±5V, ±15V
- Low Power, High Efficiency Voltage Converter for Single Battery Operation



GENERAL DESCRIPTION

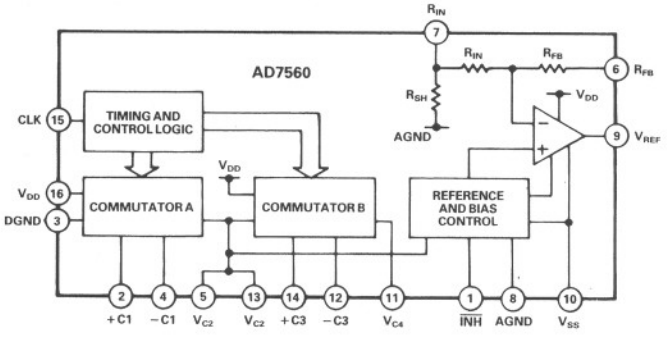
The AD7560 is a monolithic CMOS voltage converter plus voltage reference circuit. It performs both voltage inversion and subsequent voltage multiplication of the incoming positive supply voltage. It contains two converter circuits, A and B, in series to provide two negative output voltages of approximately $-V_{DD}$ and $-3V_{DD}$ from the $+V_{DD}$ input. The unregulated $-3V_{DD}$ output from converter B is used to generate an internal reference voltage of −5V. This is buffered and amplified to provide a temperature compensated −10V output (V_{REF}, pin 9) which can sink over 1.0mA. In applications where the reference output is not required this section can be powered down via the reference inhibit input $\overline{INH}$, pin 1.

An on-chip oscillator is provided to drive the converters. The oscillator frequency is determined by the addition of an external capacitor. Additionally, if converter synchronization to an external clock source is required, the clock input can be driven directly from a 5V CMOS compatible clock source.

PRODUCT HIGHLIGHTS

1. The AD7560 produces multiple output voltages with a minimum number of external components, e.g., basic configurations require only two or four low cost general purpose electrolytic capacitors.
2. A −10V voltage reference output which can be powered down if not required.
3. The 5V CMOS compatible clock input can be driven from an external clock source (for synchronization) or can be made to oscillate with the addition of an external capacitor.
4. All outputs are short-circuit proof and latch-up free.

AD7560 FUNCTIONAL BLOCK DIAGRAM



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SPECIFICATIONS

(V_{DD} = +5V[1], F_{CLK} = 6kHz external clock, $0 \le I_{REF} \le 1mA$ (see test circuits, Figures 1 & 2). All specifications T_{min} to T_{max}[2] unless otherwise noted)

Parameter	$\overline{INH}$ = 0V[3]	$\overline{INH}$ = V_{DD}[4]	Units	Conditions/Comments
CONVERTER A, V_{C2} (Pins 5 & 13)				
Voltage Conversion Factor, α_A				
T_A = +25°C	0.90	0.68	min	$I_{C2} = I_{C4} = 0mA$
	0.95	0.80	typ	
T_{MIN}, T_{MAX}	0.85	0.65	min	
	0.90	0.75	typ	
V_{C2} Output Source Resistance				
T_A = +25°C	160	N.A.	Ω max	$I_{C2} = 5mA$, $I_{C4} = 0mA$, I_{REF} = N.A. (Not Applicable)
	120	N.A.	Ω typ	
T_{MIN}, T_{MAX}	200	N.A.	Ω max	
T_A = +25°C	N.A.	160	Ω max	$I_{C2} = 1mA$, $I_{C4} = 0mA$, $0 \le I_{REF} \le 0.25mA$
	N.A.	120	Ω typ	
T_{MIN}, T_{MAX}	N.A.	200	Ω max	
V_{C2} Short Circuit Current	30	30	mA typ	Short Circuit to DGND
CONVERTER B, V_{C4} (Pin 11)				
Voltage Conversion Factor, α_B				
T_A = +25°C	2.80	2.35	min	$I_{C2} = I_{C4} = 0mA$
	2.90	2.45	typ	
T_{MIN}, T_{MAX}	2.75	2.30	min	
	2.85	2.35	typ	
V_{C4} Output Source Resistance				
T_A = +25°C	900	N.A.	Ω max	$I_{C2} = 0mA$, $I_{C4} = 2.5mA$, I_{REF} = N.A.
	750	N.A.	Ω typ	
T_{MIN}, T_{MAX}	1200	N.A.	Ω max	
T_A = +25°C	N.A.	900	Ω max	$I_{C2} = 0mA$, $I_{C4} = 0.25mA$, $0 \le I_{REF} \le 0.25mA$
	N.A.	750	Ω typ	
T_{MIN}, T_{MAX}	N.A.	1200	Ω max	
V_{C4} Short Circuit Current	20	20	mA typ	Short Circuit to DGND
VOLTAGE REFERENCE[5], V_{REF} (PIN 9)				
Reference Voltage Output	N.A.	−10.00	V	
Reference Voltage Accuracy	N.A.	±500	mV max	
Reference Temperature Coefficient[6]	N.A.	±200	ppm/°C max	
Reference Voltage Drift	N.A.	±60	mV typ	1,000 hours, +70°C
Reference Sink Current, I_{REF}	N.A.	1.0	mA min	
		1.5	mA typ	
Reference Output Resistance	–	3	Ω max	
	20K	1	Ω typ	
Reference Short Circuit Current	0.4	5	mA max	Short Circuit to AGND
Power Supply Rejection				
V_{REF}/V_{DD}	N.A.	±12	mV/V max	
		±6	mV/V typ	
Buffer Amplifier Resistor Values				
R_{IN} and R_{FB}	30/50/75	30/50/75	kΩ min/typ/max	
Input Shunt Resistance, R_{SH}	75	75	kΩ typ	R_{SH} is Approximately $1.5R_{FB}$
DIGITAL INPUTS				
INH (Pin 1)				
V_{IH} Input High Voltage	+3.0	+3.0	V min	
V_{IL} Input Low Voltage	+0.8	+0.8	V max	
I_{IN} Input Current	±10	±10	μA max	V_{IN} = 0V or V_{DD}
C_{IN} Input Capacitance[7]	7	7	pF max	
CLK (Pin 15)				
V_{IH} Input High Voltage	+3.0	+3.0	V min	
V_{IL} Input Low Voltage	+0.8	+0.8	V max	
I_{IN} Input Current	±25	±25	μA max	V_{IN} = 0V or V_{DD}
	±15	±15	μA typ	
POWER REQUIREMENTS				
Power Supply Current, I_{DD}	6	22	mA max	$I_{C2} = I_{C4} = 0mA$
	3	15	mA typ	
	16	N.A.	mA max	$I_{C2} = 0mA$, $I_{C4} = 2.5mA$
	12	N.A.	mA typ	
V_{DD} Operating Range	+4.5/+5.5	+4.75/+5.5	V	Specifications not guaranteed outside V_{DD} = +5V ±5%
	+4.5/+7.5	+4.75/+7.5	V	Degraded performance over this range. External limit resistors required. See Figure 15.

NOTES

[1] V_{DD} = +5V ±5%.

[2] Temperature range of AD7560JN is −25°C to +70°C.

[3] See test circuit, Figure 1.

[4] See test circuit, Figure 2.

[5] To meet this voltage reference specification (T_{min} to T_{max}) external loading on V_{C2} (pins 5 & 13) and V_{C4} (pin 11) should be restricted to satisfy conditions $|V_{C4}| \ge |V_{REF}| + 0.5V$. Refer to Figures 4 and 9.

[6] Using internal resistors R_{FB} and R_{IN}.

[7] Guaranteed by design, not tested.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

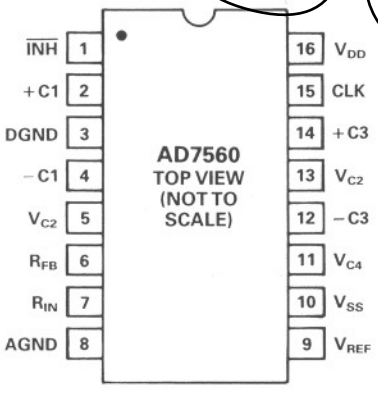
V_{DD} to DGND	−0.3V, +8V
V_{DD} to V_{C2}	−0.3V, +16V
V_{DD} to V_{C4}	−0.3V, +32V
V_{DD} to V_{SS}	−0.3V, +32V
V_{C2}, −C1, (DGND = 0V)	V_{DD}, −8V
V_{C4}, −C3, (DGND = 0V)	V_{DD}, −24V
+C1 (DGND = 0V)	−0.3V, V_{DD}
+C3 (DGND = 0V)	V_{C2}, V_{DD}
AGND to DGND	V_{SS}, V_{DD}
CLK, $\overline{INH}$, (DGND = 0V)	V_{DD}, −5V
V_{REF}	V_{DD}, V_{SS}
R_{IN}, R_{FB} (AGND = 0V)	±15V
I_{DD}	100mA dc
I_{REF} Short Circuit Duration to V_{DD}	Continuous
I_{C2} Short Circuit Duration to DGND	Continuous
I_{C4} Short Circuit Duration to DGND	Continuous
Operating Temperature Range, JN	−25°C to +70°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10secs)	+300°C
Power Dissipation (Package) to +50°C	450mW
Derate Above +50°C by	6mW/°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational selections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

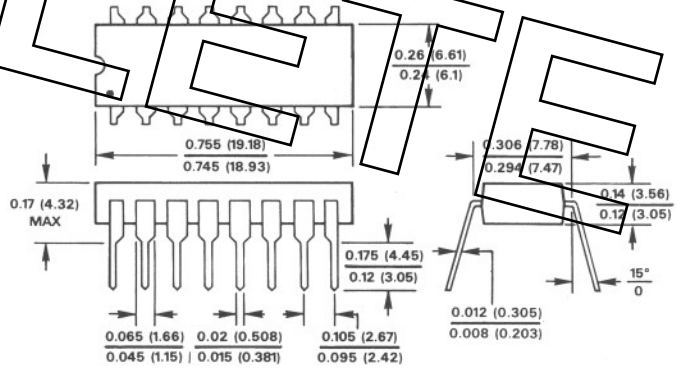
ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The foam should be discharged to the destination socket before devices are removed.

PIN CONFIGURATION



OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS ARE SOLDER OR TIN-PLATED KOVAR OR ALLOY 42

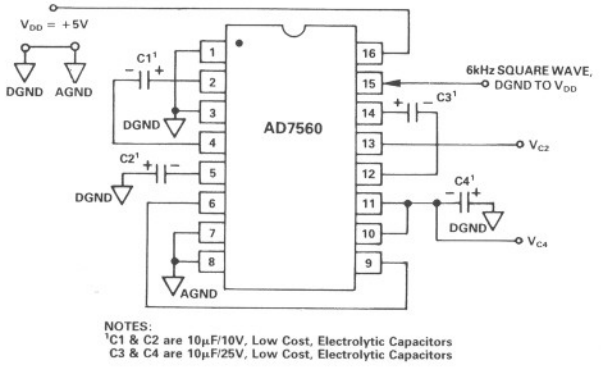
ORDERING INFORMATION

Reference Voltage Accuracy (T_{min} to T_{max})	Reference Voltage T.C. (max)	Temperature Range & Package −25°C to +70°C Plastic
±500mV	±200ppm/°C	AD7560JN

PRICING INFORMATION, 100+

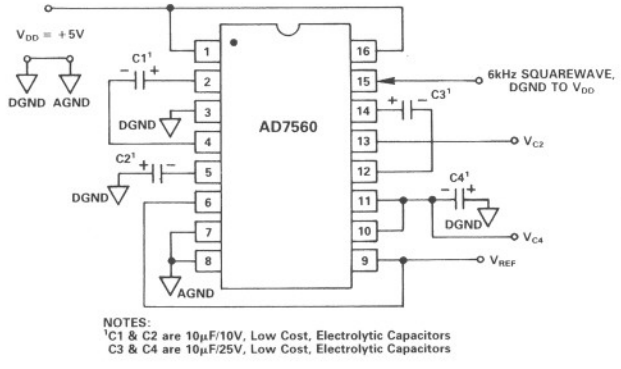
AD7560JN: $4.75

TEST CIRCUITS



NOTES:
¹C1 & C2 are 10μF/10V, Low Cost, Electrolytic Capacitors
C3 & C4 are 10μF/25V, Low Cost, Electrolytic Capacitors

Figure 1. Test Circuit for dc-dc Converter Only, $\overline{INH}$ = 0V



NOTES:
¹C1 & C2 are 10μF/10V, Low Cost, Electrolytic Capacitors
C3 & C4 are 10μF/25V, Low Cost, Electrolytic Capacitors

Figure 2. Test Circuit for dc/dc Converter & Voltage Reference, $\overline{INH}$ = V_{DD}

Typical Performance Characteristics

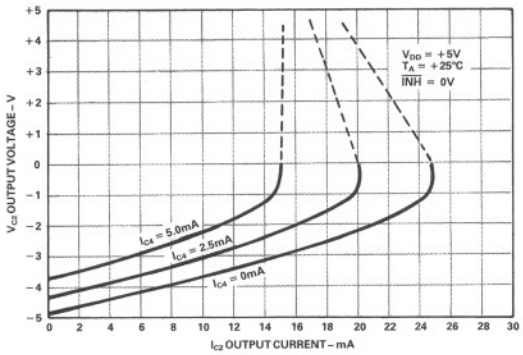


Figure 3. V_{C2} Output Voltage vs. I_{C2} Output Current for Different Values of I_{C4} (See Figure 1)

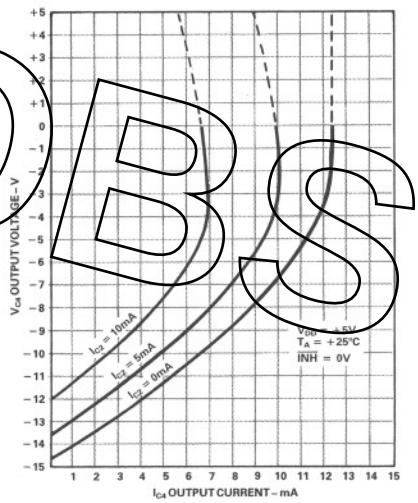


Figure 4. V_{C4} Output Voltage vs. I_{C4} Output Current for Different Values of I_{C2} (see Figure 1)

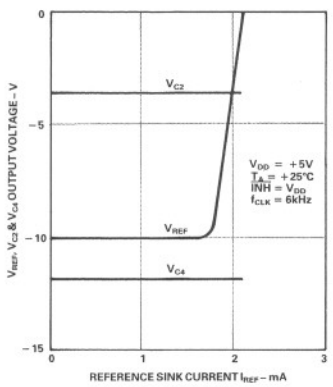


Figure 5. V_{REF}, V_{C2} and V_{C4} Output Voltage Levels vs. Reference Sink Current I_{REF} (see Figure 2)

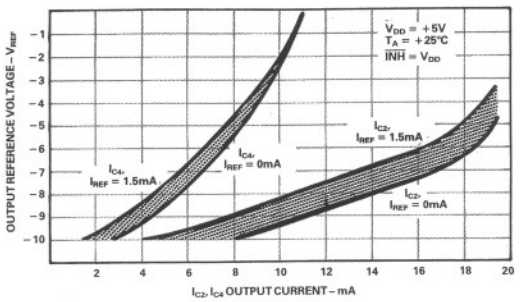


Figure 6. Output Reference Voltage V_{REF} vs. I_{C2} and I_{C4} Load Currents (see Figure 2)

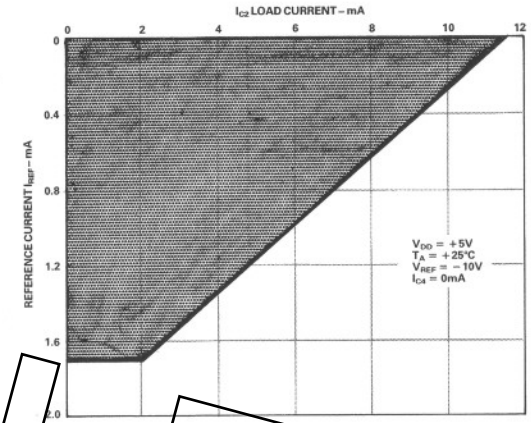


Figure 7. I_{C2} vs. I_{REF} Operating Area (Shaded) for V_{REF} = – 10V (see Figure 2)

Figure 8. I_{C4} vs. I_{REF} Operating Area (Shaded) for V_{REF} = – 10V (see Figure 2)

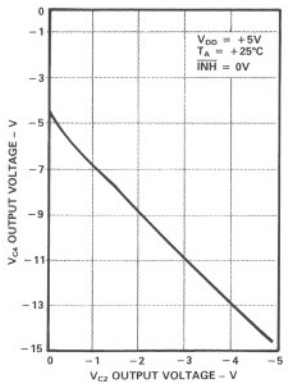


Figure 9. V_{C4} Output Voltage vs. V_{c2} Output Voltage i.e., V_{C4} Output Voltage as a Function of Current Loading on V_{C2} (see Figure 1)

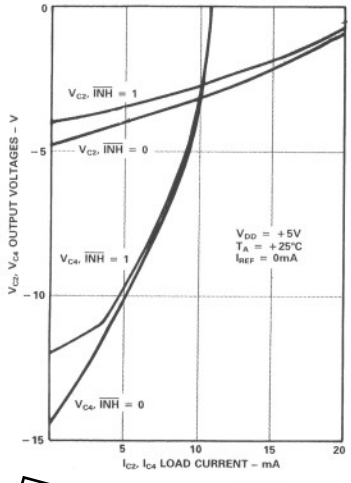


Figure 10. Effect of INHIBIT Input ($\overline{INH}$, Pin 1) on Converter Efficiency

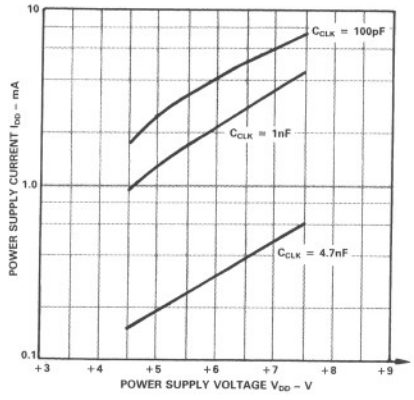


Figure 13. Power Supply Current vs. Power Supply Voltage for Different Values of C_{CLK}

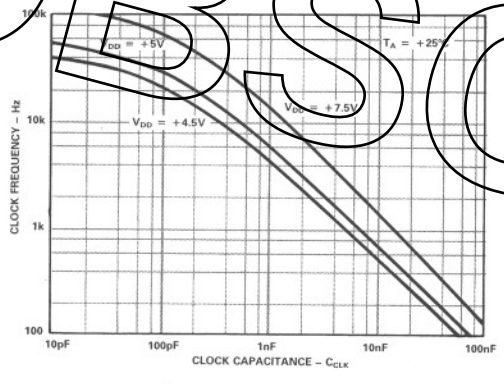


Figure 11. Typical Clock Frequency vs. Clock Capacitance

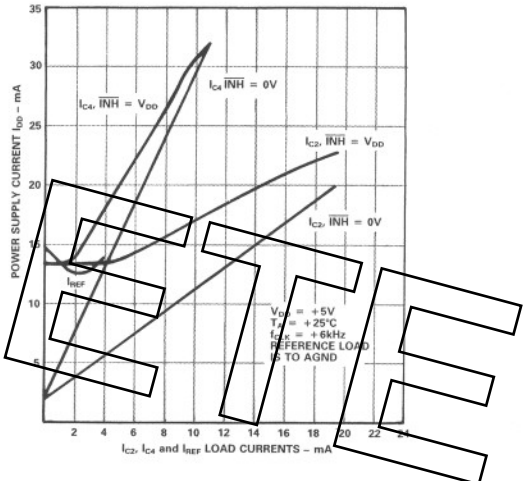


Figure 14. Power Supply Current I_{DD} vs. I_{C2}, I_{C4} and I_{REF} Load Currents

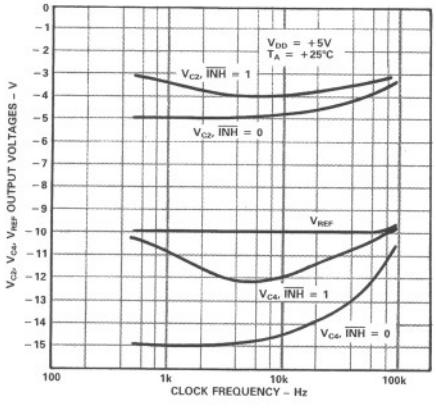


Figure 12. V_{C2}, V_{C4} and V_{REF} Output Voltages vs. Clock Frequency

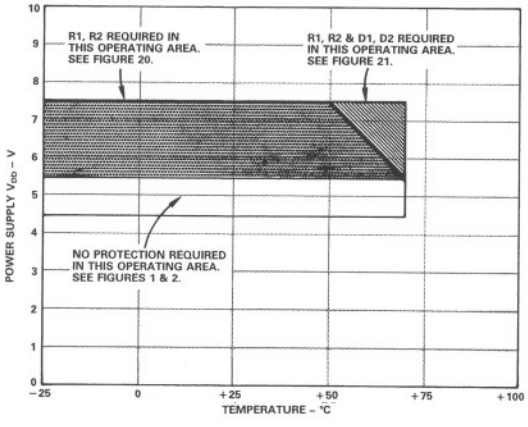


Figure 15. Operating Areas as a Function of Supply Voltage and Temperature

CIRCUIT DESCRIPTION

The AD7560 consists of two separate dc-to-dc converters which are driven in series plus a precision voltage reference with buffer amplifier. The voltage conversion circuitry of the AD7560 may best be understood by referring to Figure 16. This shows the two converters A, and B, each comprising four switches and two external capacitors.

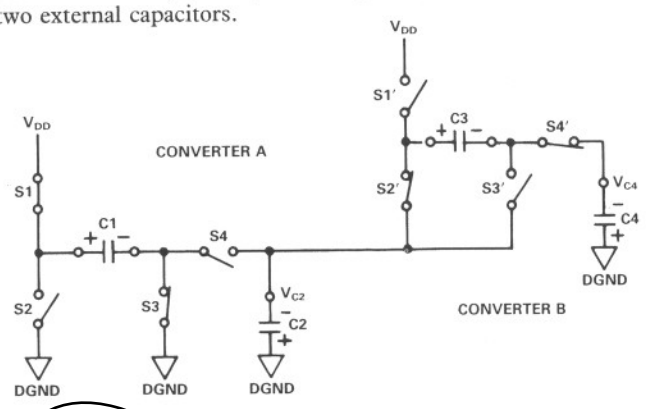


Figure 16. Converter Circuitry with External Capacitors Included

Consider initially converter A, switches S1 through S4, and capacitors C1 and C2. The oscillator and voltage-level translator sections provide the control signals to the four switches. During the charge phase, capacitor C1 is charged through S1 and S3 (S2 and S4 open) to a voltage equal to the supply voltage V_{DD}. In the pump phase, S2 and S4 are closed (S1 and S3 open) and the charge is pumped or transferred from capacitor C1 to C2. The voltage on C2 (V_{C2}, pins 5 and 13) is equal in value and opposite in polarity to $+V_{DD}$ with respect to DGND (assuming ideal switches and no load on C2). Since a finite time is required after power-on for the voltage to build up across C2 this discussion has assumed that steady state conditions have been reached.

Operation of the second converter is identical with the first except that capacitor C3 is now charged between $+V_{DD}$ and $-V_{DD}$.

This means that during the charge phase capacitor C3 will charge to $(+V_{DD}) - (-V_{DD})$ or $+2V_{DD}$. This voltage is then pumped to capacitor C4. The subsequent voltage on C4 (V_{C4}, pin 11) is ideally $3V_{DD}$ and is negative with respect to DGND. When the first converter is in the charge phase, the second is in the pump phase and vice versa. Converter timing is derived from an on-chip oscillator which can be free-running or synchronized with an externally applied clock.

Figures 3 and 4 in the Typical Performance section show output voltage vs. load current characteristics for converter A (V_{C2}) and converter B (V_{C4}) outputs respectively.

The reference portion of the AD7560 consists of an internal reference voltage circuit and an output buffer amplifier (see Figure 17). Both the reference circuit and the amplifier obtain their bias conditions from a bias controller which is powered by V_{C2} (converter A output) via an internal connection and from an externally applied negative voltage to V_{SS} (pin 10). The amplifier operating current is supplied from V_{DD} and V_{SS}. Normally the voltage output V_{C4} available on C4 (converter B output) is used as the V_{SS} supply. The reference voltage circuit, which is referenced to analog ground (AGND, pin 8), provides a stable temperature compensated $-5V$ reference voltage at the noninverting input of the buffer amplifier A1. R_{IN} and R_{FB} are two thin film resistors with nominal value of 50kΩ each. With R_{IN} (pin 7) tied to AGND and R_{FB} (pin 6) tied to the amplifier output V_{REF} (pin 9), the amplifier provides a noninverting gain of 2 for the internal reference. The amplifier thus supplies a precision reference

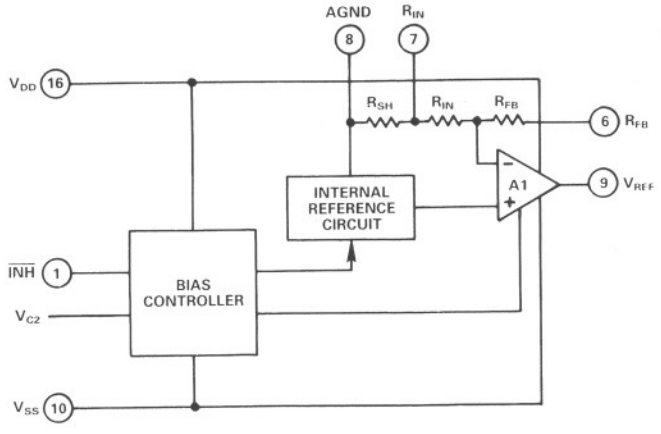


Figure 17. Reference Voltage Circuitry

voltage output of $-10V$ with a current sink capability of over 1.0mA. The R_{IN} pin is internally tied to AGND via a shunt resistor R_{SH} which is approximately equal to 1.5 R_{FB}.

The entire reference voltage circuitry can be powered down via the INHIBIT input ($\overline{INH}$, pin 1). This reduces current loading on V_{C2} and V_{C4} and results in increased conversion efficiency of both dc-to-dc converters. See Figure 10 under Typical Performance Characteristics.

TRIM TECHNIQUES

Normal lot-to-lot variations in fabrication will produce devices whose output reference voltages will be distributed symmetrically around $-10.00V$. With the addition of one fixed resistor and a potentiometer it is possible to adjust every device to provide a $-10.00V$ output (see Figure 18).

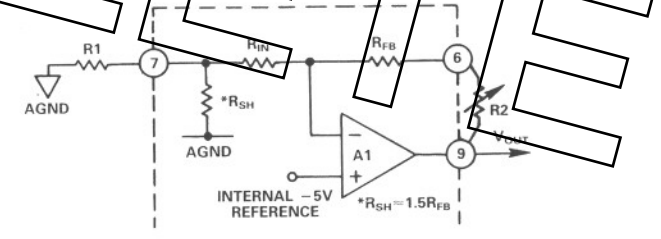


Figure 18. Trim Resistors for Reference Circuit

Trim Resistor	AD7560JN
R1 (Fixed)	10kΩ
R2 (Variable)	20kΩ

R1: thick film metal glaze, tolerance ±2%, T.C. ±100ppm/°C
R2: 20 turn cermet trimmer, tolerance ±10%, T.C. ±100ppm/°C

Table I. Recommended Trim Resistor Values

The fixed resistor R1 must be sufficiently large (when R2 = 0Ω) to ensure that the output reference voltage of any device is less than $-10.00V$. Potentiometer R2 is then increased from 0Ω until the reference voltage equals $-10.00V$. Worst case values of R1 and R2 are indicated in Table I and, therefore, represent the minimum values required which will ensure all devices can be properly trimmed.

In the absence of external gain trim components the output reference voltage is expressed as:

$$V_{REF} = -5 \times \left(1 + \frac{R_{FB}}{R_{IN}}\right) \text{Volts}$$

This reference voltage has a typical temperature coefficient (TC) of 40ppm/°C. The internal thin-film resistors R_{IN} and R_{FB} (and R_{SH}) have typical TCs of -300ppm/°C. However, their

matching and tracking is so tight as to produce no appreciable effect on the output TC.

The inclusion of external gain trim components R1 and R2 (as shown in Figure 18) modifies the overall reference performance since these external trim resistors will have different TCs from the internal thin-film resistors. The lowest values possible for R1 and R2 should be chosen in order to minimize their effect on the overall reference TC. To obtain the lowest possible reference TC the most suitable technique for reference trimming is a "select on test" approach to choosing R1 and/or R2 as opposed to potentiometer trimming.

Referring to Figure 18, if pins 6, 7 and 9 are connected together–omitting R1 and R2–amplifier A1 is configured as a unity gain buffer amplifier making the internal −5V reference available externally. However, the current loading capability of the V_{C4} output is not appreciably increased over normal −10V reference conditions.

OUTPUT VOLTAGE CALCULATION

Since the two converters (A and B), are driven in series, current loading on either of the two storage capacitors will reduce both output voltages, V_{C2} and V_{C4}, as well as the overall converter efficiency. An approximate equivalent circuit for the converter outputs is shown in Figure 19.

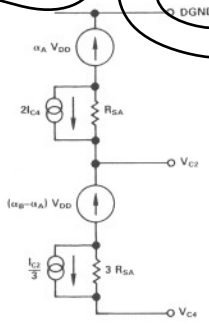


Figure 19. Equivalent Circuit for V_{C2}, V_{C4} Outputs (See Figure 1)

The output voltages using this equivalent circuit and under moderate current loads can be calculated as follows:

$$V_{C2} = -\alpha_A V_{DD} + I_{C2} R_{SA} + 2 I_{C4} R_{SA}$$

$$V_{C4} = -\alpha_B V_{DD} + 2 I_{C2} R_{SA} + 6 I_{C4} R_{SA}$$

Where: α_A is converter A conversion factor, typically $\alpha_A = 0.95$

$$\alpha_A = \frac{|V_{C2}|}{V_{DD}}$$

α_B is converter B conversion factor, typically $\alpha_B = 2.90$

$$\alpha_B = \frac{|V_{C4}|}{V_{DD}}$$

I_{C2} = External current load on C2

I_{C4} = External current load on C4

R_{SA} = Converter A output source resistance
$R_{SA} = 120\Omega$ typically.

If only converter B output is loaded the previous expression simplifies to:

$$V_{C4} = -\alpha_B V_{DD} + 6 I_{C4} R_{SA}$$

which is the analysis of a voltage source, $\alpha_B V_{DD}$, with an output impedance of $6R_{SA}$. Refer to the relevant current-voltage characteristics shown under Typical Performance Characteristics.

VOLTAGE CONVERSION EFFICIENCY

The efficiency of the dc-to-dc converters depends upon the switching transient losses which occur during the conversion cycles.These losses increase with increasing supply voltage V_{DD} and with increasing oscillator frequency f_{CLK}. Figure 13 shows typical power supply current I_{DD} vs. power supply voltage V_{DD} for different values of clock capacitor. The choice of values for the pump and reservoir capacitors for both converters depends primarily on the required output current loading and the peak-to-peak output voltage ripple. The AD7560 is specified with C1 = C2 = C3 = C4 = 10μF and a clock frequency of 6kHz as per the test circuit of Figure 1. The efficiency is relatively constant and optimal over a clock frequency range from 2kHz to 20kHz as indicated in Figure 12 which shows the converter output voltages as a function of clock frequency with fixed values for C1 to C4. If maximum efficiency is required at clock frequencies other than 6kHz, then the value of the pump and storage capacitors must be changed to ensure that the capacitive load impedances remain constant, i.e., if the clock frequency is reduced from 6kHz to 600Hz (a reduction of 10) then C1 to C4 values should be increased by 10 (from 10μF to 100μF). Note that the pump frequency is always one half the clock frequency at pin 15.

CLOCK FREQUENCY CONTROL

The conversion cycle time (charge and pump phases) of the dc-to-dc converters may be derived from the on-chip oscillator or else controlled by an externally applied clock signal.

1. External Clock Capacitor: When the clock input (CLK, pin 15) of the AD7560 is left open circuit, the internal oscillator runs at a typical rate of 50kHz. This frequency is lowered by connecting an external capacitor between CLK and V_{DD} or between CLK and DGND.
2. External Clock Signal: The internal oscillator can be over-ridden by an externally applied clock signal. The clock input of the AD7560 is 5V CMOS compatible and sources or sinks typically 15μA of input current. The mark/space ratio of the external clock can be highly asymmetric; minimum clock HIGH level (or LOW level) requirement is 5μs. The conversion phases change state on the negative going edge of the clock signal.

INHIBIT INPUT

As mentioned in the Circuit Description section, the reference and amplifier circuitry of the AD7560 obtains bias and operating current from the converter outputs–internally from converter A and externally (via V_{SS}) from converter B. This total current load is constant and is typically 3.5mA. Note that this 3.5mA includes any reference current that the reference amplifier sinks. In applications where the reference output voltage is not required, this current load can be reduced to negligible values by applying a logic LOW to the inhibit input ($\overline{INH}$, pin 1). The effect of the inhibit control on voltage conversion efficiency is evident from the performance characteristics as shown in Figure 10.

INTERNAL CIRCUIT PROTECTION

Referring to Figure 16, the MOS switches of both converters, S3, S4 and S3′, S4′ are N-channel devices. During normal

charge and pump cycles and also during power-up and output short circuit conditions (see following section), the voltages on the sources and drains of these output transistors vary in amplitude and polarity. To ensure optimum transistor performance (i.e., low R_{ON} and substrate reverse biased with respect to source) under any condition, their substrates must be tied to the most suitable negative potential available. To achieve this, a section of the internal control logic is devoted to sensing the voltages on the transistor sources and drains, and ensuring that their substrates are always correctly biased. This technique prevents the AD7560 from latching up during power-up and overload conditions, and also ensures optimum efficiency of both dc-to-dc converters.

OPERATION AT HIGH VOLTAGES AND ELEVATED TEMPERATURES

Under normal specified conditions, the AD7560 operates efficiently over its full temperature and supply voltage ranges. If any one of the external capacitors short circuits or if the V_{C2} or V_{C4} output is shorted to any low impedance point (e.g., V_{DD} or DGND) the AD7560 internal protection circuitry mentioned previously acts to prevent SCR action and to avoid device destruction. If the AD7560 is to operate under a combination of temperature/supply voltage conditions, as shown in the shaded areas of Figure 15, then external protection circuitry is required both to ensure device operation and, in the event of a short circuit occurring, to preclude device destruction.

Figure 20 shows the protection circuitry required when operating in the dotted area of Figure 15. Due to the inclusion of R1 in series with the V_{C2} output on pin 5, the V_{C2} output on pin 13 should not be used.

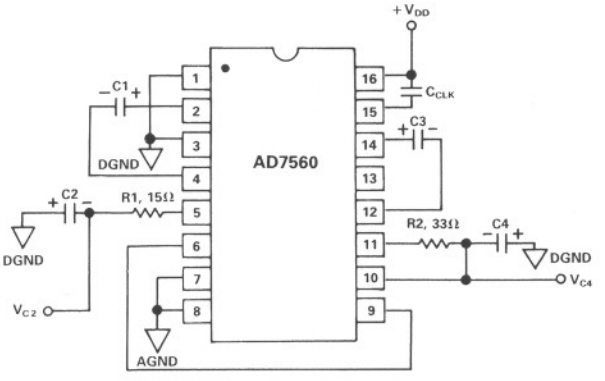


Figure 20. Location of Protection Components R1, R2 Required for Operation in Shaded Area of Figure 15

Figure 21 shows the protection circuitry required when operating in the lined area of Figure 15. Under these conditions of high temperature/high voltage, if the V_{C2} or V_{C4} output is shorted to V_{DD}, then internal parasitic transistors may be turned on leading to SCR action and possible device destruction. Diodes D1 and D2 ensure that the V_{C2} and V_{C4} outputs are never pulled higher than a diode drop above DGND. Note that these diodes will require current limiting protection via the R_{LIMIT} series resistors.

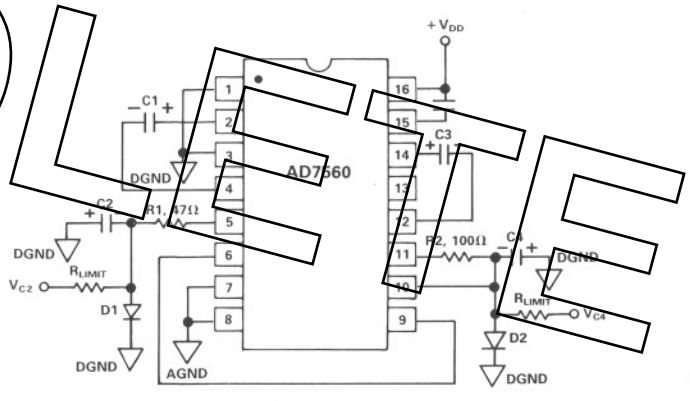


Figure 21. Location of Protection Components R1, R2 and D1, D2 Required for Operation in Lined area of Figure 15

Note that none of the above external protection is required when operating the AD7560 within specified limits of $+4.5 \leq V_{DD} \leq +5.5V$ at any temperature over its $-25°C$ to $+70°C$ range.

The AD7560 can be used in a multitude of configurations to suit different requirements and applications. Table II outlines some of these operating configurations.

Figure	Input Voltage	Nominal Output Voltages
22	+5V	−5V
23	+5V	−5V, −15V
24	+5V	−5V, −15V, −10V Reference
25	+5V	−5V, +10V
26	+5V	−5V, +15V
27	+5V	−5V, −15V, +10V
28	+5V	−5V, −15V, +15V
29	+5V	−5V, −15V, +10V, −10V Reference
30	+5V	−5V, −15V, +15V, −10V Reference

Table II. Typical AD7560 Operating Configurations

$+V_{DD}$ In, $-V_{DD}$ Out (Figure 22)
Figure 22 shows the circuitry required for single voltage conversion. C1 and C2 are standard 10μF/10V electrolytic capacitors. See Figure 3 for typical performance characteristics.

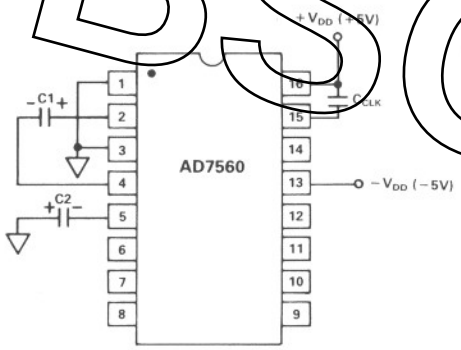


Figure 22. $+V_{DD}$ to $-V_{DD}$

$+V_{DD}$ In, $-V_{DD}$, and $-3V_{DD}$ Out (Figure 23)
Figure 23 shows the circuitry required for voltage conversion and negative voltage multiplication. Capacitors C1 and C2 are 10μF/10V, capacitors C3 and C4 are 10μF/25V. All are standard low cost electrolytic types. Typical performance characteristics are shown in Figure 4.

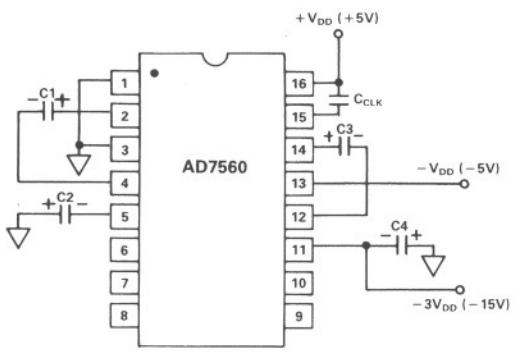


Figure 23. $+V_{DD}$ to $-V_{DD}$ and $-3V_{DD}$

$+V_{DD}$ In, $-V_{DD}$, $-3V_{DD}$ and $-10V$ Reference Out (Figure 24)
To allow the voltage reference circuit to operate, the inhibit input ($\overline{INH}$, pin 1) is tied to V_{DD}. The feedback loop of the internal buffer amplifier is closed by tying R_{FB} (pin 6) to V_{REF} (pin 9). The amplifier input resistance R_{IN} (pin 7) is tied to AGND (pin 8) to provide a gain of +2 for the internal −5V reference (see Figure 24).

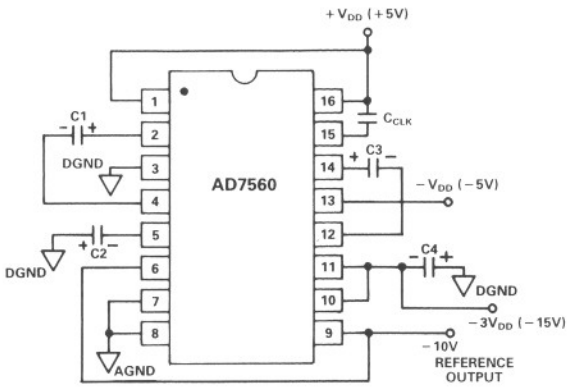


Figure 24. $+V_{DD}$ to $-V_{DD}$, $-3V_{DD}$ and $-10V$ Reference Output

$+V_{DD}$ In, $-V_{DD}$, $+2V_{DD}$ Out (Figure 25)
Positive voltage multiplication is possible using a diode pump scheme as shown in Figure 25. In this configuration, the input capacitor (C5) of the diode pump is switched between $+V_{DD}$ and DGND by the action of converter A. During its pump phase (pin 2 at AGND) C5 is charged to $+V_{DD} - V_F$ (where V_F is the forward diode drop of D1.) During the charge phase (pin 2 at $+V_{DD}$) the voltage on C5 plus the supply voltage is applied through D2 to capacitor C6. Thus the output voltage on C6 is $+2V_{DD} - 2V_F$.

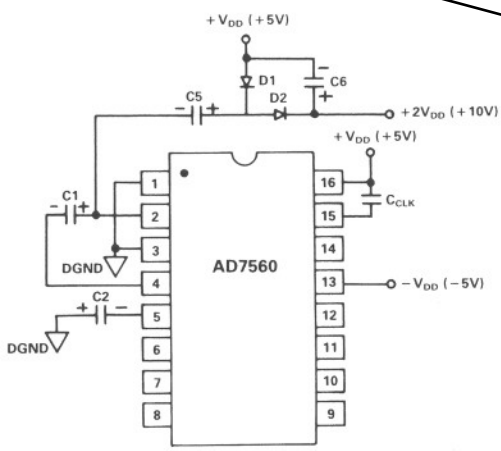


Figure 25. $+V_{DD}$ to $-V_{DD}$ and $+2V_{DD}$

$+V_{DD}$ In, $-V_{DD}$, $+3V_{DD}$ Out (Figure 26)
In this configuration, multiplication of $+V_{DD}$ to $+3V_{DD}$ is achieved by switching the input of the diode pump capacitor (C5) between $+V_{DD}$ and V_{C2}. During the pump phase of converter B capacitor C5 is charged to $+V_{DD} + V_{C2} - V_F$ (where V_F is the forward diode drop of D1). During the charge phase the voltage on C5 plus the supply voltage is applied through diode D2 to capacitor C6. The output voltage on C6 is thus $2V_{DD} + V_{C2} - 2V_F$. Capacitors C5 and C6 are 10μF/25V.

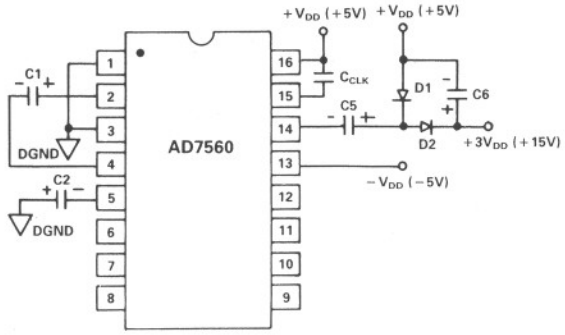


Figure 26. $+V_{DD}$ to $-V_{DD}$ and $+3V_{DD}$

$+V_{DD}$ In, $-V_{DD}$, $-3V_{DD}$ and $+2V_{DD}$ Out (Figure 27)
This configuration uses both converters and a diode pump. Driving the diode pump input capacitor from +C1 (pin 2) provides positive voltage doubling as explained in conjunction with Figure 25.

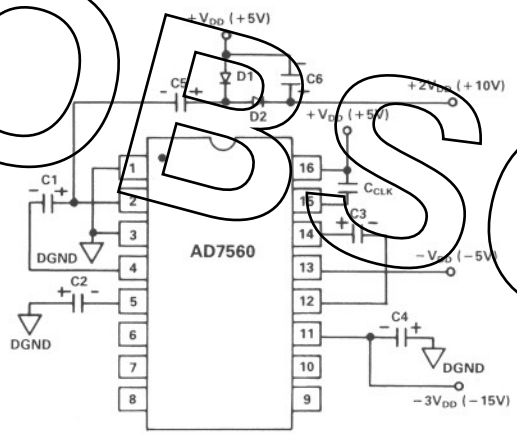


Figure 27. $+V_{DD}$ to $-V_{DD}$, $+3V_{DD}$ and $+2V_{DD}$

$+V_{DD}$ In, $-V_{DD}$, $-3V_{DD}$ and $+3V_{DD}$ Out (Figure 28)
This circuit is similar to Figure 27 except that the diode pump is now driven from +C3 (pin 14). This provides voltage trebling as explained in conjunction with Figure 26.

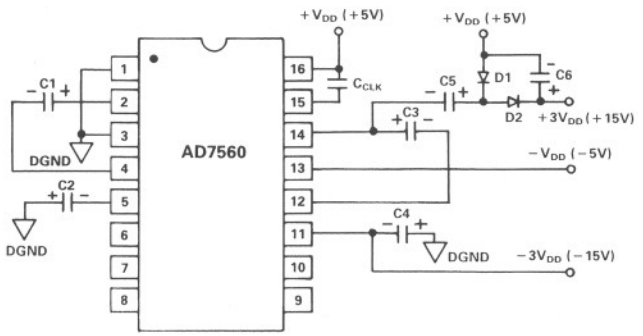


Figure 28. $+V_{DD}$ to $-V_{DD}$, $-3V_{DD}$ and $+3V_{DD}$

$+V_{DD}$ In, $-V_{DD}$, $-3V_{DD}$, $+2V_{DD}$ and $-10V$ Reference Out (Figure 29)
The configuration shown in Figure 29 uses both converters, reference circuit and diode pump to provide multiple analog outputs.

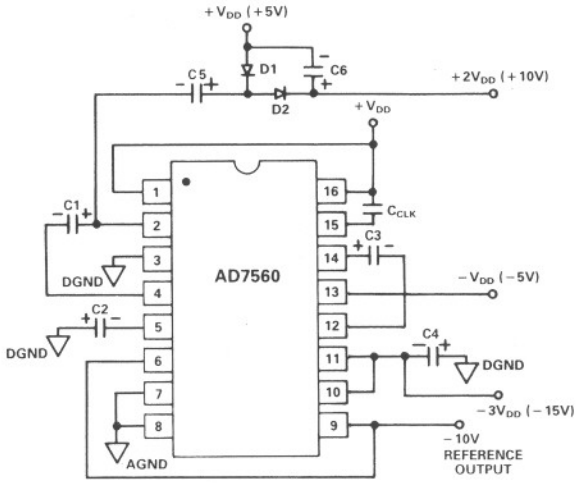


Figure 29. $+V_{DD}$ to $-V_{DD}$, $-3V_{DD}$ and $+2V_{DD}$ and $-10V$ Reference Output

$+V_{DD}$ In, $-V_{DD}$, $-3V_{DD}$, $+3V_{DD}$ and $-10V$ Reference Out (Figure 30)
This circuit is similar to Figure 29 except that the diode pump is now driven from +C3 (pin 14) to provide positive voltage trebling (see Figure 30).

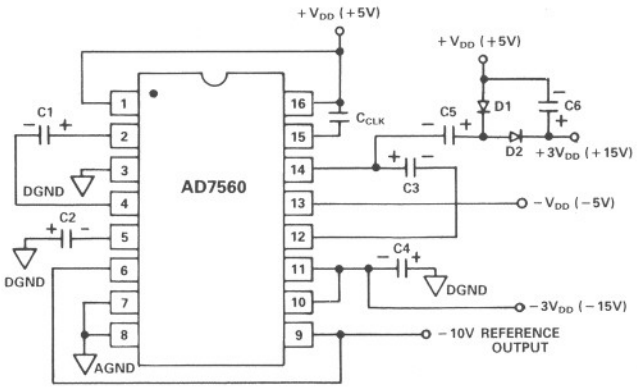


Figure 30. $+V_{DD}$ to $-V_{DD}$, $-3V_{DD}$ and $+3V_{DD}$ and $-10V$ Reference Output

INCREASING OUTPUT CURRENT CAPABILITY

It is possible to run two or more AD7560s in parallel to reduce the output resistance of both V_{C2} and V_{C4}. Figure 31 shows the circuit connections. Each converter has its own pump capacitor while the respective storage capacitors are common. The resultant output resistance of either converter A or converter B is approximately equal to that of a single device divided by the number of devices paralleled.

Each AD7560 in Figure 31 is shown with an individual clock capacitor. Thus each device runs independently at a different conversion frequency leading to increased noise in the reference voltage output. To reduce the generated noise to a minimum drive all CLK inputs in parallel from a common clock signal.

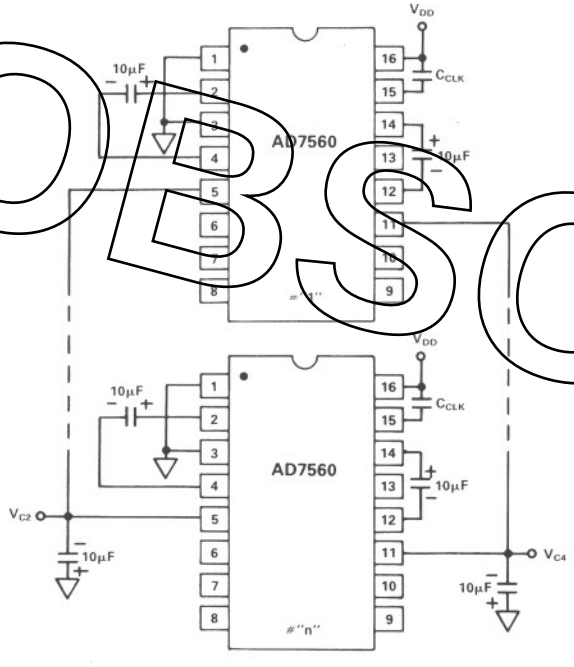


Figure 31. Paralleling Devices to Increase Output Current Capability

The reference voltage output can also benefit from the paralleling of devices. Figure 32 shows how the final AD7560 (e.g., device # "n" in Figure 31) should be connected to boost the available reference current. For example, with two devices in parallel the typical reference current is increased to over 5mA.

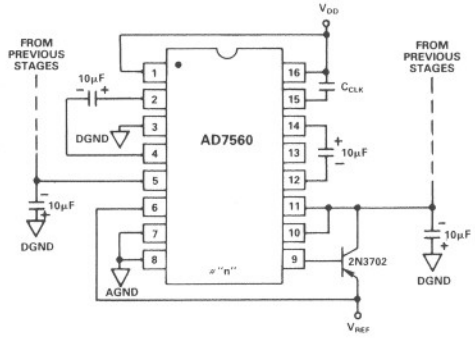


Figure 32. Reference Current Boosting

Note that this reference current boosting technique may also be used with existing −12V to −15V power supplies. Using the single general purpose PNP transistor as indicated in Figure 32 and an existing −12V power supply, one AD7560 can control up to 200mA of reference current (see Figure 33).

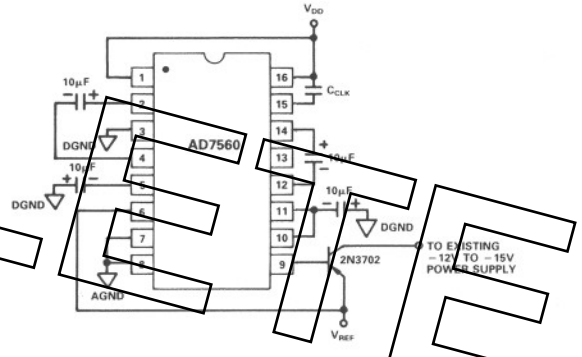


Figure 33. Reference Current Boosting Using Existing −12V to −15V Power Supply