ANALOG DEVICES

AN-292
APPLICATION NOTE

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Interfacing the AD7572A to High-Speed DSP Processors

by John Reidy

The AD7572A is a complete 12-bit CMOS analog-to-digital converter, with a conversion time of 3μs (7572AXX03) or 10μs (7572AXX10). An on-chip, buried Zener diode provides a stable reference voltage to give low drift performance over the full temperature range. An on-chip clock circuit is provided, which may be used with a crystal/ceramic resonator or an external clock source such as a divided-down microprocessor clock. The only other external components required for basic operation of the AD7572A are decoupling capacitors for the supply voltages and reference output.

The AD7572A is designed to interface with microprocessors as a memory-mapped device. Interface timing is sufficiently fast to allow the AD7572A to support today's most popular microprocessors. The more advanced processors such as the TMS32020 from Texas Instruments or ADSP-2100 from Analog Devices demand faster data access times than the AD7572A can meet when operating at their maximum clock frequency. This note addresses the problem of interfacing the AD7572A to such high performance processors.

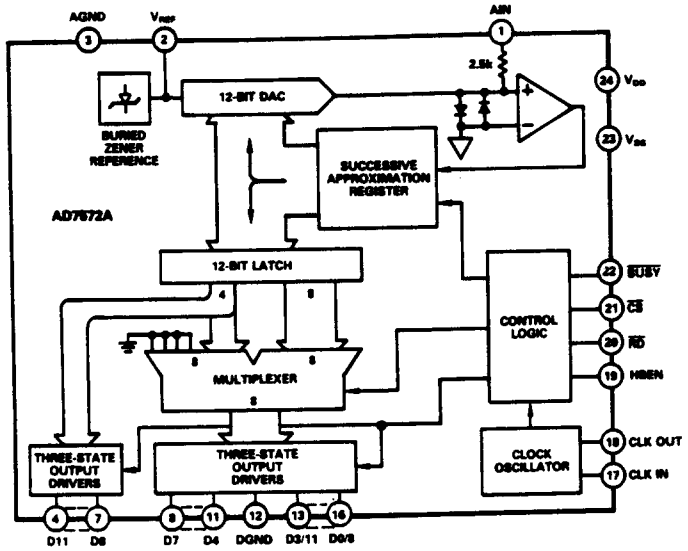

Figure 1. AD7572A Functional Block Diagram

THE USE OF WAIT STATES

A useful feature when interfacing ADCs to high speed microprocessors is a WAIT state input. This feature simplifies the hardware required for slow memory devices by extending the microprocessor bus access time, thereby, accommodating slower data access times. An example is the AD7572A/TMS32020 interface of Figure 2. One WAIT state (i.e., one clock cycle) is added to the microprocessor bus timing during an ADC data read cycle.

The AD7572A is mapped at a port address. The following I/O instruction both starts a conversion and reads the previous conversion result into a data memory location.

IN A, PA (PA = PORT ADDRESS)

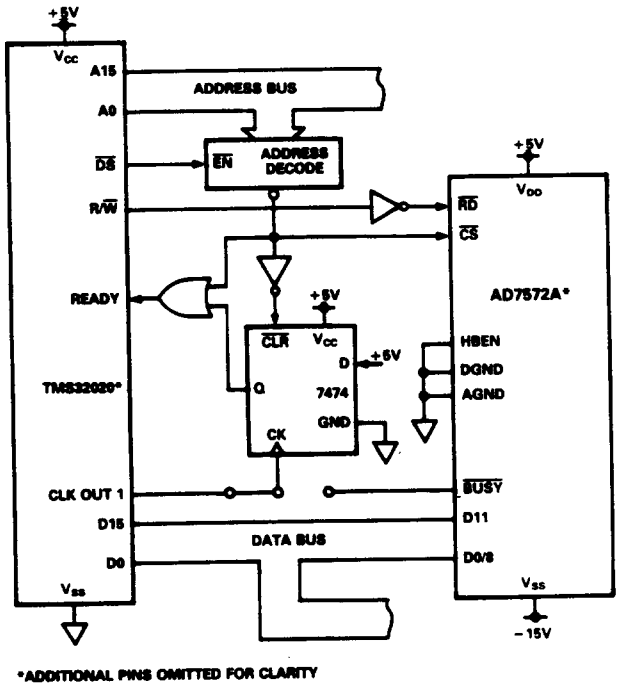

Figure 2. AD7572A/TMS32020 Interface Using WAIT States

If the previous conversion result is too old, then more up-to-date data may be read when conversion is complete. A delay at least as long as the ADC conversion time must be allowed between read operations. Note, this interface is not meant specifically for the TMS32020. It works equally as well for the ADSP-2100 or any other processor that has the same WAIT state input configuration.

The interface of Figure 2 is designed to extend the ADC data read cycle by just one WAIT state (i.e., one clock cycle or 200ns for a 20MHz TMS32020 clock input). The circuit can be easily modified to extend the ADC read cycle by the AD7572A conversion time. This is done by driving the 7474 clock input from the AD7572A $\overline{BUSY}$ output rather than the TMS32020 CLK OUT1. In this way once a conversion has started the TMS32020 READY input does not get asserted until the AD7572A conversion is complete. Stopping the microprocessor for the entire ADC conversion is costly in processing time, but it does have the advantage of reducing microprocessor noise.

MICROPROCESSOR NOISE

High resolution ADCs, like the AD7572A, are sensitive to the noisy environments created by high speed microprocessors. Careful attention should be given to a PCB layout and power supply decoupling. A continuously active microprocessor bus can cause LSB errors in the conversion results. These errors are due to feedthrough from the microprocessor to the ADC comparator. The problem of microprocessor noise can be eliminated by using WAIT states for the duration of the ADC conversion time as suggested in the AD7572A/TMS32020 interface. Alternatively three-state buffers can be used to isolate the ADC data bus as shown in the ADSP-2100 interface of Figure 3.

EQUAL SAMPLING INTERVALS

In Digital Signal Processing, and many other applications, it is important that the signal sampling occurs at exactly equal intervals. This is to avoid errors due to sampling uncertainty or jitter. Trying to achieve precise timing with a microprocessor necessitates counting clock cycles and calculating software loop delays. This is especially difficult in interrupt driven systems where there is uncertainty in interrupt servicing delays. A preferred solution is to use an external timer to provide conversion control. Such timers can be software programmable like the 8254 from Intel or a simple counter as shown in the AD7572A/ADSP-2100 interface of Figure 3.

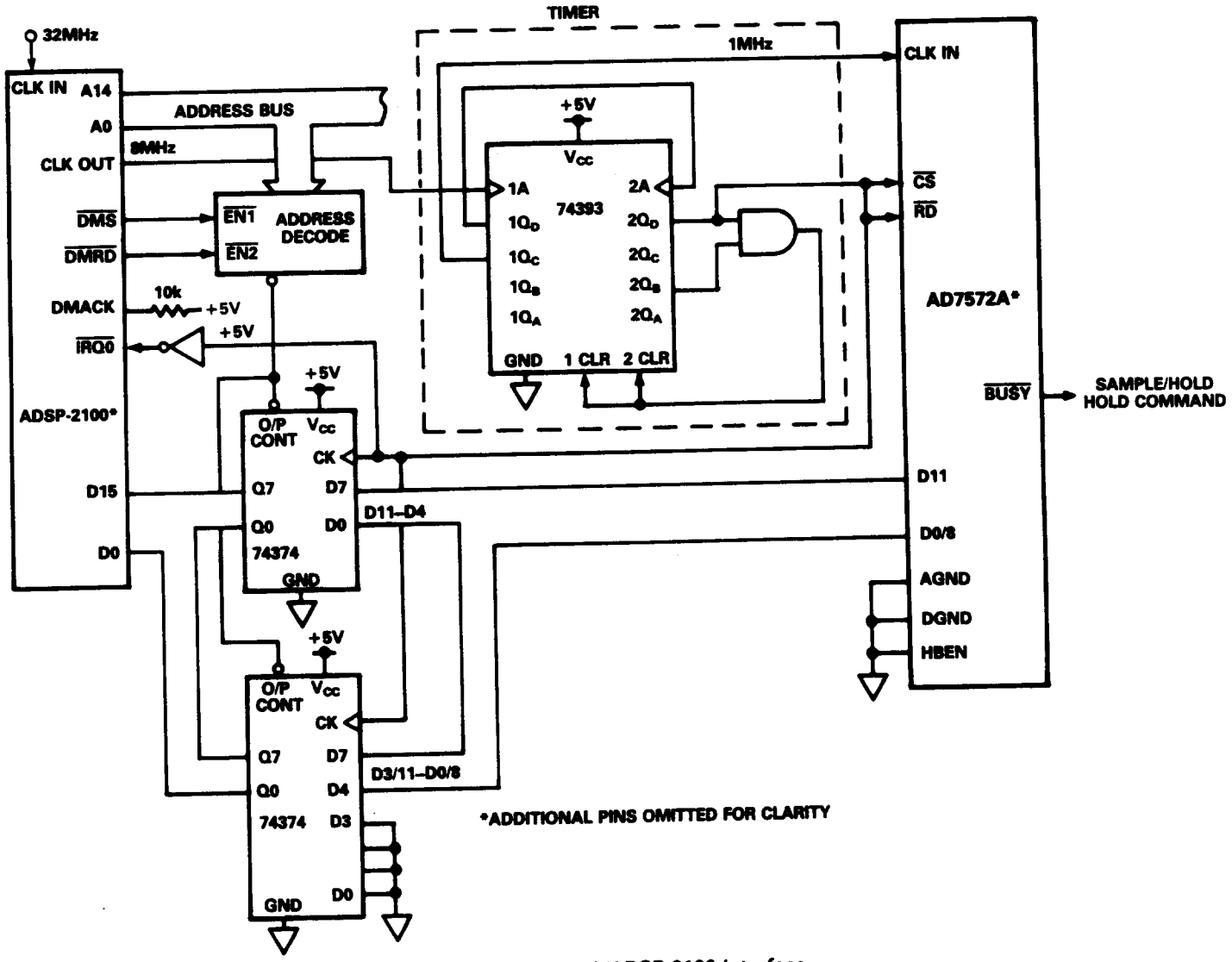

Figure 3. AD7572A/ADSP-2100 Interface

AD7572A-ADSP2100 INTERFACE

The 74393 timer counter of Figure 3 uses the ADSP-2100 CLK OUT to generate an AD7572A CLK IN and provide accurate conversion control. With an ADSP-2100 CLK IN of 32MHz, CLK OUT is 8MHz – the counter is configured so that it starts a conversion every 160 CLK OUT cycles resulting in a sampling rate of 50kHz (see Figure 4 timing diagram). An AD7572A conversion starts when the timer takes $\overline{CS}$ and $\overline{RD}$ inputs low.

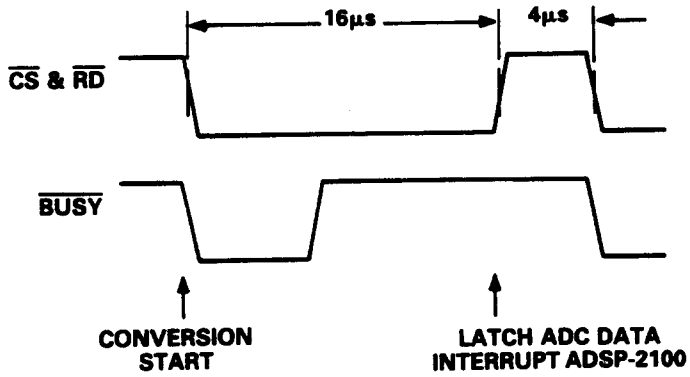

Figure 4. AD7572A/DSP-2100 Timing Diagram

The converter acknowledges by taking $\overline{BUSY}$ low, which asserts the HOLD input of the Sample-and-Hold amplifier (not shown in Figure 3) for the duration of the conversion. $\overline{CS}$ and $\overline{RD}$ remain low for 16µs; the rising edge of $\overline{CS}$ and $\overline{RD}$ latches the conversion result into the 74374 latches and interrupts the ADSP-2100 processor. The interrupt input is set to be edge sensitive during program initialization, so that it does not have to be reset during the interrupt service routine. The following single load instruction in the interrupt service routine reads the ADC data into the MR0 data register.

MR0 = DM (ADC ADDRESS)

The AD7572A data bus of Figure 3 is connected so that the conversion result is placed at the MSB end of the 16-bit MR0 register (i.e., D15-D4). This suits the internal left-justified fractional data format of the ADSP-2100. The same does not apply for all processors; for instance, right-justified data would probably be more suitable for the TMS32020. This allows for word extension in the event of an overflow when adding or multiplying.

Again, the interface of Figure 3 is not specific to the ADSP-2100, it is suitable for practically every processor available today. It has the advantage of allowing the processor to operate at maximum speed while the AD7572A performs conversions at constant sampling intervals.