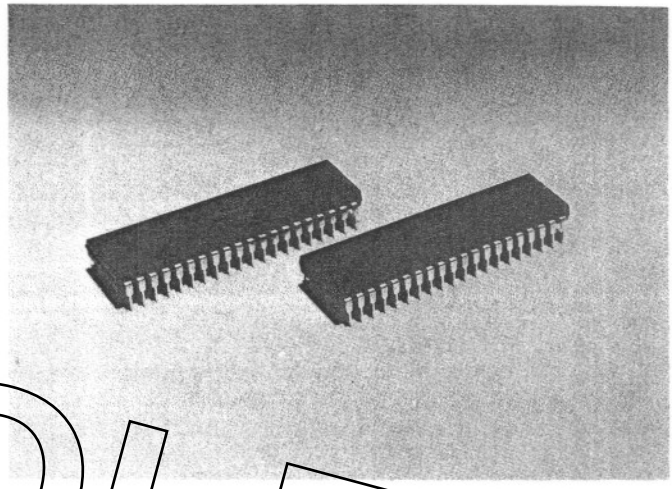
CMOS Single Supply, 9-Channel, 8-Bit ADC

AD7583

PRELIMINARY TECHNICAL DATA

FEATURES

- 8-Bit Resolution and Accuracy
- 9-Channel Analog Input (Expandable)
- Single Supply +5V to +15V Operation
- Easily Interfaced to Most μP's via an I/O Port
- Low Power Consumption
- Ratiometric
- TTL/CMOS Compatible



GENERAL DESCRIPTION

The AD7583 is a monolithic CMOS, 9-channel (expandable), 8-bit A/D converter designed for single supply operation (+5V to +15V), making it highly suited to battery operation. It provides accuracy with stability using a patented integrating technique (ADI patent No. 3872466) called "quad slope".

Most applications require the addition of only a few passive components and two general purpose operational amplifiers.

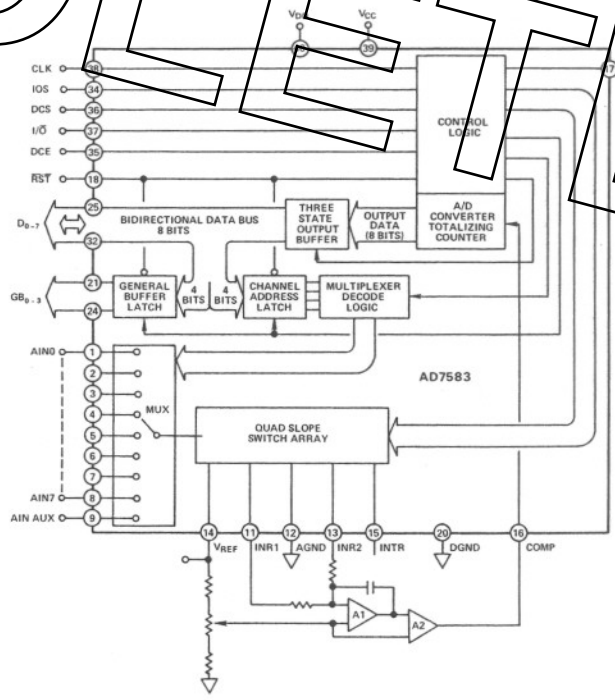
Digital information (channel address input, converted output data) is passed to and from the AD7583 via an 8-bit bidirectional I/O bus under command of control signals I/$\overline{O}$ (Input/Output) and IOS (IO Strobe).

The A/D converter responds to analog inputs ranging from $0.15V_{REF}$ to $0.85V_{REF}$. In single supply applications, this precludes the necessity for signal conditioning circuitry whose output swings to the supply rails. It also facilitates connection to ratiometric transducers whose zero output may not be at "true zero".

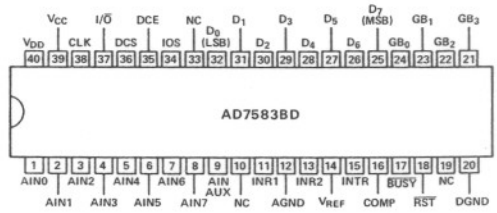
Direct TTL input/output interface is provided when V_{CC} = +5V. Putting V_{CC} equal to the CMOS logic supply voltage provides CMOS compatibility.

Single supply operation, low power consumption and easy hardware interface to μP's make the AD7583 useful in a wide variety of data-acquisition and process-control applications.

FUNCTIONAL DIAGRAM



PIN CONFIGURATION



ORDERING INFORMATION

Model	Temperature Range	Package
AD7583KN	0 to +70°C	40 pin plastic DIP

Route 1 Industrial Park; P.O. Box 280; Norwood, Mass. 02062
Tel: 617/329-4700 TWX: 710/394-6577
West Coast 714/842-1717 Mid-West 312/894-3300 Texas 214/231-5094

SPECIFICATIONS

($V_{REF} = V_{DD} = 12V$, $V_{CC} = 5V$, $f_{CLK} = 1.28MHz$, $R_1 = R_2 = 2M\Omega$, $R_3 = R_4 = 10k\Omega$, $C_1 = 0.001\mu F$ unless otherwise noted. Amplifier A_1 has input error less than 1.4% of V_{REF}. See page 6, Selecting an Integrator Amplifier).

PARAMETER	$T_A = 25°C$	$T_A = T_{min}/T_{max}$	UNITS	CONDITIONS	COMMENTS
ACCURACY					The AD7583 rounds down to the nearest integer value. At reduced V_{DD} typical values for Relative Accuracy, Full Scale Error and Zero Scale Error are: For $9 \leqslant V_{DD} \leqslant 15$, ±1 count; for $7 \leqslant V_{DD} \leqslant 9$, ±2 counts; for $5 \leqslant V_{DD} \leqslant 7$, ±4 counts.
Resolution	8	8	Bits		
Relative Accuracy	±1	±1	Counts max		
Differential Nonlinearity	±1	±1	Counts max		
Full Scale Error	±1	±1	Counts max	AIN = $0.85V_{REF}$	
Zero Scale Error	±1	±1	Counts max	AIN = $0.15V_{REF}$	
TRANSFER FUNCTION	Straight unipolar binary see Table 2. Zero scale output (00000000) at AIN $\leqslant 0.15V_{REF}$ Full scale output (11111111) at AIN $\geqslant 0.85V_{REF}$				
MULTIPLEXER					
R_{ON}	2	2	kΩ max	$0.15V_{REF} \leqslant AIN \leqslant 0.85V_{REF}$	
$\Delta R_{ON}/AIN$[1]	30	30	% typ		
Switch Leakage[1]	±1	±1	μA max	Multiplexer 'common' at GND Multiplexer input at V_{DD}	
LOGIC INPUTS (CLK, IOS, DCS, I/$\overline{O}$, DCE, RST, D_{0-7})					
V_{INH} (Logic High Input)	2.4	2.4	V min	V_{CC} = 5V	
	11.5	11.5	V min	V_{CC} = 12V	
V_{INL} (Logic Low Input)	0.8	0.8	V max	V_{CC} = 5V	
	0.5	0.5	V max	V_{CC} = 12V	
I_{IN} (all logic inputs except D_{0-7})	5	5	μA max	V_{IN} = 0, 5V, 12V	
I_{IN} (Logic inputs D_{0-7})	5	5	μA max	V_{IN} = 0, 5V, 12V measured when 3-state bus is disabled.	
C_{IN} (Input Capacitance)[2]	8	8	pF typ		
LOGIC OUTPUTS (D_{0-7}, $\overline{BUSY}$, GB_{0-3})					
V_{OH} (Logic High Output)	2.8	2.8	V min	V_{CC} = 5V I_{SOURCE} = 40μA	
	11.5	11.5	V min	V_{CC} = 12V I_{SOURCE} = 0.6mA	
V_{OL} (Logic Low Output)	0.4	0.4	V max	V_{CC} = 5V I_{SINK} = 1.6mA	
	0.5	0.5	V max	V_{CC} = 12V I_{SINK} = 1.0μA	
I_L, 3-State Output Leakage	10	10	μA max		
POWER SUPPLY CURRENT					
I_{CC} (V_{CC} Supply Current)	2	2	mA max	f_{CLK} = 1.28MHz	
I_{DD} (V_{DD} Supply Current)	20	20	mA max		
DYNAMIC PERFORMANCE[3]					
Conversion Time	4	4	ms max	f_{CLK} = 1.28MHz	See "Conversion Time" Page 6
f_{CLK}	1.28	1.28	MHz max		
t_{BSIO}	1100	1100	ns min		$\overline{BUSY}$ to IOS Set Up Time Figure 6
t_{IOS}	500	500	ns min		IOS Pulse Width Figure 6
t_{AD}	650	650	ns min		Data Access Time Figure 6
t_{HD}	300	300	ns max		Data Hold Time Figure 6
t_{IO}	1200	1200	ns min		I/$\overline{O}$ Pulse Width Figure 5
t_{WOS}	500	500	ns min		I/$\overline{O}$ Setup Time Figure 5
t_{WOH}	200	200	ns min		I/$\overline{O}$ Hold Time Figure 5
t_{DS2}	200	200	ns min		Data Setup Time Figure 5
t_{DH2}	200	200	ns min		Data Hold Time Figure 5
t_{IDPD}	1450	1450	ns max		IOS to BUSY Propagation Delay Figure 5
t_{IGPD}	650	650	ns max		IOS to General Buffer Latched Delay Figure 5
t_{DCE}	750	750	ns min		DCE Pulse Width Figure 4
t_{DDS}	250	250	ns min		DCE Setup Time
t_{PCS}	500	500	ns min		DCS Pulse Width
t_{DDH}	0	0	ns min		DCE Hold Time
t_{DSI}	200	200	ns min		Device Address Setup Time
t_{DHI}	500	500	ns min		Device Address Hold Time

PRICE	
AD7583KN	
(1–24)	$26.50
(25–99)	$21.00
(100's)	$17.50

[1] Typical values not guaranteed or subjected to production test.
[2] Guaranteed not tested.
[3] AC parameters sample tested at +25°C to ensure specification compliance.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

V_{DD} to DGND . . . . . 0V, +17V
V_{CC} to DGND . . . . . .0V, V_{DD}
Digital Input Voltage to DGND
CLK, IOS, DCS, I/$\overline{O}$, DCE, $\overline{RST}$ . . . . . .–0.3V, V_{CC}
Digital Output Voltage to DGND
$\overline{BUSY}$, GB_{0-3} . . . . . .–0.3V, V_{CC}
I/O Bus (D_{0-7}) to DGND. . . . . .–0.3V, V_{CC}
AGND to DGND. . . . . .–0.3V, V_{DD}
Analog Inputs/Outputs to AGND
COMP, AIN0 – AINAUX, V_{REF}, INTR, INR1 INR2
. . . . . .–0.3V, V_{DD}
Power Dissipation (Package)
Up to +50°C. 1000mW
Derates Above +50° by. . . . . 10mW/°C
Storage Temperature . . . . . –65°C to +150°C
Lead Temperature (soldering, 10s) . . . . . +300°C
Operating Temperature Range . . . . . –25°C to +85°C

CAUTION:
ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

PIN FUNCTION DESCRIPTION

PIN	MNEMONIC	FUNCTION
1	AIN0	Analog Input Channel 0
2–8	AIN1–AIN7	Analog Input Channels 1–7
9	AIN AUX	Auxiliary Analog Input – Can be used for channel expansion as shown in Figure 8.
10	NC	Not Connected
11	INR1	Integrator Resistor 1 (see Figure 7)
12	AGND	Analog Ground
13	INR2	Integrator Resistor 2 (see Figure 7)
14	V_{REF}	Reference Voltage Input. The reference voltage must be a positive voltage $\leq V_{DD}$.
15	INTR	Integrator reset pin, normally should be connected to AGND.
16	COMP	Input to AD7583 from output of the external comparator (A2 in Figure 7)
17	$\overline{BUSY}$	Status Output. When HIGH, indicates conversion is complete and that data can be read-out.
18	$\overline{RST}$	RESET Input (active low); resets control logic, general buffer latch, channel address latch, and device enable latch.
19	NC	Not Connected
20	DGND	Digital Ground
21–24	GB_3–GB_0	General Buffer Outputs. When writing a channel address (and convert start command), data at D_{4-7} is strobed into the general buffers on the positive edge of IOS. (D_4 is latched into GB_0, D_5 into GB_1, D_6 into GB_2 and D_7 into GB_3)
25	D_7	I/O Bus (MSB)
26–31	D_{6-1}	I/O Bus
32	D_0	I/O Bus (LSB)
33	NC	Not Connected
34	IOS	I/O Strobe Input. If the device enable latch is *SET* and I/$\overline{O}$ is High, analog channel address data on D_{0-3} is latched into the channel address latch on the positive edge of IOS. The phase 0 integration cycle begins within 1 clock period *after* the leading edge of IOS. If the device enable latch is *SET*, if $\overline{BUSY}$ is HIGH and if I/$\overline{O}$ is LOW; the 3-state output buffers are activated, placing converted data on D_{0-7} during the time IOS is held HIGH.
35	DCE	Decode Enable Input. If DCE is HIGH, and if code XXX11001 is placed on D_{0-7}, strobing DCS *SETs* the Device Enable Latch. If DCS is strobed when DCE is LOW, the device enable latch is *RESET*.
36	DCS	Decode Strobe Input. See DCE above.
37	I/$\overline{O}$	I/O control input. When I/$\overline{O}$ is HIGH, the AD7583 is in a data Input mode (write channel address and convert start). When I/$\overline{O}$ is LOW, the AD7583 is in a data Output mode (data READ).
38	CLK	Clock Input
39	V_{CC}	Logic Supply Input, range +5V to V_{DD}. For TTL output levels, put V_{CC} = +5V.
40	V_{DD}	Main Supply input, range +5V to +15V.

A/D CONVERTER OPERATION

Figures 1 and 2 show the basic converter circuit and its corresponding timing diagram. The inputs AGND (Analog GrouND), V_{REF} (Voltage REFerence) AIN (Analog INput) and INTR (INTegrator Reset) are applied to the integrator via switches 1 to 6, creating two reset phases (phases 0 and 5) and four measurement phases (phases 1 through 4). If the junction voltage of the integrator ("V_S" in Figure 1) is precisely $0.5V_{REF}$ (and AGND = 0V), then the phase 1 and phase 2 integration times are equal, indicating no input errors. If the junction voltage is different from $0.5V_{REF}$ (due to op amp offset voltage, bias current, etc.) and/or AGND $\neq$ 0, an error count "n" is obtained. The analog input integration cycle (phase 3) is subsequently lengthened or shortened by "n" counts. The effect is to eliminate the error term from the final output-count N_0 on a first order basis. The errors remaining in N_0 are negligible.

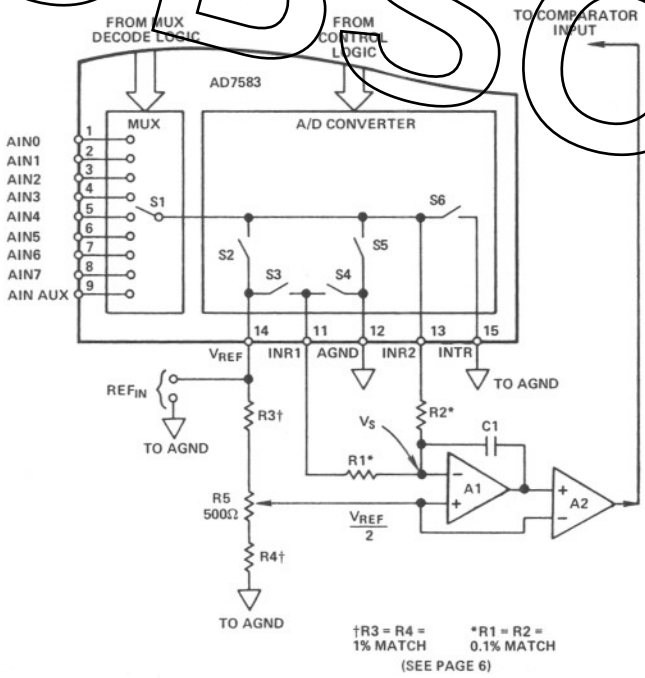


Figure 1. Functional Diagram of AD7583 Analog Circuitry

The time difference between the last comparator crossing and the termination of counter K3 represents the output count N_0. This count is divided by two and fed to an output totalizing counter which is preset in such a manner as to give a transfer function per table 1.

Phase	Input Voltage	Integration Time
0	$V_{REF} - V_S$	$\left(\frac{2V_{DD}}{V_{REF}} - 1\right) \cdot \left(\frac{R_1 R_2}{R_1 + R_2}\right) \cdot C_1$
1	$AGND - V_S$	$K_1 t$
2	$V_{REF} - V_S$	$(K_1 + n)t$
3	$\frac{AIN}{2} - V_S$	$(2K_1 - n)t$
4	$V_{REF} - V_S$	$(2K_1 + n - N_0)t$
5	$AGND - V_S$	$\left(\frac{2V_{DD}}{V_{REF}} - 1\right) \cdot \left(\frac{R_1 R_2}{R_1 + R_2}\right) \cdot C_1$

Where:
t = clock period
n = system error count (±)
K_1 = fixed count = 364
K_2 = fixed count = $4K_1$ = 1456
K_3 = fixed count = $4K_1$ = 1456
N_0 = internal count corresponding to the analog input voltage

Table 1. Integrator Equivalent Input Voltages and Integration Times

Analog Input Voltage	Internal Count Representation, N_0	Digital Output D_7 (MSB) . . . . . D_0 (LSB)
0 to $0.15V_{REF1}$	$N_0 = 0$	00000000
$(0.15$ to $0.85)\ V_{REF1}$	$N_0 = \frac{255}{0.7}\left(\frac{AIN}{V_{REF1}} - 0.15\right)$	00000000 to 11111111
$0.85V_{REF1}$ to V_{REF1}	$N_0 = 255$	11111111

Note: V_{REF1} and the Analog Input must both be positive voltages ($0 \leq AIN \leq V_{REF}$).

Table 2. Code Relationship

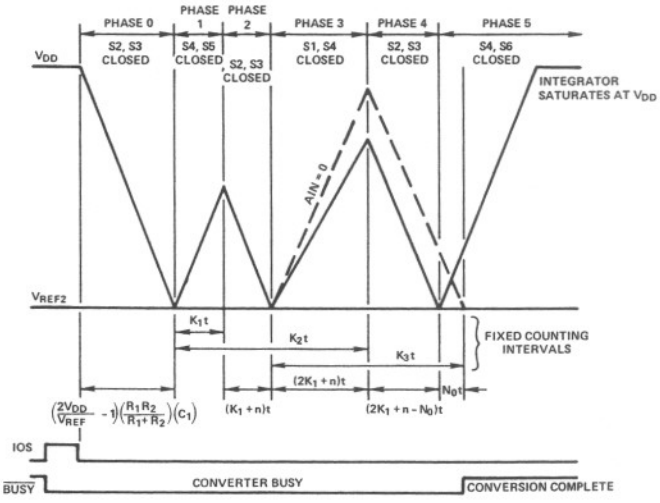


Figure 2. Quad Slope Timing Diagram

TIMING AND CONTROL OF THE AD7583

INTERFACE LOGIC

Figure 3 shows the functional diagram of the AD7583 Input/Output Logic. Digital information is communicated to and from the AD7583 via a bidirectional 8-bit data bus (D_{0-7}) under command of control inputs I/$\overline{O}$ (INPUT/$\overline{OUTPUT}$) and IOS (INPUT/OUTPUT STROBE).

With $\overline{RST}$ high, before the AD7583 will respond to commands placed on the I/$\overline{O}$ and IOS inputs, the device must be *enabled* by setting the Device Enable Latch. This is a one-time requirement which is accomplished by putting D_{0-7} equal to XXX11001, putting DCE (Decode Enable) HIGH, and strobing DCS (Decode Strobe). The AD7583 will remain *enabled* until a specific *disable* command is issued. Once the internal Device Enable Latch's "Q" output is HIGH, the internal READ and WRITE gates are enabled, control of these gates thus passes to the I/$\overline{O}$ and IOS inputs.

I/$\overline{O}$ controls data direction while IOS activates either the internal READ or WRITE signal. The 3-state output buffer is activated when READ is high. The General Buffer Latch and Channel Address Latch is loaded on the positive edge of the internal WRITE signal.

OPERATION

The AD7583 responds to 4 basic operation commands:

- ☐ Enable Command to bring the AD7583 out of its standby state.
- ☐ Disable Commands to place the AD7583 in standby.
- ☐ Channel Select and Start Command.
- ☐ Data READ Command.

1. ENABLE COMMAND (See Figure 4)
   Place code XXX11001 binary on D_{0-7}, put DCE HIGH, and strobe DCS. Timing requirements are shown in Figure 4.

2. DISABLE COMMAND (See Figure 4)
   There are 3 ways to place the AD7583 in a standby (disabled) mode:
   1. Put data bus D_{0-7} to a code *other than* XXX11001, put DCE HIGH, and strobe DCS.
      or
   2. Put DCE LOW and strobe DCS (D_{0-7} are "don't care")
      or
   3. Put $\overline{RST}$ momentarily LOW.

3. CHANNEL SELECT and START COMMAND (See Figure 5)
   Assuming the AD7583 has been *enabled* as per paragraph 1 above, the AD7583 will accept a Channel Select and Start Command. Put the channel address (per table 3) on Data Bus inputs D_{0-3}, put I/$\overline{O}$ HIGH (INPUT mode) and strobe IOS as per Figure 5.

   The positive edge of IOS strobes D_{0-3} into the Channel Address Latch, strobes data on D_{4-7} into the General Buffer Latch, resets all internal control logic, and causes $\overline{BUSY}$ (status output) to go LOW. In addition, within one clock period after IOS goes HIGH, phase 0 of the A/D conversion cycle begins (see Figure 2). Note: Attempting to execute a convert start when $\overline{BUSY}$ is LOW can cause an erroneous conversion.

4. DATA READ COMMAND (Figure 6)
   Prior to issuing a READ command, the AD7583 should have been enabled (as per paragraph 1) and $\overline{BUSY}$ must be HIGH.

   Failure to observe this precaution will cause erroneous data to be read.

   A DATA READ COMMAND is as follows: Put I/$\overline{O}$ LOW (OUTPUT mode) and put IOS HIGH. (The 3-state buffers are activated when IOS is HIGH). Timing is shown in Figure 6.

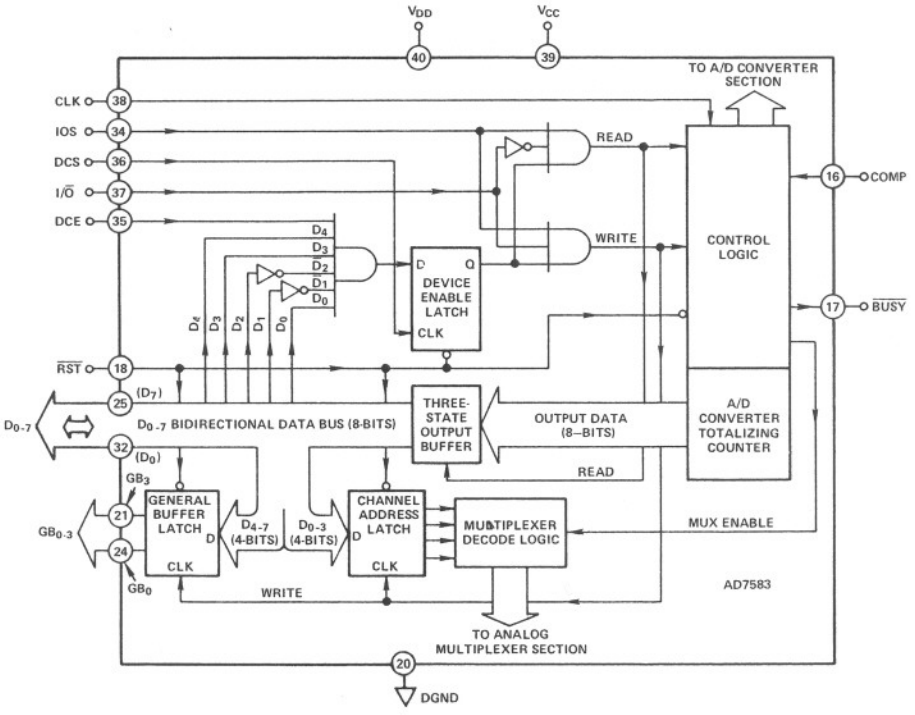


Figure 3. AD7583 Logic Section Functional Diagram

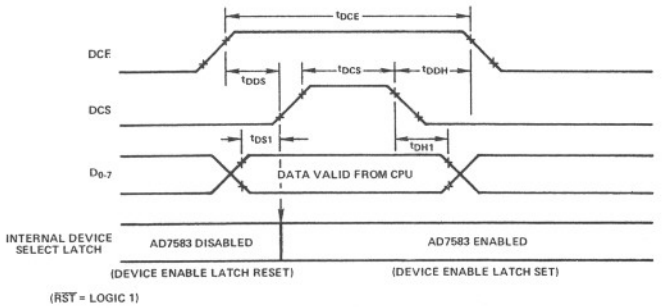


Figure 4. Setting the Device Enable Latch (Enabling the AD7583)

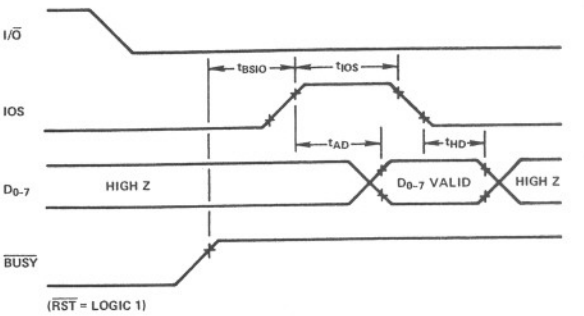


Figure 6. Data Read Timing

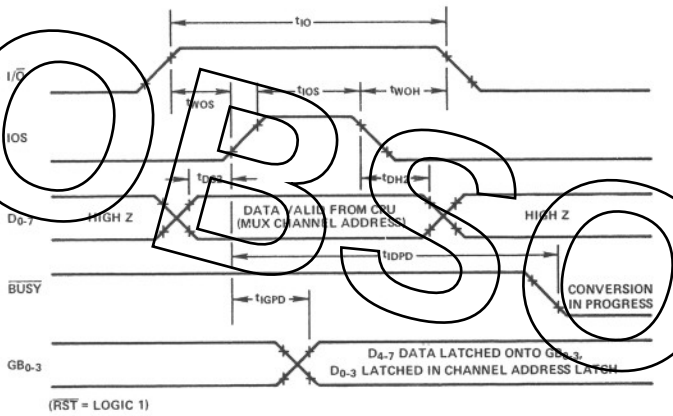


Figure 5. Writing Analog Channel Address and Convert Start

Channel Address				Selected Channel
D3	D2	D1	D0	
0	0	0	0	AIN0
0	0	0	1	AIN1
0	0	1	0	AIN2
0	0	1	1	AIN3
0	1	0	0	AIN4
0	1	0	1	AIN5
0	1	1	0	AIN6
0	1	1	1	AIN7
1	X	X	X	AIN AUX

Note: 1 is Logic HIGH
0 is Logic LOW
X is "DON'T CARE"

Table 3. Channel Address Codes

ANALOG CIRCUIT SETUP

Selecting an Integrator Amp (A1 in Figure 7)

Integrator amplifier A1 (Figure 7) must be chosen such that its total equivalent input error voltage e_{eq} over the temperature range of interest is

$$e_{eq} = V_{OS} + I_{BIAS}\left(\frac{R_1 R_2}{R_1 + R_2}\right) \text{is less than } 1.4\%\ V_{REF}$$

Where:

V_{OS} = Op Amp A1 Offset Voltage
I_{BIAS} = Op Amp A1 Bias Current
R1 and R2 are integrator resistors (Figure 7)

General purpose BIFET or BIMOS op amps (such as the AD544J, TL081 or CA3160) meet the above criteria when using a V_{REF} of at least +6V. BIMOS amplifiers have an advantage over BIFET types in that the output voltage swing can be virtually rail-to-rail. This precludes the necessity to guardband the integrator's peak output swing when calculating the integrator time constant.

Integrator Time Constant (Figure 7)

Proper selection of integrator time constant $\left(\frac{R_1 R_2}{R_1 + R_2}\right) \cdot C_1$ is important. Too large a value may cause noisy operation, while too small a value may cause the integrator output to saturate to V_{DD}. Use the following for calculating the time constant τ:

$$\tau = \left(\frac{R_1 R_2}{R_1 + R_2}\right) \cdot C_1 = \frac{364 V_{REF}}{(f_{CLK})(V_{DD} - 0.5 V_{REF})}$$

if $V_{REF} = V_{DD}$, this simplifies to

$$\tau = \left(\frac{R_1 R_2}{R_1 + R_2}\right) \cdot C_1 = \frac{728}{f_{CLK}}$$

The integrator resistors R1 and R2 must match and track to within 0.1% over the temperature range of interest. Their absolute value; however, may be between 200kΩ to 2MΩ. Values larger than 2MΩ may cause noisy operation, whereas values smaller than 200kΩ cause relative accuracy degradation.

The integrator capacitor C1 should be a low leakage, low dielectric absorption type (teflon, polypropylene or polystyrene). Ensure that the outside foil of the capacitor is connected to the *output* of amplifier A1 to minimize noise injection.

CONVERSION TIME

Total conversion time is equal to 2184 clock periods plus the phase 0 reset time.

$$t_{CONVERT} = \frac{2184}{f_{CLK}} + \tau\left(\frac{2V_{DD}}{V_{REF}}\right) - 1$$

Where:

τ = Integrator time constant

If $V_{REF} = V_{DD}$, this simplifies to

$$t_{CONVERT} = \frac{2184}{f_{CLK}} + 2\tau$$

INITIAL CALIBRATION (FIGURE 7)

Short circuit integrating capacitor C1 (with the AD7583 powered but not converting) and adjust trimpot R5 for amplifier A1 output equal to $0.5V_{REF}$ to within 1.4%.

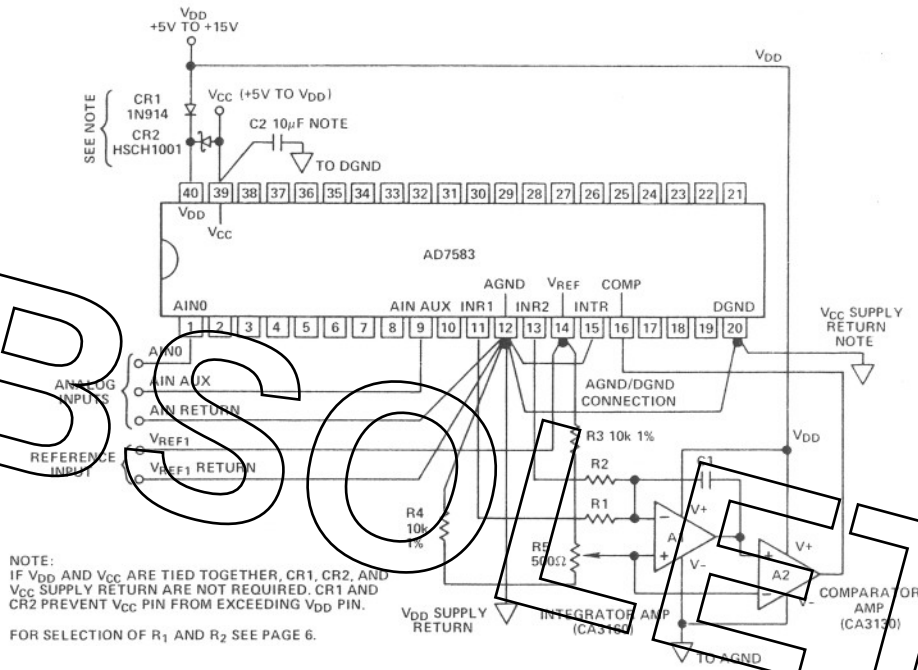


Figure 7. Analog Circuit Connections (Logic Input/Output Connections Omitted for Clarity)

APPLICATION HINTS

1. The AGND/DGND connection should be made at the AD7583, as shown in Figure 7. In systems where the connection must be remote, connect back-to-back diodes (1N914 or equivalent) between pin 12 and 20 of the AD7583.
2. Failure to observe correct grounding techniques can introduce conversion error and/or noise. System analog common must be located directly at pin 12 of the AD7583, as shown in Figure 7.
3. A major advantage of the AD7583 is the fact that the ADC does not respond to analog inputs less than $0.15V_{REF}$ or greater than $0.85V_{REF}$ (see table 1). A signal buffer amplifier used to drive the AIN inputs can therefore be powered from AGND and V_{DD} since its output will not have to swing to either rail. This is a particular advantage in single supply systems. For +5V single supply applications, we recommend BIMOS amplifiers (such as the CA3160) because of their rail-to-rail output voltage capability.
4. Do not apply V_{CC} before V_{DD}. Additionally, V_{CC} must never exceed V_{DD}. Failure to observe this precaution may cause device failure.
5. Attempting to write a convert start command when $\overline{BUSY}$ is LOW may result in an erroneous conversion.
6. To prevent loading errors due to the finite input impedance at any AIN input ($R_{IN} \approx R_1$), AIN should be driven from a source impedance lower then 0.1% R1.
7. For proper operation, ensure that the correct values for the integrator components have been selected and resistance tolerance and capacitor type are as recommended on page 6.

CHANNEL EXPANSION

Figure 8 shows the AD7583 expanded to 24 channel operation using a single supply CD4067 16-channel analog multiplexer. The AD7583 General Buffer Outputs (GB_{0-3}) are used as the multiplexer address. The ON resistance of the CD4067 is buffered by amplifier A1.

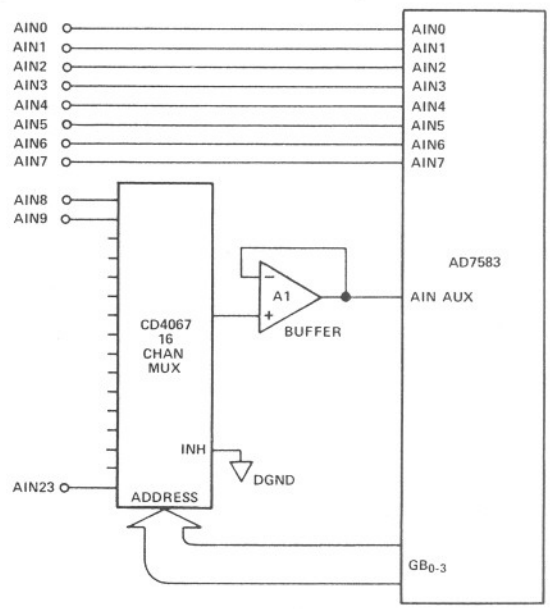


Figure 8. Channel Expansion Scheme

MICROPROCESSOR INTERFACE

Figure 9 shows how to interface the AD7583 to a MCS-85 microprocessor via an I/O port.

Port A of the 8155 is used as a bidirectional bus for sending channel address data to the AD7583, and for reading converted data into the MCS-85 system. Port B is used to control the strobes IOS, DCS, I/$\overline{O}$, and DCE.

The $\overline{BUSY}$ output is used as an interrupt, while $\overline{RST}$ is tied to the MCS-85 system reset.

A typical operating procedure is as follows:

Initilization

1. Power ON
2. $\overline{RST}$ (System Reset)
3. Put Port B as follows:
   DCS = LOW
   DCE = HIGH
   IOS = LOW
   I/$\overline{O}$ = Don't Care
4. Put Port A to Code XXX11001
5. Put Port B as follows:
   DCS = HIGH
   DCE = HIGH
   (AD7583 is now "enabled")
   IOS = LOW
   I/$\overline{O}$ = Don't Care
6. Put Port B as follows:
   DCS = LOW
   DCE = LOW
   IOS = LOW
   I/$\overline{O}$ = HIGH

Channel Address and Convert Start

1. Output desired Channel address to Port A (as per table 3).
2. Put Port B as follows:
   DCS = LOW
   DCE = HIGH
   IOS = LOW
   I/$\overline{O}$ = LOW
3. Put Port B as follows:
   DCS = LOW
   DCE = LOW
   IOS = HIGH
   I/$\overline{O}$ = HIGH
   (Latches in channel address, $\overline{BUSY}$ goes LOW)
4. Put Port B as follows:
   DCS = LOW
   DCE = LOW
   IOS = LOW
   I/$\overline{O}$ = HIGH
5. Put Port B as follows:
   DCS = LOW
   DCE = LOW
   IOS = LOW
   I/$\overline{O}$ = LOW

Interrupt Service (Reading Converted Data)

1. Enter Interrupt when BUSY goes HIGH (ie, valid data is available)
2. Put Port B as follows:
   DCS = LOW
   DCE = LOW
   IOS = HIGH (activates three-state buffers)
   I/$\overline{O}$ = LOW
3. READ Port A (converted data)
4. Put Port B as follows:
   DCS = LOW
   DCE = LOW
   IOS = LOW (deactivates three-state buffers)
   I/$\overline{O}$ = HIGH
5. Return to Main Program

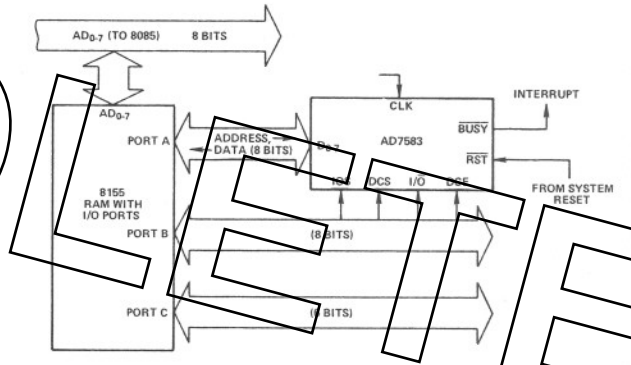


Figure 9. Interfacing the AD7583 to MCS-85 VIA an I/O PORT (Analog Circuitry Not Shown for Clarity)

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

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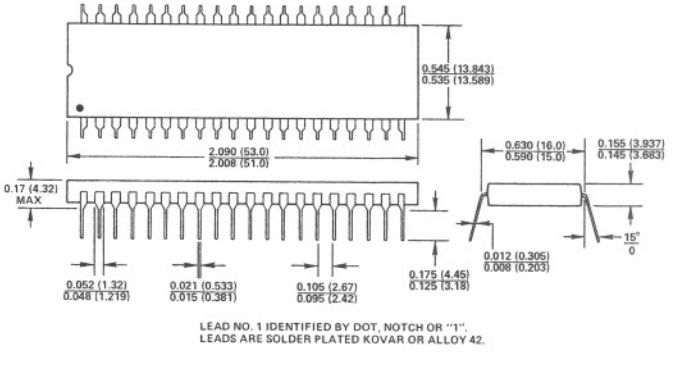

LEAD NO. 1 IDENTIFIED BY DOT, NOTCH OR "1".
LEADS ARE SOLDER PLATED KOVAR OR ALLOY 42.