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APPLICATION NOTE

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Achieving Pseudosimultaneous Sampling by Using the AD7616 Flexible Sequencer and Burst Mode

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INTRODUCTION

The AD7616 is a cost and performance optimized, 16-bit, 2 × 8 channel analog-to-digital converter (ADC) with dual simultaneous sampling. The dual ADC architecture enables the AD7616 to sample two analog channels simultaneously.

For power line applications, sample the voltage channel and current channel inputs concurrently to reduce the phase error between these inputs.

However, in a 3-phase power measurement system, dual-channel simultaneous sampling is not sufficient for concurrently sampling six analog channels. The phase error between the samples of the different phases can cause some level of error for power measurement, and it is difficult to compensate accurately in the software, especially when taking harmonic content into account.

This application note introduces a method for achieving pseudosimultaneous sampling by using the AD7616 input channels and by minimizing the phase mismatch between the 16 channels. When using this method, it minimizes the channel-to-channel phase mismatching without diminishing the amplitude accuracy performance.

For this application note, a theoretical analysis was done by using a mathematical simulation to show how the accuracy of the signal amplitude can be influenced, and how accurate channel-to-channel matching can be using this method. In addition, an on-board test result was implemented to prove the simulation results in practice.

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REVISION HISTORY

8/2016—Revision 0: Initial Version

PSEUDOSIMULTANEOUS SAMPLING

When a muxed input, nonsimultaneous sampling ADC cycles through its input channels and converts them one after another, a conversion time delay gets introduced between the channels. The delay time depends on the sampling rate of the ADC. From a system level point of view, such a time delay generates a system level phase error or phase mismatch between each analog channel.

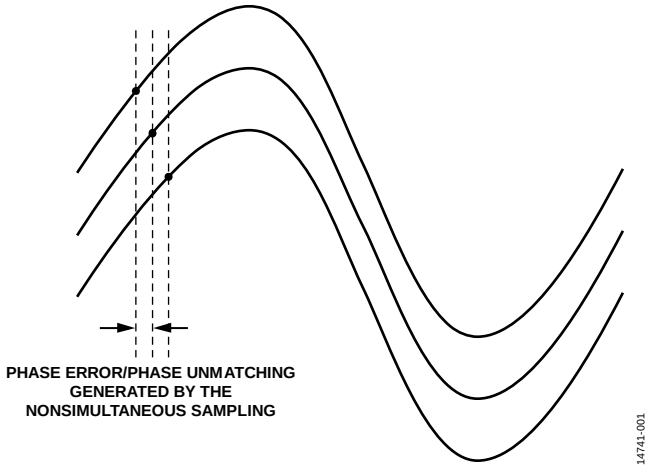

Figure 1. Phase Mismatch Due to Nonsimultaneous Sampling

Assume that one 50 Hz sine wave signal is applied to the inputs of an 8-channel muxed ADC (all channels share a single input source), and that the ADC samples at 1 MSPS cycling through the channels. When the software receives the final sample, the discrete Fourier transform (DFT) algorithm calculates the phase angle between the channels. Theoretically, the phase angle between the first channel and second channel is

$$(1\ \mu s/20\ ms) \times 360 \times 60° = 1.08'$$

The pseudosimultaneous sampling method uses the phase angle average to minimize phase error.

For example, arrange the ADC sampling burst into an up and down sequencer, as follows: VIN1 → VIN2 → VIN3 → … → VIN6 → VIN7 → VIN6 → … → … → VIN3 → VIN2 → VIN1.

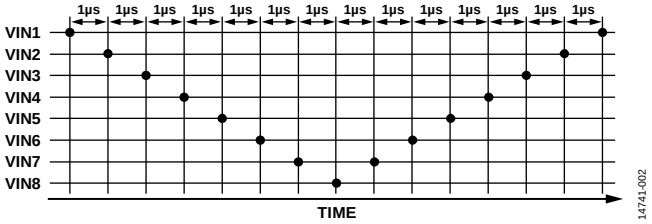

Figure 2. Analog Channel VINx Sampling Pattern

Because of this averaging, within each conversion burst, there are two conversion results for Analog Channel VIN1 to Analog Channel VIN7 and a single conversion result for Analog Channel VIN8. For VIN1 to VIN7, average the two samples, and use the averaged result as the final ADC sampling result for the power calculation. When there is tight control of the timing between conversions, the timing between each sample is equidistant (1 µs between each sample). The average result of VIN0 toVIN7 is equivalent to simultaneously sampling the signal, which is aligned to VIN8 (the middle sample) on the time axis.

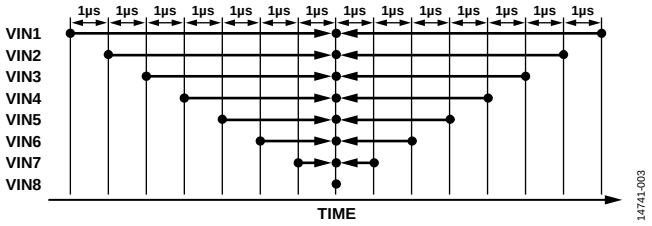

Figure 3. Time Averaged Samples Align with VIN8

Note that this is why this method is called pseudosimultaneous sampling.

BOUNDARY CONDITION FOR USING PSEUDO-SIMULTANEOUS SAMPLING

To understand the boundary conditions for using the pseudo-simultaneous sampling method, analyze the worst case error and determine what must be done within the system level design to control the error to an acceptable level.

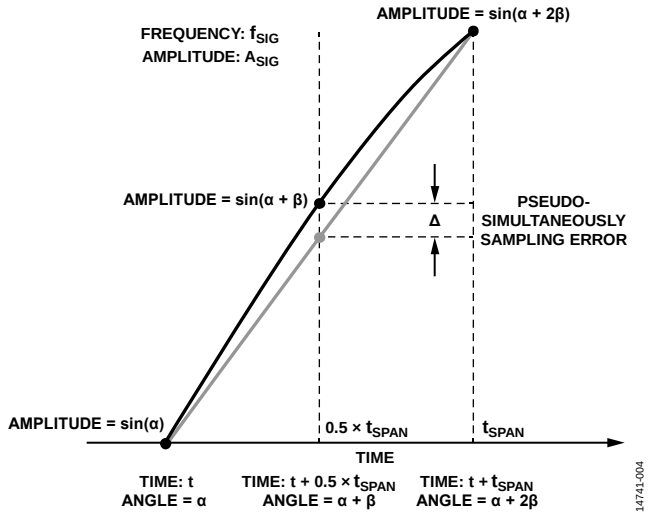

Figure 4. Determining Sampling Error

When using a pseudosimultaneous sampling method, see Figure 4 and use the following formula to calculate the error.

The average value of two sample points is

$$(\sin(\alpha) + \sin(\alpha + 2\beta))/2$$

The original value of a sine wave at the center point of the two samples is

$$\sin(\alpha + \beta)$$

Therefore, the error Δ is

$$|(\sin(\alpha) + \sin(\alpha + 2\beta))/2 - \sin(\alpha + \beta)| = |(1 - \cos(\beta)) \times \sin(\alpha + \beta)|$$

Maximum error happens when α = (π/2 − β), and the maximum error depends on β only.

$$\Delta_{MAX} = 1 - \cos(\beta)$$

$$\beta = (N - 1) \times 2\pi \times f_{SIG}/f_S$$

Therefore,

$$\Delta_{MAX} = 1 - \cos((N - 1) \times 2\pi \times f_{SIG}/f_S)$$

where:
N is the number of channels.
f_{SIG} is the signal frequency.
f_S is the sampling frequency.

For example, assuming that the maximum sampling frequency is 1 MHz, that the ADC has eight channels in total, and that the input frequency is 50 Hz, the theoretical maximum amplitude error for a 50 Hz signal is

$$1 - \cos(7 \times 2\pi \times 50/1000000) < 0.001\%$$

Note that this error can be neglected.

When the input frequency is 250 Hz (fifth-order harmonic), the theoretical maximum amplitude error for a 50 Hz signal is

$$1 - \cos(7 \times 2\pi \times 250/1000000) < 0.01\%$$

When the input frequency is 2.55 kHz (51st-order harmonic), the theoretical maximum amplitude error for a 50 Hz signal is

$$1 - \cos(7 \times 2\pi \times 2500/1000000) = 0.604\%$$

Note the following about this theoretical analysis:

- A higher sampling rate has benefits in achieving a higher system level amplitude accuracy.
- It is recommended to keep the time interval between the samples in a burst constant.
- A higher frequency input signal cannot be measured accurately. However, in a typical power transmission and distribution application, the measurement accuracy for higher order harmonics is not normally that critical. It is normally sufficient to meet system level specifications for most applications.

USING THE AD7616 TO IMPLEMENT PSEUDOSIMULTANEOUS SAMPLING

FLEXIBLE SEQUENCER

When used in software mode, the AD7616 has a flexible and programmable sampling sequencer. During system power on, the user can program the sequencer of the AD7616 into a predefined sampling order by writing to the sequencer stack registers. The sequencer stack is composed of 32 registers, which allow a maximum of 32 channel pairs to be programmed flexibly.

The eight LSBs of each sequencer stack register (Channel D0 to Channel D7) define which channel in Group A (Channel A0 to Channel A7) and which channel in Group B (Channel B0 to Channel B7) are selected for the next conversion. Bit D8 in the register defines whether the sequencer stops after the next conversion to go back to the first layer of the stack. When the sequencer is activated, it reads out the configuration from the first sequencer stack register, sequentially cycles through the remaining layers, and stops when it meets the first sequencer stack register with Bit D8 set to 1. The sequencer pointer then returns to the first layer of the stack for the next sequence.

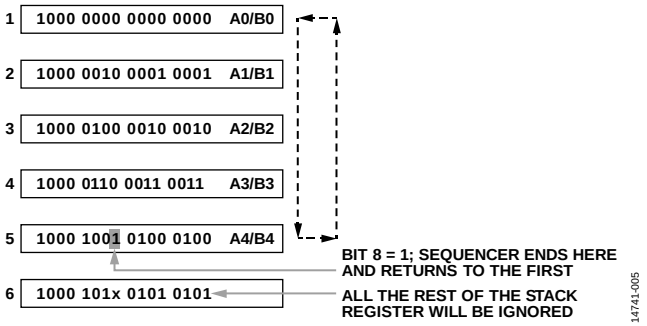

Figure 5. Programming the AD7616 Sequencer to Activate a Sampling Burst

BURST MODE

For most traditional muxed input, successive approximation register (SAR) ADCs, one convert signal results in only one ADC conversion. In other words, only one ADC channel can be sampled by one CONV pulse.

To meet the boundary conditions required to use pseudo-simultaneous sampling, users must continually generate the CONVST signal to the ADC in a burst of high speed pulses with the same time interval in between.

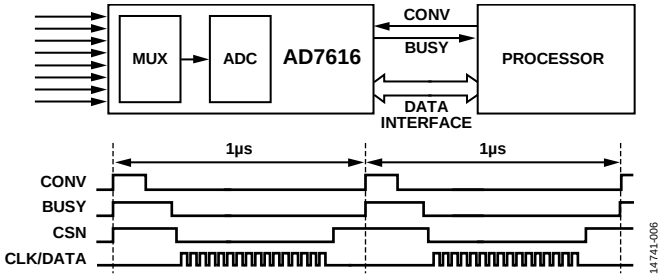

Figure 6. Sampling Burst Achieved by Using a Traditional Muxed Input ADC

In addition, the ADC conversion data must be read out in a very short time. Sometimes, such a requirement can cause problems when customers want to use a general-purpose microcontroller unit (MCU) to interface with the ADC.

However, the burst mode of the AD7616 solves this problem very well. When burst mode is activated, the ADC requires a single CONVST trigger from the controller. The internal logic of the ADC generates a series of high speed internal CONVST pulses to trigger the ADC core, cycles through the preselected channels programmed to the sequencer, and stores the complete burst of the ADC conversion results in a data buffer. The controller can then read the whole data frame out at a slower speed.

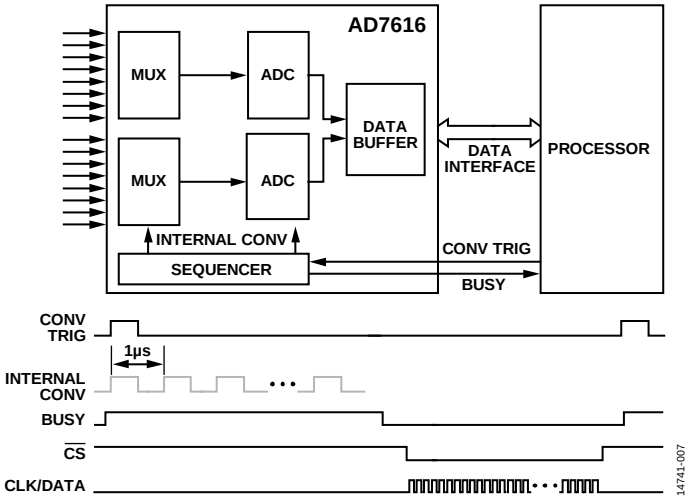

Figure 7. Sampling Burst Achieved by Using the Burst Mode of the AD7616

By using the burst sequencer, the user can easily achieve the highest sampling rate of the ADC core in a short burst without any limitation on the MCU MIPS and data interface speed. In combination with the user defined flexible sequencer, pseudosimultaneous sampling can be implemented easily on the AD7616.

PRACTICE TESTING

Testing Setup

Figure 8 shows the practice test setup. A precision signal (audio precision) generator feeds a low noise, low THD sine wave to the AD7616.

The ADSP-CM408F processor controls the AD7616 using the pseudosimultaneous sampling configuration. The ADC raw data is sent to the PC via the universal asynchronous receiver/transmitter (UART) for further analysis. Then, the VisualAnalog® software can analyze the ADC data to get the ac performance (SNR and THD), and Microsoft Excel® can run a DFT algorithm to get the phase and amplitude information.

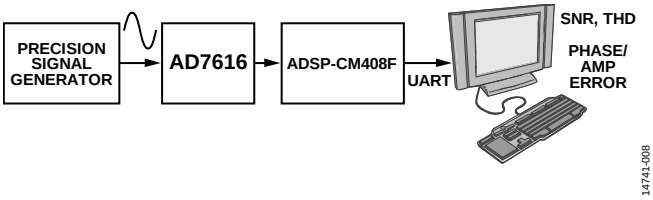

Figure 8. Practice Test Setup

To make the comparison easier, the sequencer is programmed to sample the same Analog Input VIN1

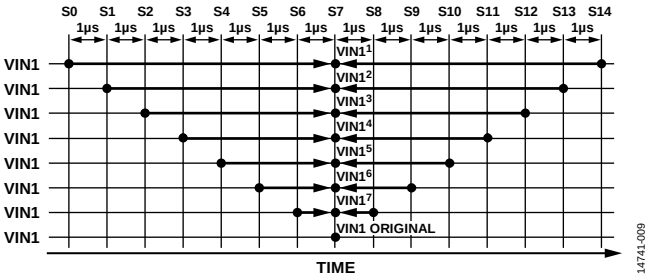

Figure 9. VIN1 Sample (S0 to S14)

In one data burst, VIN1 is sampled 15 times. As shown in Figure 9, the first sample (S0) is paired with the last sample (S14) to get an avearaged result for VIN1[1], the second sample (S1) is paired with the 14th sample (S13) to get VIN1[2], and so on. Note that the eighth sample is untouched and used as the original VIN1. All other averaged data (VIN1[1] to VIN1[7]) are compared to the original VIN1 to get the final testing result.

Testing Results

Test Signal = 50 Hz (Power Line Fundamental)

For a low frequency input signal (50 Hz), the averaged signal has overall zero delay relative to the original signal. The amplitude and total harmonic distortion (THD) are not influenced at all; in fact, the signal-to-noise ratio (SNR) performance is slightly improved. See Table 1 for additional details.

Testing Signal = 250 Hz (Power Line Fifth Harmonic)

When the input frequency is increased slightly to 250 Hz, the averaged signal maintains almost zero delay to the original signal. The amplitude has −0.001 dB attenuation (equal to 0.01%, which is compatible with the mathematical calculation discussed in the Boundary Condition for Using Pseudo-Simultaneous Sampling section). The THD has no overall change compared to the original signal, and the SNR has an improvement of 0.5 db to 1 dB. See Table 2 for additional details.

Table 1. Testing Results, Input Signal Frequency = 50 Hz

Averaged Item	Full-Scale SNR (dB)	THD (dBFS)	AMP (dBFS)	Phase (°) Compared with S7
S7 (VIN1 Original)	88.27	−101.37	−0.352	Not applicable
S0 + S14 (VIN1[1])	89.09	−101.75	−0.352	<0.01
S1 + S13 (VIN1[2])	90.18	−103.34	−0.352	<0.01
S2 + S12 (VIN1[3])	90.07	−102.66	−0.352	<0.01
S3 + S11 (VIN1[4])	89.78	−101.72	−0.352	<0.01
S4 + S10 (VIN1[5])	89.67	−102.09	−0.352	<0.01
S5 + S9 (VIN1[6])	89.40	−100.97	−0.352	<0.01
S6 + S8 (VIN1[7])	89.06	−101.75	−0.352	<0.01

Table 2. Testing Results, Input Signal Frequency = 250 Hz

Averaged Item	Full-Scale SNR (dB)	THD (dBFS)	AMP (dBFS)	Phase (°) Compared with S7
S7 (VIN1 Original)	86.88	−100.61	−0.352	Not applicable
S0 + S14 (VIN1[1])	88.46	−102.86	−0.353	<0.01
S1 + S13 (VIN1[2])	88.32	−101.98	−0.353	<0.01
S2 + S12 (VIN1[3])	88.34	−101.14	−0.353	<0.01
S3 + S11 (VIN1[4])	87.86	−101.52	−0.353	<0.01
S4 + S10 (VIN1[5])	88.14	−101.38	−0.353	<0.01
S5 + S9 (VIN1[6])	87.79	−100.73	−0.353	<0.01
S6 + S8 (VIN1[7])	87.72	−101.17	−0.352	<0.01

Testing Signal = 2550 Hz (Power Line 51st Harmonic)

When the input frequency is increased to 2550 Hz (the 51st order of the 50 Hz line frequency), the maximum amplitude error is increased slightly. The averaged signal S0 + S14 is the worst case for the amplitude measurement. The attenuation is approximately −0.055 dB, which is equal to 0.63% and is consistent with the mathematical analysis result. The THD has no overall change compared to the original signal, and the SNR has an improvement of 0.5 dB to 1 dB. The phase error still maintains a very low level (<0.01°) and can be ingnored for most of the power automation applications. See Table 3 for additional details.

Table 3. Testing Results, Input Signal Frequency = 2550 Hz

Averaged Item	Full-Scale SNR (dB)	THD (dBFS)	AMP (dBFS)	Phase (°) Compared with S7
S7 (VIN1 Original)	85.66	−95.69	−0.381	Not applicable
S0 + S14 (VIN1[1])	86.78	−95.86	−0.436	<0.01
S1 + S13 (VIN1[2])	86.88	−95.54	−0.422	<0.01
S2 + S12 (VIN1[3])	86.75	−95.58	−0.409	<0.01
S3 + S11 (VIN1[4])	86.75	−95.01	−0.399	<0.01
S4 + S10 (VIN1[5])	86.49	−95.29	−0.392	<0.01
S5 + S9 (VIN1[6])	86.47	−95.29	−0.386	<0.01
S6 + S8 (VIN1[7])	86.18	−95.40	−0.383	<0.01

CONCLUSION

For most power automation applications, the measured input signal is in the 50 Hz to 2550 Hz range. By using the flexible sequencer and burst mode of the AD7616, the pseudosimultaneous sampling method achieves perfect phase to phase synchronization without decreasing the system level ac performance.

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