AN-611
APPLICATION NOTE

50 Hz/60 Hz Rejection on Σ-Δ ADCs

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INTRODUCTION

Rejection of 50 Hz and 60 Hz interference is a require-ment in many industrial settings. This Application Note outlines how the AD7708/AD7718, AD7709, AD7719, AD7782/AD7783 Σ-Δ ADCs are used for optimal rejection of these frequencies.

POWER LINE FREQUENCIES

Electrical ac power is distributed worldwide at one of two frequencies, 50 Hz or 60 Hz. This frequency can be picked up as undesired interference on electrical signals, either via the power supply transformers or via radiation from unshielded power cables or electrical equipment. There can also be interference present at harmonics of these frequencies, i.e., 100 Hz/150 Hz or 120 Hz/180 Hz, and so on, although these components are generally lower than the fundamental. The exact frequency of the mains signal can typically vary by up to ±1 Hz over time.

Mains interference presents significant problems when trying to measure low level signals with a high resolu-tion ADC.
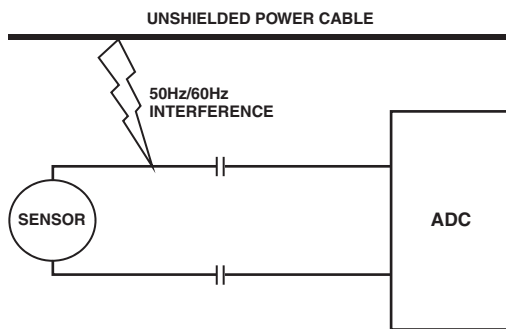

Figure 1. Source of 50 Hz/60 Hz Interference

REJECTING INTERFERENCE

Using differential signals allows rejection of any com-mon-mode 50 Hz/60 Hz interference, provided the system has good common-mode rejection. However, this does not provide any rejection of normal mode interference.

One solution for attenuating this interference is to use a low-pass analog filter. To obtain good rejection of 50 Hz and 60 Hz, this filter needs a low cutoff frequency and/or high order. A low cutoff frequency will limit the bandwidth of signals that can be measured, while high order analog filters are costly in terms of component count and board space. Also, the cutoff frequency may be prone to drift.

An alternative is to use a digital filter. This filter can be optimized for rejection at one power line frequency or can attenuate both frequencies simultaneously, allowing the equipment to be used worldwide without reconfiguration. The features of the filter to consider are rejection at 50 Hz ± 1 Hz and/or 60 Hz ± 1 Hz, rejection at harmonics of these frequencies, the settling time of the filter, and the complexity of the filter (affects power con-sumption, and so on.). The rejection required depends on the magnitude of the interference and the noise level of the system, e.g., 60 dB of rejection is sufficient to attenu-ate a 1 mV interference level down to 1 μV.

Σ-Δ ADCs

Σ-Δ ADCs include a digital filter as one of the components in their architecture. If correctly configured, this filter can provide impressive rejection of power line frequencies while still having sufficient bandwidth for measuring the input signal. The filter used on this family of ADCs from Analog Devices offers good mains frequency rejection while providing reasonably high update frequencies.

SINC[3] FILTER (UNCHOPPED)

The digital filter used in these ADCs is a sinc[3] filter. The response of this filter depends on the filter sampling rate, f_S (32.768 kHz), and a register value SF. This sets the update rate of the ADC, the position of the notches in the frequency response, and the noise of the ADC conversions. The frequency response of the sinc[3] filter is given by:

$$\left(\frac{1}{8SF} \times \frac{\sin\left(8SF \times \pi \times f / f_S\right)}{\sin\left(\pi \times f / f_S\right)} \right)^3$$

and the ADC update rate is:

$$\frac{f_S}{8SF}$$

REV. 0

A sinc[3] filter gives faster settling times compared to higher order sinc filters, so it is an excellent choice for good conversion speed if used with a low noise modulator. This filter response is only obtained from the AD7708/AD7718 when operating with chop off (ADMODE[7] = 1). In this mode, the settling time after a channel change, for example, is three times the time between conversions. This is to allow the sinc[3] filter to settle fully. A plot of the frequency response for SF = 75 (decimal) is shown in Figure 2.
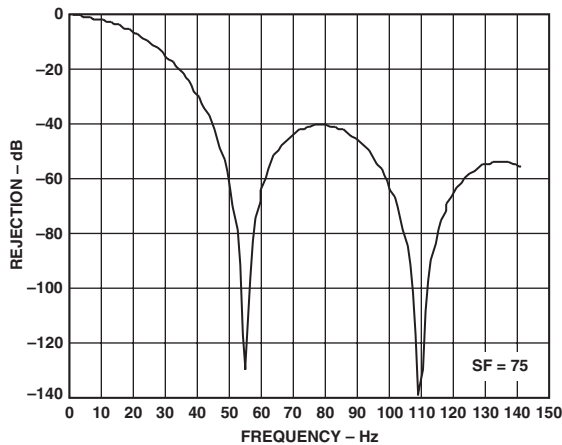

Figure 2. Rejection vs. Frequency; SF = 75

This choice of SF gives a deep notch around 55 Hz, which is midway between 50 Hz and 60 Hz, giving rejection of at least 57 dB at 50 Hz ± 1 Hz and 60 Hz ± 1 Hz while having an update rate of 55 Hz, and a low settling time of 55 ms. This is the best choice of SF for high update rates with 50 Hz/60 Hz rejection.

Increasing SF to 151 improves the 50 Hz/60 Hz rejection by 3 dB to 60 dB, but doubles the settling time to 111 ms. Setting SF to its max value of 255 gives 68 dB rejection while increasing the settling time to 187 ms.

If the country where the equipment will be operated is known, and hence the mains frequency, it is possible to get very high rejection at this frequency. For 50 Hz operation, a value of SF = 82 should be used; for 60 Hz, SF = 68 should be used. These give over 100 dB of rejection at the frequency of choice, but as low as 40 dB at the other frequency, while the settling time is 60 ms/50 ms.

An update rate of 10 Hz in theory allows rejection of both 50 Hz and 60 Hz, however, the conversion rate is very low, with a settling time of 300 ms. Note that it is not possible to get a 10 Hz (chop-off) rate on the AD7708/AD7718 using a 32.768 kHz crystal because the lowest available rate is 16 Hz.

The calculations in Table I assume that an exact 32.768 kHz crystal/clock is applied to the ADC. If the frequency is not exact, the rejection can degrade; e.g., for SF = 75, the rejection decreases to a worst-case figure of 52 dB assuming a clock with ±2% error. It should be noted, however, that 32.768 kHz crystals are much more accurate than this.

All of the above filter responses give equally good or better rejection at harmonics of 50 Hz and 60 Hz.

POST-FILTERING
Applying a simple post-filter to the ADC data can improve the 50 Hz/60 Hz rejection for a very small overhead. For example, with SF = 171 the ADC update rate is 24 Hz, so there is a deep notch at 24 Hz, 48 Hz, and so on. Performing a simple average-by-2 externally achieves a first order notch at 12 Hz, 36 Hz, 60 Hz, and so on. This gives worst-case 50 Hz/60 Hz rejection of 71 dB with a 3 dB frequency of 4.4 Hz and a settling time of 167 ms when accounting for the external average-by-2. It is also quite immune to clock inaccuracies, only decreasing to 65 dB with ±2% error on the clock. The ADC noise is lower than for SF = 75.

Table I. Rejection on AD7708/AD7718 (with Chopping Inactive)

	50 ± 1 Hz Rejection (dB)	60 ± 1 Hz Rejection (dB)	ADC Update Rate (Hz)	Settling Time (ms)	3 dB Frequency (Hz)
SF = 68	40	101	60.2	49.8	15.8
SF = 75	57	59	54.6	54.9	14.3
SF = 82	101	47	50.0	60.1	13.1
SF = 151	60	60	27.1	110.6	7.1
SF = 255	77	68	16.1	186.7	4.2

CHOPPED ADC

The AD7709/AD7719 operate with a chopped ADC to give very low offset errors and drifts. The AD7708/AD7718 can also optionally operate chopped. The averaging inherent in chopping affects the frequency response and can give improved 50 Hz/60 Hz rejection. The equation for the frequency response when chopped is given by:

$$\left(\frac{1}{2}\times\frac{\sin(2\times\pi\times f/f_{OUT})}{\sin(\pi\times f/f_{OUT})}\right)\left(\frac{1}{8SF}\times\frac{\sin(8SF\times\pi\times f/f_S)}{\sin(\pi\times f/f_S)}\right)^3$$

where $f_{OUT} = f_S/(8 \times SF \times 3)$

The output rate of the ADC is one-third that of a non-chopped ADC for an equivalent SF, and the settling time is two output periods. There are extra notches in the frequency response at odd multiples of $f_{OUT}/2$. For example, with SF = 69 (default), there is the usual sinc³ notch near 60 Hz but also a notch near 50 Hz, resulting in a worst-case rejection of 60 dB at an update rate of 19.8 Hz and a settling time of 101 ms. The rejection at 100/120 Hz is a little lower, at 46 dB. See Figure 3.
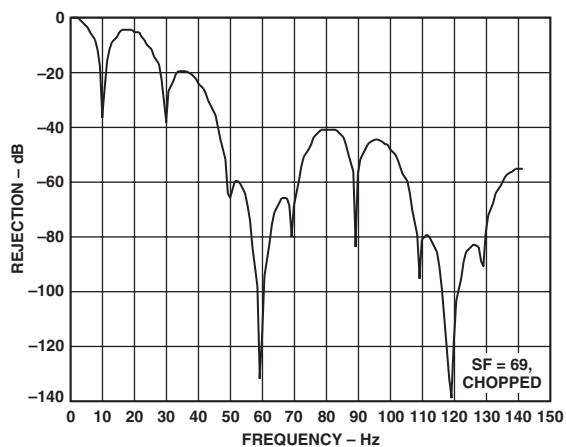

Figure 3. Rejection vs. Frequency; SF = 69, Chopped

Increasing SF to 79 for an update rate of 17.3 Hz achieves better rejection of 67 dB, and 55 dB at 100 Hz/120 Hz.

SF = 75 achieves 62 dB rejection at 50 Hz/60 Hz and 65 dB at 100 Hz/120 Hz.

For >100 dB rejection of one, power-line frequency SF = 82 or SF = 68 should be used for 50 Hz and 60 Hz, respectively.

AD7782/AD7783

The AD7782/AD7783 do not allow the value of SF to be modified, so they operate with the default value of SF = 69 and are chopped, giving 60 dB 50 Hz/60 Hz rejection at an update rate of 19.8 Hz. To improve the rejection, the ADC could be operated with a 28.8 kHz clock rather than 32.768 kHz, which will improve the rejection to 66 dB by operating at an update rate of 17.4 Hz. An extra 6 dB gives twice as much attenuation of the interference signal.

SUMMARY

This family of ADCs provides high conversion rates of up to 55 Hz while maintaining good 50 Hz and 60 Hz rejection. A software selectable update rate provides some flexibility in improving the 50 Hz/60 Hz rejection at the expense of conversion speed. There are certain values of ADC update rate for both chop off and chop on that yield optimum simultaneous 50 Hz and 60 Hz rejection. When selecting an update rate, care needs to be taken to ensure there is also sufficient rejection at harmonics of the mains interference, and any inaccuracies in the clock frequency are considered.

	50 ± 1 Hz Rejection (dB)	60 ± 1 Hz Rejection (dB)	ADC Update Rate (Hz)	Settling Time (ms)	3 dB Frequency (Hz)
SF = 68	54	101	20.1	99.6	4.8
SF = 69	60	95	19.8	101.1	4.7
SF = 75	62	66	18.2	109.9	4.4
SF = 79	75	67	17.3	115.7	4.1
SF = 82	101	53	16.7	120.1	4.0
SF = 150	67	66	9.2	219.7	2.2

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