AD7732/AD7734/AD7738/AD7739 Calibration Registers
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This application note concentrates on the AD7739 but is also applicable to the AD7732, AD7734, and AD7738. The purpose of this application note is to explore the calibration registers in more detail than is found on the data sheets.

INTRODUCTION
The AD7739 features two sets of calibration registers. The main function of these registers is to store the offset and gain coefficients for the various calibration modes. However, since all nine sets of registers can be read to and written from over the serial interface, these registers are available to manipulate raw ADC conversion results.

The first set of registers is a 24-bit offset (ADC offset) register and 24-bit gain (ADC gain) register, which affect all channels. The second set includes a per channel 24-bit offset register and a 24-bit per channel gain register, which affect a specific channel only.

The effect of the calibration registers is independent of conversion time, but does depend on the range. All calibration registers on the AD7732, AD7734, AD7738, and AD7739 can be read to or written from over the serial interface. However, a write to the registers will be ignored if the ADC is converting or calibrating when the write takes place. This avoids corrupting the conversion result. Therefore, you must set the ADC into its sync mode by writing 000 to the mode bits before writing to any of the calibration registers.
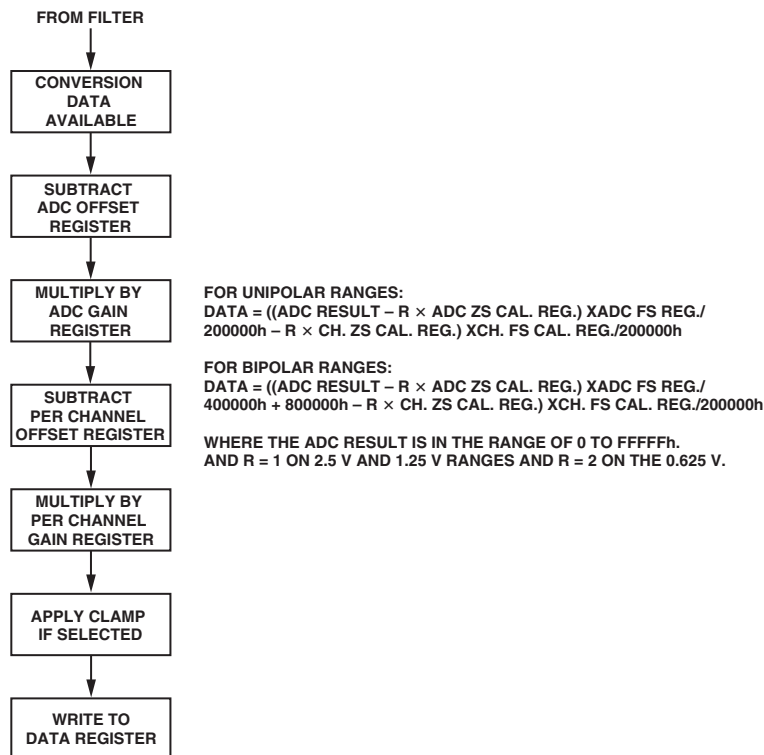

FROM FILTER

CONVERSION DATA AVAILABLE

SUBTRACT ADC OFFSET REGISTER

MULTIPLY BY ADC GAIN REGISTER

SUBTRACT PER CHANNEL OFFSET REGISTER

MULTIPLY BY PER CHANNEL GAIN REGISTER

APPLY CLAMP IF SELECTED

WRITE TO DATA REGISTER

FOR UNIPOLAR RANGES:
DATA = ((ADC RESULT – R × ADC ZS CAL. REG.) XADC FS REG./200000h – R × CH. ZS CAL. REG.) XCH. FS CAL. REG./200000h

FOR BIPOLAR RANGES:
DATA = ((ADC RESULT – R × ADC ZS CAL. REG.) XADC FS REG./400000h + 800000h – R × CH. ZS CAL. REG.) XCH. FS CAL. REG./200000h

WHERE THE ADC RESULT IS IN THE RANGE OF 0 TO FFFFFh.
AND R = 1 ON 2.5 V AND 1.25 V RANGES AND R = 2 ON THE 0.625 V.

Figure 1. Flow Chart for Calibration Register Contents

ADC OFFSET COEFFICIENT

The shared ADC offset register is a 24-bit register used in the calculation of all ADC results on any channel. Although this register may be read from and written to, this register should be modified only by self-ZS calibrations. The per channel offset registers were provided to allow users to manipulate the output code.

The format of the register is offset binary so that 0x000,000 is negative full-scale, 0xFFF,FFF is positive full-scale, and 0x800000 is 0. The default value of the register is 0x800000, which results in an adjustment of zero in the output code. The maximum absolute change is $\pm 2^{24}$.

If the mode is set to 000 and then 0x70BDC0 (minus one million in decimal) is written to the ADC ZS register, the effect on the output code for a 0 V input is as follows:

Table I. 24-Bit Output Codes for V_{IN} = 0, ADC Coefficient = 0x70BDC0 as Measured on Applications Board

V_{IN}	Range	Output Code Increase
0.0	±2.5	2,000,000
0.0	±1.25	2,000,000
0.0	±0.625	4,000,000
0.0	0/2.5	4,000,000
0.0	0/1.25	4,000,000
0.0	0/0.625	8,000,000

ADC GAIN COEFFICIENT

The shared ADC gain register is a 24-bit register and is used in calculating all ADC results on any channel. Although this register may be read from and written to, this register should be modified by only self-FS calibrations. The per channel gain registers were provided to allow users to manipulate the output code.

Table II. Bit Map of the ADC Gain Register

MSB	MSB-1	MSB-2	MSB-3	MSB-4	MSB-5	....	LSB
1	1/2	1/4	1/8	1/16	1/32		$1/2^{23}$

The range of the adjustment in gain is therefore from 0 to 2.

The default value of the register is 0x800000, which corresponds to a gain of 1.

If the mode is set to 000 and then 0x900,000 is written to the ADC FS register, the effect on the output code for a 0.5 V input is as follows:

Table III. Change in Output Code Due to Change in ADC Gain Coefficient

V_{IN}	Range	Output with ADC Gain Coefficient = 0x800000	Output with ADC Gain Coefficient = 0x900000
0.5	±2.5	1,695,000	1,906,794
0.5	±1.25	3,386,431	3,808,826
0.5	±0.625	6,772,522	7,617,452
0.5	0/2.5	3,389,465	3,812,643
0.5	0/1.25	6,771,653	7,617,749
0.5	0/0.625	13,544,211	15,233,216

INTRODUCTION TO THE PER CHANNEL OFFSET AND GAIN COEFFICIENTS

On each of the generics there are eight sets of per channel calibration registers, each comprised of a 24-bit offset and a 24-bit gain register. These registers are assigned to the physical input channels as shown in Table IV.

Table IV. Assignment of Physical Pins to Per Channel Calibration Registers

Channel	AD7738/AD7739	AD7734	AD7732
000	[AIN0, AIN1], [AIN0, Common]	AIN0	[AIN0+, AIN0–]
001	[AIN2, AIN3], [AIN1, Common]	AIN1	
010	[AIN4, AIN5], [AIN2, Common]	AIN2	[AIN1+, AIN1–]
011	[AIN6, AIN7], [AIN3, Common]	AIN3	
100	[AIN0, AIN1], [AIN4, Common]	AIN0	[AIN0+, AIN0–]
101	[AIN2, AIN3], [AIN5, Common]	AIN1	
110	[AIN4, AIN5], [AIN6, Common]	AIN2	[AIN0+, AIN0–]
111	[AIN6, AIN7], [AIN7, Common]	AIN3	

It can be seen from this table that most channel combinations have two available register sets. For example, AIN0 on the AD7738 uses channel register set 0 when converting on channel 000, but if the conversion is done on channel 100, then it uses register set 100.

On all four generics including the AD7732, AD7734, system zero-scale and system full-scale calibrations can be used to remove all offset and gain errors in the signal chain including offset and gain due to the on-chip resistor matching on the AD7732/AD7734. A system ZS calibration changes the per channel offset coefficient for a specific channel, and a system FS calibration changes the gain coefficient for the selected channel. If the system ZS and the system FS calibrations are performed in the factory and stored in external memory, they can be downloaded to the ADC after power-up.

PER CHANNEL OFFSET COEFFICIENT

With the per channel gain register at its default value, increasing the offset register contents by 1 increases or decreases the output of all future conversions on that channel, depending on the sign bit.

Table V. Bit Map of Per Channel Offset Register

MSB	MSB-1	Bits MSB-2 to LSB
Sign	0	Magnitude 0 to 2,097,151

The MSB of the per channel offset coefficient is the sign bit. If the sign bit is 1, the offset coefficient is negative and it causes the ADC output code to increase. If the MSB is 0, then the offset coefficient is positive and the output code decreases. Bit 23 of the per channel offset register must be 0 and the remaining 22 bits are magnitude bits.

As an illustration, if 0x8F4240, sign = 1, magnitude = 1 million decimal is written to the channel 0 ZS calibration register, the resulting change in all Channel 0 conversions will be as shown in Table VI.

Table VI. 24-Bit Output Codes Change Per Channel Offset Register = 0x8F4240

V_{IN}	Range	Output Code Increase
0.0	±2.5	1,000,000
0.0	±1.25	1,000,000
0.0	±0.625	2,000,000
0.0	0/2.5	2,000,000
0.0	0/1.25	2,000,000
0.0	0/0.625	4,000,000

Therefore for the ±2.5 V and ±1.25 V ranges, an LSB change in the per channel offset register corresponds to an LSB change in the ADC output code. For the ±0.625 V, 0/2.5 V, and 0/1.25 V ranges, a 1 LSB change in the calibration register gives a 2 LSB change in the output code; finally for the 0/0.625 V range, the change is 4 LSB.

PER CHANNEL GAIN COEFFICIENT

The default gain coefficient is 0x200000. This corresponds to multiplying all outputs by 1. The MSB bit corresponds to multiply by 4 and each successive bit multiplies by 2, 1, 0.5, and so on.

Table VII. Bit Map of the Per Channel Gain Register

MSB	MSB-1	MSB-2	MSB-3	MSB-4	MSB-5	----	LSB
4	2	1	1/2	1/4	1/8		1/2, 097, 152

The range of the adjustment is therefore from 0 to 8. This allows a digital PGA to be implemented to give input ranges smaller than ±0.625 V.

The per channel gain register is also used for system full-scale calibrations.

USE OF THE PER CHANNEL GAIN COEFFICIENT TO IMPLEMENT A PGA

The lowest available input range of the AD7739 is ±0.625 V. Suppose your signal range is only ±0.078 mV. The default per channel gain coefficient results in the outputs shown in column 2 for the input shown in column 1. A per channel gain coefficient of all ones results in a digital gain of 8, and –78.125 mV corresponds to an output of all zeros and +78.125 mV to all ones.

Table VIII. Effect of Digital PGA with Gain = 8

V_{IN}	Output Code with Coefficient = 0x800000	Output Code with Coefficient = 0xFFFFFF
–78 mV	0x8FF972	0xFFCB92
0	0x800000	0x800000
+78 mV	0x7FFBE9	0x00346E

The digital PGA is possible because the internal resolution of the AD7739 is more than 24 bits and because using the per channel gain coefficient gives access to these bits.

With a conversion time of 2.7 ms, the AD7739's output noise on the ±0.625 V range is only 1.2 μV rms or 19.9 bits rms. With a digital gain of 8, the user still has 16.9 bits of rms resolution on the ±0.078 mV range. Another important factor for implementing a digital PGA is the 24-bit no missing codes performance of these parts at high output rates.

PICKING COEFFICIENTS TO GIVE A SPECIFIC GAIN

If a user wants the input range to correspond to ±1.0 V, it is necessary to pick the per channel gain coefficient. The easiest way is to select the ±1.25 V range, put 1.0 V on the analog input, perform a system full-scale calibration, and record the contents of the per channel gain coefficient.

An alternative mathematical method is as follows: divide the actual input range by the desired input range and multiple by 2^{21}, i.e., multiply 1.25 by 2^{21} = 2621440d, which is 280000h. For this case, 1.25/1.0 is 1.25.

REMEMBER

You must set the mode bits in the mode register to 000 before writing to any of the calibration registers. Otherwise, if a calibration or conversion is in progress, the write will be ignored.

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