

Circuit Note CN-0277

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Devices Connected/Referenced		
AD7960	18-Bit, 5 MSPS PulSAR® Differential ADC	
ADA4897-1/ ADA4897-2	1 nV/√Hz, Low Power, Rail-to-Rail Output Single/Dual Amplifiers	
AD8031/ AD8032	2.7 V, 800 μA, 80 MHz Rail-to-Rail I/O Single/Dual Amplifiers	
ADR4550	Ultralow Noise, High Accuracy Voltage References	

18-Bit, 5 MSPS, Data Acquisition System Optimized for AC Performance

EVALUATION AND DESIGN SUPPORT

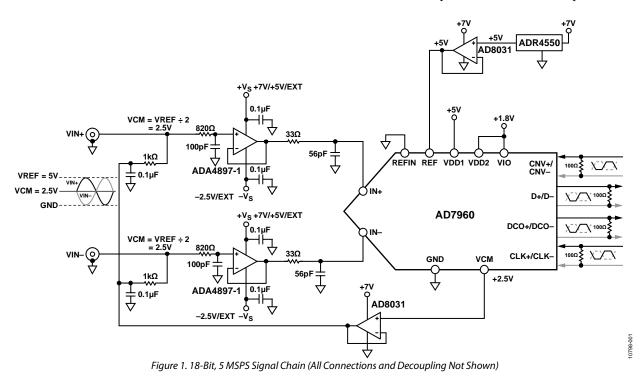
Circuit Evaluation Boards

AD7960 Circuit Evaluation Board (EVAL-AD7960FMCZ) System Demonstration Platform (EVAL-SDP-CH1Z) Design and Integration Files

Schematics, Layout Files, Bill of Materials

CIRCUIT FUNCTION AND BENEFITS

The circuit shown in Figure 1 is an 18-bit, 5 MSPS low power, low noise, high-precision complete data acquisition signalchain solution that dissipates only 122 mW. The reference, reference buffer, driver amplifiers, and ADC provide an optimized solution with industry-leading SNR of 99 dB, THD of -117 dB. The circuit is ideal for portable applications because of its low power and small PCB footprint.



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CIRCUIT DESCRIPTION

The ADA4897-1 is an ideal candidate for driving the AD7960 high precision 18-bit, 5 MSPS SAR ADC. The ADA4897-1 is a low noise (1 nV/ $\sqrt{\text{Hz}}$ typical) and low power (3 mA) rail-to-rail output amplifier that has 230 MHz bandwidth, 120 V/ μ s slew rate, and settles to 0.1% in 45 ns.

The input signals to the ADA4897-1 op amps are filtered by the 820 Ω / 100 pF network that has a bandwidth of 2 MHz. Additional filtering at the input of the AD7960 ADC is provided by the 33 Ω / 56 pF network that has a bandwidth of 86 MHz. The latter filter helps to reduce the kick back coming from the cap DAC input of the AD7960 and limits the noise coming to the AD7960 inputs.

The circuit uses supplies of +7 V and -2.5 V for the input ADA4897-1 drivers to minimize power dissipation and to achieve the optimum system distortion performance. The ADA4897-1 output stage is rail-to-rail and swings to within 150 mV of each supply rail. The additional headroom afforded by the +7 V and -2.5 V supplies provides excellent distortion performance.

The AD7960 differential input range is set by a 5 V or 4.096 V external reference voltage. In Figure 1, the 5 V reference is supplied by the ADR4550 is a high precision, low power (max 950 μ A operating current), low noise voltage reference featuring ±0.02% maximum initial error, excellent temperature stability, and low output noise. The AD8031 is used to buffer the external reference and the common-mode output voltage of the AD7960, and is an ideal for a wide range of applications, from battery-operated systems with large bandwidth to high-speed systems where component density requires lower power dissipation. The AD8031 is also stable for large capacitive loads, and can drive the decoupling capacitors that are required to minimize voltage spikes caused by transient currents.

The AD7960 digital interface uses low voltage differential signaling (LVDS) to enable high data transfer rates. An LVDS CLK+/CLK- signal must be applied to the AD7960 to transfer data to the digital host.

The AD7960, 5MSPS, 18-bit converter has ± 0.8 LSB INL, ± 0.5 LSB DNL, 100 dB DR, and dissipates only 46.5 mW. As shown in Figure 1, the AD7960 is powered from ± 5 V (VDD1) and ± 1.8 V (VDD2 and VIO) supplies. The required 5 V and 1.8 V supplies can be generated using LDOs such as ADP7104 and ADP124.

The AD7960 converts the differential voltage of the antiphase analog inputs (IN+ and IN-) into a digital output. The analog inputs, IN+ and IN-, require a common-mode voltage equal to one-half the reference voltage. The low noise and low power AD8031 amplifier buffers the +5V reference voltage from the low noise and low drift ADR4550 and it also buffers the commonmode output voltage (VCM) of the AD7960. The ADA4897-1 is configured as a unity gain buffer and drives the inputs of the AD7960 with a 0 V to 5 V differential anti-phase (180°out of phase with each other). Figure 2 shows the typical integral nonlinearity as a function of the AD7960 output code is within the specifications of ±0.8 LSB using a 5 V external reference.

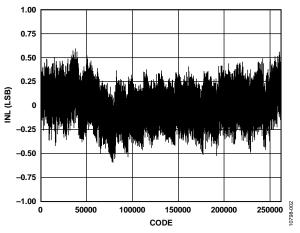


Figure 2. AD7960 Typical Integral Nonlinearity vs. Output Code, REF = 5 V

Histogram and FFT Performance

The precision performance of the circuit shown in the histogram plot in Figure 3 and the FFT plot in Figure 4 using a 5 V external reference . The data was taken using the EVAL-AD7960FMCZ evaluation board and the Audio Precision SYS-2702 as a signal source.

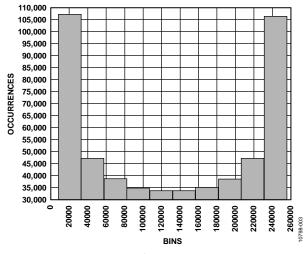
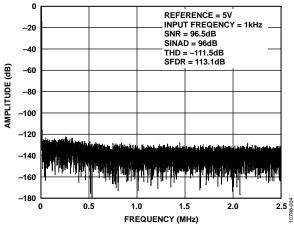
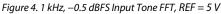


Figure 3. Typical Histogram, REF = 5 V

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Complete schematics and layout of the printed circuit board can be found in the CN-0277 Design Support Package: www.analog.com/CN0277-DesignSupport.

COMMON VARIATIONS

The AD7961 is a 16-bit, 5 MSPS PulSAR* differential ADC and is pin compatible with the AD7960 PulSAR* family, so it can be used in place of the AD7960 in the circuit of Figure 1 when only 16-bit performance is required. The AD7960 series supports either 4.096 V or 5 V external references. The EVAL-AD7960FMCZ board allows either the ADR4540 (4.096 V) or the ADR4550 (5 V) to be selected with a jumper.

The various options for connecting the reference voltage are controlled by the enable EN[0:3] pins of the AD7960 as described in the AD7960 datasheet. If a 0 V to 5 V input range is required, the ADR4550 reference can be used with the AD8031 reference buffer. This is done by setting the enable pins of the AD7960 as EN[0:3] = 'X001' or 'X101'.

The ADA4897-1 and AD8031 single op amps can be replaced with their dual versions (ADA4897-2 and AD8032, respectively) if desired.

For optimized noise and distortion performance, the ADA4899-1 (15 mA), unity-gain stable, ultralow distortion, 1 nV/ \sqrt{Hz} voltage noise, high speed op amp can be used instead of the ADA4897-1 in the circuit if desired.

CIRCUIT EVALUATION AND TEST

The EVAL-AD7960FMCZ evaluation board was developed to evaluate and test the AD7960 ADC. To test the circuit shown in Figure 1, two ADA4897-1 op amps were used to drive the AD7960.

A detailed schematic and user instructions are available in the EVAL-AD7960FMCZ user guide UG-490. This documentation describes how to run the ac/dc tests described in this circuit note.

Note that the user has the option to provide +7 V and -2.5 V supplies for the input amplifiers on the EVAL-AD7960FMCZ board from the external dual power supply.

A functional block diagram of the test setup is shown in Figure 5, and a photograph of the evaluation board is shown in Figure 6

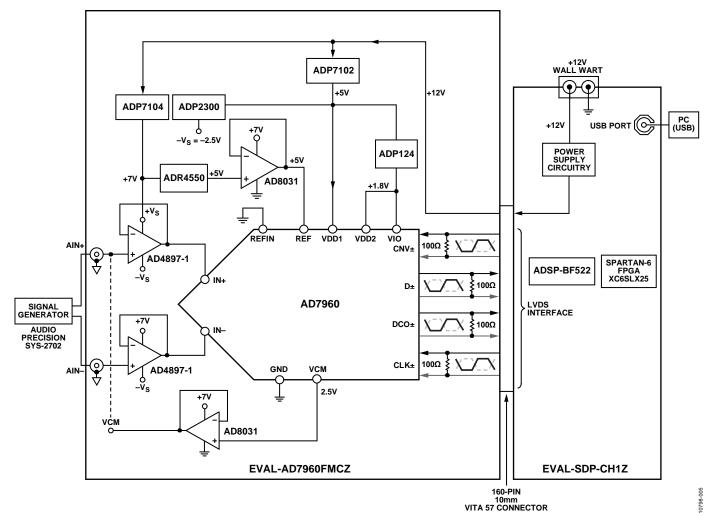
Equipment Required

The following equipment is required to test the circuit:

- The EVAL-AD7960FMCZ Evaluation Board and Software
- The System Demonstration Platform (EVAL-SDP-CH1Z) board
- A low distortion signal generator, such as the Agilent 81150A or Audio Precision SYS2702
- A PC with a USB 2.0 port running Windows[®] XP, Windows Vista, or Windows 7 (32-bit or 64-bit)
- A 12 V dc wall wart (included with EVAL-SDP-CH1Z board)
- USB interface Cable (1) and SMA cable (1)

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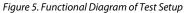




Figure 6. EVAL-AD7960FMCZ Board Connected to EVAL-SDP-CH1Z Board

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LEARN MORE

- CN-0277 Design Support Package: www.analog.com/CN0277-DesignSupport
- CN-0307 Circuit Note, CN-0307 Circuit Note, A 16-Bit, 6 MSPS SAR ADC System with Low Power Input Drivers and Reference Optimized for Multiplexed Applications
- CN-0237 Circuit Note, Ultralow Power, 18-Bit, Differential PulSAR[®] ADC Driver.
- MT-031 Tutorial, *Grounding Data Converters and Solving the Mystery of AGND and DGND*. Analog Devices.
- MT-035 Tutorial, Op Amp Inputs, Outputs, Single-Supply, and Rail-to-Rail Issues. Analog Devices.
- MT-101 Tutorial, Decoupling Techniques. Analog Devices.
- Voltage Reference Wizard Design Tool.
- UG-490 User Guide, *Evaluating the AD7960 18-Bit, 5 MSPS PulSAR Differential ADC*, Analog Devices.
- UG-502 User Guide, SDP-H1 Controller Board, Analog Devices.

Data Sheets and Evaluation Boards

AD7960 Data Sheet and Evaluation Board

ADA4897-1 Data Sheet

ADA4897-2 Data Sheet

ADR4550 Data Sheet

AD8031 Data Sheet

AD8032 Data Sheet

REVISION HISTORY

2/14-Rev. B to Rev. C

Changes to Common Variations Section	3
Changes to Learn More Section	;
12/13—Rev. A to Rev. B	
Changes to Title 1	Ĺ
9/13—Rev. 0 to Rev. A	
Changes to Figure 3	2
8/13—Revision 0: Initial Version	

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