High Temperature, 16-Bit, 600 kSPS PulSAR® ADC

Known Good Die

AD7981-KGD

FEATURES

- **Extreme high temperature operation**
  - **Specified temperature range: −55°C to +175°C**
- **High performance**
  - **16-bit resolution with no missing codes**
  - **600 kSPS throughput with no latency/pipeline delay**
  - **SNR: 91 dB typical at 1 kHz input frequency**
  - **THD: −102 dB typical at 1 kHz input frequency**
  - **INL: ±2.0 LSB maximum, DNL: ±0.9 LSB maximum**
- **Low power dissipation**
  - **2.25 mW typical at 600 kSPS (VDD only)**
  - **4.65 mW typical at 600 kSPS (total)**
  - **70 µW typical at 10 kSPS**
- **Pseudo differential analog input range**
  - **0 V to V_{REF} with V_{REF} between 2.4 V and 5.1 V**
- **Easy to use**
  - **Single-supply 2.5 V operation with 1.8 V/2.5 V/3 V/5 V logic interface**
  - **SPI-/QSPI-/MICROWIRE-/DSP-compatible digital interface**
  - **Daisy-chain multiple ADCs and busy indicator**
- **Known good die (KGD): these die are fully guaranteed to data sheet specifications**

APPLICATIONS

- **Downhole drilling and instrumentation**
- **Avionics**
- **Heavy industrial**
- **High temperature environments**

FUNCTIONAL BLOCK DIAGRAM

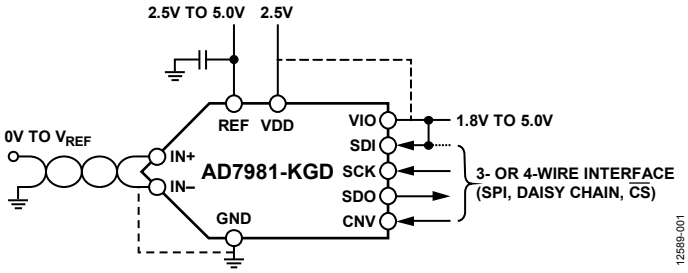

Figure 1.

GENERAL DESCRIPTION

The AD7981-KGD[1] is a 16-bit, successive approximation, analog-to-digital converter (ADC) designed for high temperature operation. The AD7981-KGD is capable of sample rates up to 600 kSPS while maintaining low power consumption from a single power supply, VDD. It is a fast throughput, high accuracy, high temperature, successive approximation register (SAR) ADC and packaged in a small form factor with a versatile serial port interface (SPI).

On the CNV rising edge, the AD7981-KGD samples an analog input, IN+, between 0 V and REF with respect to a ground sense, IN−. The reference voltage, REF, is applied externally and can be set independent of the supply voltage, VDD. The device power scales linearly with throughput.

The SPI-compatible serial interface also features the ability, using the SDI input, to daisy-chain several ADCs on a single, 3-wire bus and provides an optional busy indicator. It is compatible with 1.8 V, 2.5 V, 3 V, or 5 V logic, using the separate supply VIO.

The AD7981-KGD is a member of a growing series of high temperature qualified products offered by Analog Devices, Inc. For a complete selection of available high temperature products, see the high temperature product list and qualification data available at www.analog.com/hightemp.

Additional application and technical information can be found in the AD7981 data sheet.

[1] Protected by U.S. Patent 6,703,961.

Rev. A Document Feedback

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REVISION HISTORY

10/2017—Rev. 0 to Rev. A

Changed Metal Mask Die Image Section to Functional Block Diagram Section 1
Changes to Figure 1 1

4/2015—Revision 0: Initial Version

SPECIFICATIONS

VDD = 2.5 V, VIO = 2.3 V to 5.5 V, V_{REF} = 5 V, T_A = −55°C to +175°C, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RESOLUTION		16			Bits
ANALOG INPUT					
Voltage Range	IN+ − IN−	0		V_{REF}	V
Absolute Input Voltage	IN+	−0.1		V_{REF} + 0.1	V
	IN−	−0.1		+0.1	V
Analog Input Common-Mode Rejection Ratio (CMRR)	f_{IN} = 100 kHz		60		dB
Leakage Current at 25°C	Acquisition phase		1		nA
ACCURACY					
No Missing Codes		16			Bits
Differential Nonlinearity	V_{REF} = 5 V	−0.9	±0.4	+0.9	LSB[1]
	V_{REF} = 2.5 V		±0.5		LSB[1]
Integral Nonlinearity	V_{REF} = 5 V	−2.0	±0.7	+2.0	LSB[1]
	V_{REF} = 2.5 V		±0.6		LSB[1]
Transition Noise	V_{REF} = 5 V		0.75		LSB[1]
	V_{REF} = 2.5 V		1.2		LSB[1]
Gain Error[2]	T_{MIN} to T_{MAX}		±2		LSB[1]
Gain Error Temperature Drift			±0.35		ppm/°C
Zero Error[2]	T_{MIN} to T_{MAX}	−1	±0.08	+1	mV
Zero Temperature Drift			0.45		ppm/°C
Power Supply Sensitivity	VDD = 2.5 V ± 5%		±0.1		LSB[1]
THROUGHPUT					
Conversion Rate		0		600	kSPS
Transient Response	Full-scale step			290	ns
AC ACCURACY[3]					
Dynamic Range	V_{REF} = 5 V		92		dB
	V_{REF} = 2.5 V		87		dB
Oversampled Dynamic Range[4]	OSR = 256		110		dB
Signal-to-Noise Ratio (SNR)	f_{IN} = 1 kHz, V_{REF} = 5 V	89	91		dB
	f_{IN} = 1 kHz, V_{REF} = 2.5 V		86		dB
Spurious-Free Dynamic Range (SFDR)	f_{IN} = 1 kHz		104		dB
Total Harmonic Distortion (THD)	f_{IN} = 1 kHz		−102		dB
Signal-to-Noise-and-Distortion (SINAD)	f_{IN} = 1 kHz, V_{REF} = 5 V		90.5		dB
	f_{IN} = 1 kHz, V_{REF} = 2.5 V		85.5		dB

[1] LSB means least significant bit. With the 5 V input range, 1 LSB is 76.3 µV.
[2] See the Terminology section. These specifications include full temperature range variation, but not the error contribution from the external reference.
[3] All ac accuracy specifications in dB are referred to an input full-scale range (FSR). Tested with an input signal at 0.5 dB below full scale, unless otherwise specified.
[4] The oversampled dynamic range is the ratio of the peak signal power to the noise power (for a small input) measured in the ADC output FFT from dc up to $f_S/(2 \times OSR)$, where f_S is the ADC sample rate and OSR is the oversampling ratio.

VDD = 2.5 V, VIO = 2.3 V to 5.5 V, V_{REF} = 5 V, T_A = −55°C to +175°C, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
REFERENCE					
Voltage Range		2.4		5.1	V
Load Current	600 kSPS, V_{REF} = 5 V		330		µA
SAMPLING DYNAMICS					
−3 dB Input Bandwidth			10		MHz
Aperture Delay	VDD = 2.5 V		2.0		ns
DIGITAL INPUTS					
Logic Levels					
V_{IL}	VIO > 3 V	−0.3		0.3 × VIO	V
	VIO ≤ 3 V	−0.3		0.1 × VIO	V
V_{IH}	VIO > 3 V	0.7 × VIO		VIO + 0.3	V
	VIO ≤ 3 V	0.9 × VIO		VIO + 0.3	µA
I_{IL}		−1		+1	µA
I_{IH}		−1		+1	µA
DIGITAL OUTPUTS					
Data Format		Serial 16 bits straight binary			
Pipeline Delay		Conversion results available immediately after completed conversion			
V_{OL}	I_{SINK} = 500 µA			0.4	V
V_{OH}	I_{SOURCE} = −500 µA	VIO − 0.3			V
POWER SUPPLIES					
VDD		2.375	2.5	2.625	V
VIO	Specified performance	2.3		5.5	V
VIO Range		1.8		5.5	V
Standby Current[1, 2]	VDD and VIO = 2.5 V		0.35		µA
Power Dissipation	VDD = 2.625 V, V_{REF} = 5 V, VIO = 3 V				
Total	10 kSPS		70		µW
	600 kSPS		4.65	7.0	mW
VDD Only	600 kSPS		2.25		mW
REF Only	600 kSPS		1.5		mW
VIO Only	600 kSPS		0.9		mW
Energy per Conversion			7.75		nJ/sample
TEMPERATURE RANGE					
Specified Performance[3]	T_{MIN} to T_{MAX}	−55		+175	°C

[1] With all digital inputs forced to VIO or GND as required.
[2] During the acquisition phase.
[3] Qualified for up to 1000 hours of operation at the maximum temperature rating.

TIMING SPECIFICATIONS

T_A = −55°C to +175°C, VDD = 2.375 V to 2.625 V, VIO = 3.3 V to 5.5 V, unless otherwise stated. See Figure 2 and Figure 3 for load conditions.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit
Conversion Time: CNV Rising Edge to Data Available	t_{CONV}	625		1377	ns
Acquisition Time	t_{ACQ}	290			ns
Time Between Conversions	t_{CYC}	1667			ns
CNV Pulse Width ($\overline{CS}$ Mode)	t_{CNVH}	10			ns
SCK Period ($\overline{CS}$ Mode)	t_{SCK}				
VIO Above 4.5 V		10.5			ns
VIO Above 3 V		12			ns
VIO Above 2.7 V		13			ns
VIO Above 2.3 V		15			ns
SCK Period (Chain Mode)	t_{SCK}				
VIO Above 4.5 V		11.5			ns
VIO Above 3 V		13			ns
VIO Above 2.7 V		14			ns
VIO Above 2.3 V		16			ns
SCK Low Time	t_{SCKL}	4.5			ns
SCK High Time	t_{SCKH}	4.5			ns
SCK Falling Edge to Data Remains Valid	t_{HSDO}	3			ns
SCK Falling Edge to Data Valid Delay	t_{DSDO}				
VIO Above 4.5 V				9.5	ns
VIO Above 3 V				11	ns
VIO Above 2.7 V				12	ns
VIO Above 2.3 V				14	ns
CNV or SDI Low to SDO D15 MSB Valid ($\overline{CS}$ Mode)	t_{EN}				
VIO Above 3 V				10	ns
VIO Above 2.3 V				15	ns
CNV or SDI High or Last SCK Falling Edge to SDO High Impedance ($\overline{CS}$ Mode)	t_{DIS}			20	ns
SDI Valid Setup Time from CNV Rising Edge	$t_{SSDICNV}$	5			ns
SDI Valid Hold Time from CNV Rising Edge ($\overline{CS}$ Mode)	$t_{HSDICNV}$	2			ns
SDI Valid Hold Time from CNV Rising Edge (Chain Mode)	$t_{HSDICNV}$	0			ns
SCK Valid Setup Time from CNV Rising Edge (Chain Mode)	$t_{SSCKCNV}$	5			ns
SCK Valid Hold Time from CNV Rising Edge (Chain Mode)	$t_{HSCKCNV}$	5			ns
SDI Valid Setup Time from SCK Falling Edge (Chain Mode)	$t_{SSDISCK}$	2			ns
SDI Valid Hold Time from SCK Falling Edge (Chain Mode)	$t_{HSDISCK}$	3			ns
SDI High to SDO High (Chain Mode with Busy Indicator)	$t_{DSDOSDI}$			15	ns

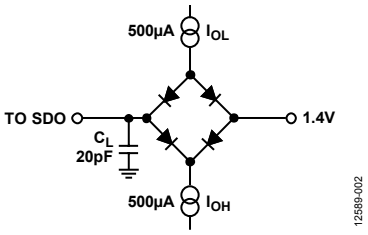

Figure 2. Load Circuit for Digital Interface Timing

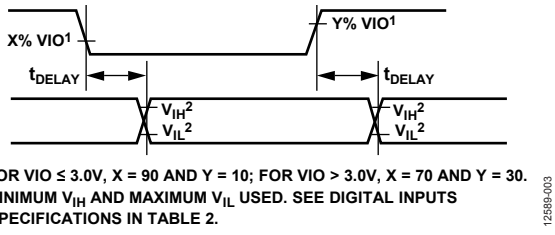

Figure 3. Voltage Levels for Timing

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Analog Inputs	
IN+, IN− to GND	−0.3 V to V_{REF} + 0.3 V or ±130 mA
Supply Voltage	
REF, VIO to GND	−0.3 V to +6 V
VDD to GND	−0.3 V to +3 V
VDD to VIO	+3 V to −6 V
Digital Inputs to GND	−0.3 V to VIO + 0.3 V
Digital Outputs to GND	−0.3 V to VIO + 0.3 V
Storage Temperature Range	−65°C to +150°C
Junction Temperature	176.4°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

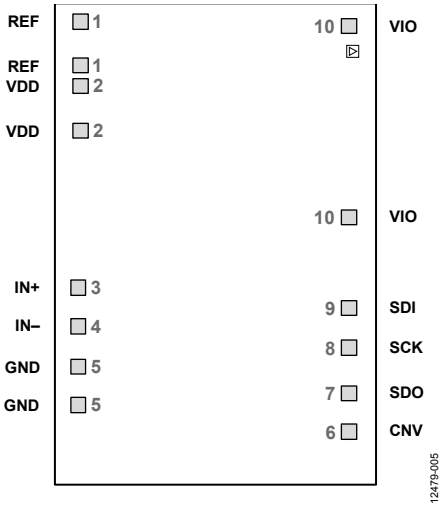

Figure 4. Pad Configuration

Table 5. Pad Function Descriptions

Pad No.	Mnemonic	X-Axis (µm)	Y-Axis (µm)	Pad Type[1]	Description
1	REF	−602	+1014	AI	Reference Input Voltage. The REF range is from 2.4 V to 5.1 V. It is referred to the GND pin.
1	REF	−602	+811	AI	Decouple REF with a 10 µF capacitor as close as possible to the pin.
2	VDD	−602	+719	P	Power Supply.
2	VDD	−602	+517	P	
3	IN+	−616	−198	AI	Analog Input. This pin is referred to IN+. The voltage range, for example, the difference between IN+ and IN−, is 0 V to V_{REF}.
4	IN−	−616	−372	AI	Analog Input Ground Sense. Connect this pin to the analog ground plane or to a remote sense ground.
5	GND	−616	−558	P	Power Supply Ground.
5	GND	−610	−730	P	
6	CNV	+624	−850	DI	Conversion Input. This input has multiple functions. On its leading edge, it initiates the conversions and selects the interface mode of the device: chain mode or $\overline{CS}$ mode. In $\overline{CS}$ mode, it enables the SDO pin when low. In chain mode, read the data when CNV is high.
7	SDO	+624	−675	DO	Serial Data Output. The conversion result is output on this pin. It is synchronized to SCK.
8	SCK	+624	−470	DI	Serial Data Clock Input. When the device is selected, this clock shifts out the conversion result.
9	SDI	+624	−288	DI	Serial Data Input. This input provides multiple features. It selects the interface mode of the ADC as follows: Chain mode is selected if SDI is low during the CNV rising edge. In this mode, SDI is used as a data input to daisy-chain the conversion results of two or more ADCs onto a single SDO line. The digital data level on SDI is output on SDO with a delay of 16 SCK cycles. $\overline{CS}$ mode is selected if SDI is high during the CNV rising edge. In this mode, either SDI or CNV can enable the serial output signals when low. If SDI or CNV is low when the conversion is complete, the busy indicator feature is enabled.
10	VIO	+619	+123	P	Input/Output Interface Digital Power. Nominally it is at the same supply as the host interface (1.8 V, 2.5 V, 3 V, or 5 V).
10	VIO	+622	+993	P	

[1]AI = analog input, DI = digital input, DO = digital output, and P = power.

TERMINOLOGY

Integral Nonlinearity (INL)
INL refers to the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs ½ LSB before the first code transition. Positive full scale is defined as a level 1½ LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line.

Differential Nonlinearity (DNL)
In an ideal ADC, code transitions are 1 LSB apart. DNL is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

Zero Error
The first transition occurs at a level ½ LSB above analog ground (38.1 µV for the 0 V to 5 V range). The offset error is the deviation of the actual transition from that point.

Gain Error
The last transition (from 111 … 10 to 111 … 11) occurs for an analog voltage 1½ LSB below the nominal full scale (4.999886 V for the 0 V to 5 V range). The gain error is the deviation of the actual level of the last transition from the ideal level after the offset is adjusted out.

Spurious-Free Dynamic Range (SFDR)
SFDR is the difference, in decibels (dB), between the rms amplitude of the input signal and the peak spurious signal.

Effective Number of Bits (ENOB)
ENOB is a measurement of the resolution with a sine wave input. It is related to SINAD by the following formula:

$$ENOB = (SINAD_{dB} - 1.76)/6.02$$

and is expressed in bits.

Noise-Free Code Resolution
Noise-free code resolution is the number of bits beyond which it is impossible to distinctly resolve individual codes. It is calculated as

$$\text{Noise-}Free\ Code\ Resolution = \log_2(2^N/Peak\text{-}to\text{-}Peak\ Noise)$$

and is expressed in bits.

Effective Resolution
Effective resolution is calculated as

$$Effective\ Resolution = \log_2(2^N/RMS\ Input\ Noise)$$

and is expressed in bits.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in dB.

Dynamic Range
Dynamic range is the ratio of the rms value of the full scale to the total rms noise measured with the inputs shorted together. It is measured with a signal at −60 dBFS to include all noise sources and DNL artifacts. The value for dynamic range is expressed in dB.

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in dB.

Signal-to-Noise-and-Distortion (SINAD) Ratio
SINAD is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in dB.

Aperture Delay
Aperture delay is the measure of the acquisition performance. It is the time between the rising edge of the CNV input and when the input signal is held for a conversion.

Transient Response
Transient response is the time required for the ADC to accurately acquire its input after a full-scale step function is applied.

OUTLINE DIMENSIONS

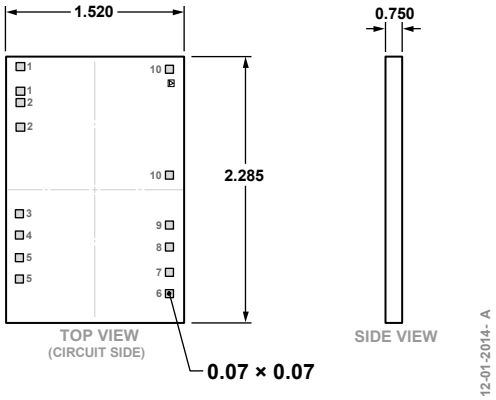

Figure 5. 10-Pad Bare Die [CHIP]
(C-10-5)
Dimensions shown in millimeters

DIE SPECIFICATIONS AND ASSEMBLY RECOMMENDATIONS

Table 6. Die Specifications

Parameter	Value	Unit
Chip Size	1440 × 2205	µm
Scribe Line Width	80 × 80	µm
Die Size	1520 × 2285	µm
Thickness	750	µm
Bond Pad	70 × 70	µm
Bond Pad Composition	0.5 AlCu	%
Backside	Standard assembly die attach	Not applicable
Passivation	Oxynitride	Not applicable

Table 7. Assembly Recommendations

Assembly Component	Recommendation
Die Attach	Epoxy adhesive
Bonding Method	Gold ball[1] or aluminum wedge
Bonding Sequence	Bond pin five first

[1] Evaluate the gold wire for suitability before use at elevated temperatures for extended durations.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD7981-KGD-WP	−55°C to +175°C	10-Pad Bare Die [CHIP]	C-10-5