High Speed Switches

For more information on ADI High Speed Switches, visit *www.analog.com*.

Categories		Features					Parameters																
Part Number	Model	Format	Gain (V/V)	Control Interface (Serial/ Parallel)	Output Disable (Individual) (Y/N)	Shut-down (Y/N)	Supply Voltage (Volts Nominal)	Supply Current (mA Typ)	Output Swing (Volts Typ)	Output Current (mA Typ)	Output Capacitance, Disabled (pF Typ)	Input V_{OS} (mV Max)	Input Voltage Noise (nV/√Hz Typ)	Diff Gain, R_L = 150 V (% Typ)	Diff Phase, R_L = 150 V (° Typ)	–3 dB Bandwidth @ A_{CL} Min (MHz Typ)	0.1 dB Flatness (MHz Typ)	Slew Rate (V/ms Typ)	Isolation @ 10 MHz (dB Typ)	All Hostile Crosstalk @ 10 MHz (dB Typ)	Channel Switch Time (ns Typ)	Price @ 100[1] (OEM $U.S.)	Package
Analog Buffered Multiplexer																							
AD8074	ARU	Buff	+1	—	Y	N	±5	30	±3.2	40	2.2	27	19.5	0.01	0.01	600	70	1350	90	80	—	3.12	16-lead TSSOP
AD8075	ARU	Buff	+2	—	Y	N	±5	30	±3.2	40	2.2	40	22	0.01	0.01	550	65	1600	90	74	—	3.12	16-lead TSSOP
AD8170	AN, AR	2:1	Resistor programmable	—	N	N	±5	8.7	±4.25	50	n/a	9	10	0.02	0.05	250	85	1000	n/a	68	7.5	2.65	8-lead SOIC
AD8174	AN, AR	4:1	Resistor programmable	—	Y	Y	±5	9.7	±4.25	50	7.5	9	10	0.02	0.05	250	85	1000	82	70	7.5	4.65	14-lead SOIC
AD8180	AN, AR	2:1	+1	—	Y	N	±5	3.8	±3.1	20	1.7	12	4.5	0.02[2]	0.02[2]	930	100	750	84	77	5	2.29	8-lead SOIC
AD8182	AN, AR	Dual 2:1	+1	—	Y	N	±5	6.8	±3.1	20	1.7	12	4.5	0.02[2]	0.02[2]	780	100	750	84	75	5	3.47	14-lead SOIC
AD8183	ARU	Triple 2:1 mux	+1	—	Y	N	±5	25	±2.95	32.5	4	25	28	0.01	0.02	590	90	1000	100	84	15	3.47	24-lead TSSOP
AD8184	AN, AR	4:1	+1	—	Y	N	±5	4.4	±3.2	20	3.2	8	4.5	0.01[2]	0.01[2]	700	75	750	109	88	5	2.59	14-lead SOIC
AD8185	ARU	Triple 2:1 mux	+2	—	Y	N	±5	25	±2.95	32.5	6.5	40	15	0.01	0.02	360	60	1150	100	72	15	3.47	24-lead TSSOP
AD8186	ARU	Triple 2:1 mux	+1	—	Y	N	5	18.5	3	20	1.5	6.5	7	0.05	0.05	1000	90	1600	76	79	3.6	3.24	24-lead TSSOP
AD8187	ARU	Triple 2:1 mux	+2	—	Y	N	5	19.5	2.7	18	2	7	9	0.05	0.05	1000	85	1500	92	74	4	3.24	24-lead TSSOP
Analog Crosspoint Switch																							
AD8106	AST	16 × 5	+1	Par	Y	N	±5	30	±3	40	2	20	15	0.02	0.02	390	80	500	93	70	25	9.26	80-lead LQFP
AD8107	AST	16 × 5	+2	Par	Y	N	±5	30	±3	40	2	20	15	0.02	0.02	260	57	500	99	80	25	9.26	80-lead LQFP
AD8108	AST	8 × 8	+1	Ser/Par	Y	N	±5	43	±3	40	2	20	15	0.02	0.02	325	70	400	93	76	25	25.88	80-lead LQFP
AD8109	AST	8 × 8	+2	Ser/Par	Y	N	±5	43	±3	40	2	20	15	0.02	0.02	250	65	480	98	83	25	25.88	80-lead LQFP
AD8110	AST	16 × 8	+1	Ser/Par	Y	N	±5	49	±3	40	2	20	15	0.02	0.02	390	80	500	93	70	25	44.12	80-lead LQFP
AD8111	AST	16 × 8	+2	Ser/Par	Y	N	±5	49	±3	40	2	20	15	0.02	0.02	260	57	500	99	80	25	44.12	80-lead LQFP
AD8113	JST	16 × 16	+2	Ser/Par	Y	N	±12, ±5	60	±10, ±3	20, 40	5	10	14	0.1	0.1	60	10	120	90	52	100	29.94	100-lead LQFP
AD8114	AST	16 × 16	+1	Ser/Par	Y	N	±5	70	±3.3	40	5	15	16	0.05	0.05	225	25	375	90	60	50	89.99	100-lead LQFP
AD8115	AST	16 × 16	+2	Ser/Par	Y	N	±5	80	±3.3	40	5	15	18	0.05	0.05	200	40	450	90	52	50	89.99	100-lead LQFP
AD8116	JST	16 × 16	+1	Ser	Y	N	±5	80	±3	40	5	45	15	0.01	0.01	200	60	300	105	60	50	105.88	128-lead LQFP

Digital Crosspoint Switch

Part Number	Model	Format	Typical Data Rate (Gb/s)	Control Interface (Serial/ Parallel)	Output Disable (Individual) (Y/N)	Output Current (mA)	Supply Voltage (Volts Nominal)	Supply Current Enable/Disable (mA Typ)	Minimum Input Swing (mV p-p)	Input Voltage Range (V)	Input Bias Current (mA Typ)	Input Capacitance (pF Typ)	Output Swing (mV p-p Typ)	Output Voltage Range (V)	Output Capacitance, Disabled (pF Typ)	Channel Jitter @ Typ Rate (ps, p-p, Typ)	Prop Delay In to Out (ps Typ)	Prop Delay Match (ps Max)	Output Rise/ Fall Time 20% to 80% (ps Max)	Price @ 100[1] (OEM $U.S.)	Package
AD8150	AST	33 × 17	1.5	CMOS/TTL parallel	Y	2 to 25 Resistor programmable	3.3, 5 ECL/PECL	400/20	300	(V_{CC} – 2) to V_{CC}	2	2	800	(V_{CC} – 1.8) to V_{CC}	2	50	600	200	100	135.00	184-lead LQFP
AD8151	AST	33 × 17	2.5	CMOS/TTL parallel	Y	2 to 25 Resistor programmable	3.3, 5 ECL/PECL	450/35	200	(V_{CC} – 2) to V_{CC}	2	2	800	(V_{CC} – 1.8) to V_{CC}	2	50	600	200	100	202.50	184-lead LQFP
AD8152	JBP	34 × 34	3.2	LVCMOS/ LVTTL parallel	Y	Digitally programmable	2.5, 3.3 LVPECL/ CML	770/32	50	V_{ee} to 0.8 to V_{CC} to 0.2	2	2	800	(V_{CC} – 1.2) to (V_{CC} +0.2)	2	45	660	120	100	234.00	256-lead SBGA

[1]USD 100s, recommended resale, FOB U.S.A. [2]R_L = 1 kΩ

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