

Circuit Note CN-0275

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Devices Connected/Referenced	
AD8147	Triple Video Driver for Wideband Video
AD8122	Triple Differential Receiver with Adjustable Line Equalization
AD8120	Triple Skew-Compensating Video Delay Line with Analog and Digital Control

# Complete Broadband Video-over-UTP Driver and Receiver Solution for RGB, YPbPr, and More

# **EVALUATION AND DESIGN SUPPORT**

### **Design and Integration Files**

Schematics, Layout Files, Bill of Materials

## **CIRCUIT FUNCTION AND BENEFITS**

Originally intended to carry local area network (LAN) traffic, the unshielded twisted pair (UTP) cable, such as Category-5e (Cat-5e), has become an economical solution in many other signal transmission applications because of its respectable performance and low cost. Among these applications are systems that transport broadband video signals in which three of the four twisted pairs in the cable carry the red, green, and blue (RGB) computer video signals or the luminance and two color difference (YPbPr), high definition component video signals. The required horizontal and vertical synchronization pulses can be embedded in the video signal blanking intervals, or these pulses can be carried as common-mode difference signals among the three pairs. These systems often include video crosspoint switches and are used to distribute video signals from a small number of sources to many displays, as in digital signage applications, or from a large number of sources to a small number of displays, as in keyboard-video-mouse (KVM) networks.

Signals transported over UTP cable suffer from three major impairments that degrade video quality:

- Nonlinear bandlimiting due to the skin effect, resulting in signal dispersion and loss of high frequency signal content. This impairment results in loss of image sharpness and dark streaking.
- Low frequency flat loss due to resistive loss that reduces image contrast.
- Delay skew between the four twisted pairs that stems from the unequal twist rates (lay lengths), which are used to minimize crosstalk between the pairs. Delay skew produces color errors in the received image due to the misalignment in time of the three received signals.

The solution shown in Figure 1 overcomes these impairments by using the AD8122 triple receiver/equalizer to restore the high frequency content of the video signals while also providing flat gain. The AD8120 triple skew-compensating, analog delay line adds delay to the two earliest arriving signals so that the three received signals are properly aligned in time. The AD8147 triple driver provides the required single-ended-to-differential conversion of the source video signals.

Rev. A

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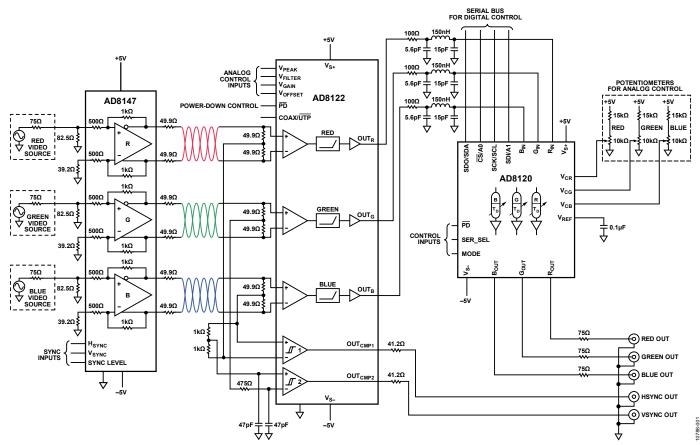


Figure 1. Equalized and Delay Compensated UTP Driver and Receiver (Simplified Schematic: All Pins, Connections, and Decoupling Not Shown)

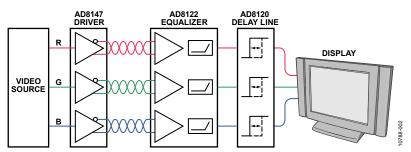


Figure 2. Simplified System Block Diagram for Video-over-UTP System

### **CIRCUIT DESCRIPTION**

The video transmission system shown in Figure 1 uses RGBHV video signals, where RGB indicates the red, green, and blue video signals, and HV indicates the individual horizontal and vertical synchronization pulse signals. Therefore, five signals are transported over three twisted pair cables.

Video system performance is best characterized in the time domain, and the most important specification is the step response settling time. The transition between two pixels in a video display is nominally a step function, and each pixel lasts for a specific time duration. Ideally, the video step response settles to an imperceptible error level with respect to its final value (approximately 46 dB less than full scale, or 3.5 mV) within a fraction of the pixel time (approximately 6 ns for UXGA at 60 Hz). While some frequency domain performance metrics are important, what matters most is how these metrics affect the video signal in the time domain. For example, the system bandwidth must be sufficient to produce a step response with a rise time that is short enough to meet the settling time specification. However, bandwidth alone is not enough because significant settling errors can occur due to ringing, overshoot, and sluggish response, even with a short rise time attained by having wide system bandwidth. A simplified system block diagram is shown in Figure 2.

### Driver

RGB signals typically originate from 75  $\Omega$ , single-ended, source terminated voltage sources and require 75  $\Omega$  load terminations. At the load, the properly terminated signal amplitudes typically vary between 0 mV and 700 mV. To transport the RGB signals over UTP, the signals are converted from single-ended mode to balanced (differential) mode and then amplified by a factor of two to account for the 6 dB loss incurred due to the UTP source and load terminations. This is easily accomplished by using a triple differential driver, such as the AD8147.

The AD8147 provides an additional feature for encoding the TTL logic level, horizontal and vertical synchronization pulse signals on the three output common-mode voltages ( $V_{OCM}$ ) according to the following equations:

$$Red V_{OCM} = \frac{K}{2} (V_{SYNC} - H_{SYNC}) + V_{MIDSUPPLY}$$
$$Green V_{OCM} = \frac{K}{2} (-2V_{SYNC}) + V_{MIDSUPPLY}$$
$$Blue V_{OCM} = \frac{K}{2} (V_{SYNC} + H_{SYNC}) + V_{MIDSUPPLY}$$

where:

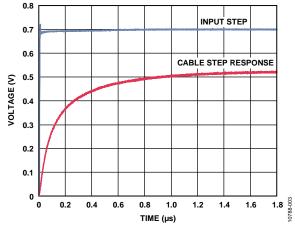
K represents the peak deviation of the common-mode pulse voltage about the midsupply voltage ( $V_{MIDSUPPLY}$ ).

 $V_{SYNC}$  and  $H_{SYNC}$  are unit weighting terms that equal +1 for a Logic 1 and -1 for a Logic 0. This encoding scheme produces a net ac common-mode voltage of zero, minimizing common-mode electromagnetic emissions from the cable.

The driver evaluation board contains everything necessary to implement the single-ended-to-differential mode conversion and sync pulse encoding, including the adjustment of K.

### Receiver

The skin effect in UTP cable produces transmission loss that increases with frequency, causing the received signals to appear rounded and dispersed, and flat resistive loss in the cable occurs due to simple cable resistance. Figure 3 illustrates these effects by comparing the full swing video step response of 300 meters of UTP with the step signal at the input to the cable.



The AD8122 triple equalizer performs differential-to-singleended mode conversion with high common-mode rejection and compensates for these signal impairments. Figure 4 shows the corrected step signal at the equalizer output that settles to 1% error in less than 70 ns. Note that the time scale in Figure 4 is in nanoseconds.

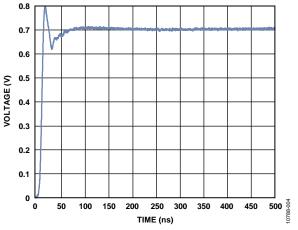
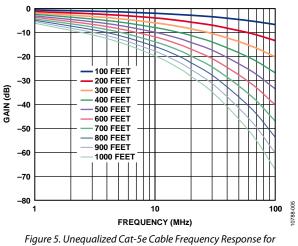


Figure 4. 300 Meter Cat-5e Cable Equalized Step Response (Note Time in ns)

Moving to the frequency domain, Figure 5 illustrates the frequency responses of Cat-5e cables in lengths from 100 feet to 1000 feet, in 100 foot increments, in which the bandlimiting effect and flat loss are clearly evident.



gure 5. Unequalized Cat-5e Cable Frequency Response f Various Cable Lengths

The effectiveness of how the AD8122 restores the received high frequency content of the signals and flat loss can be seen by comparing the equalized frequency responses at the AD8122 output in Figure 6 with the unequalized frequency responses in Figure 5. For 1000 feet (300 meters) of cable, the unequalized loss of more than 50 dB at 60 MHz was improved to 3 dB by the AD8122 equalizer.

Figure 3. 300 Meter Cat-5e Unequalized Cable Step Response

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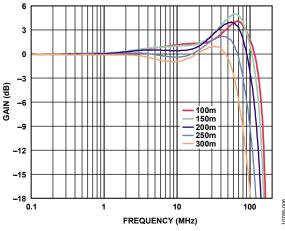


Figure 6. Equalized Cat-5e Cable Frequency Response for Various Cable Lengths

Moving to the final impairment, the AD8120 triple delay line corrects the time skew among the three pairs and provides a gain of two to drive the video signals over doubly terminated, 75  $\Omega$  cables to the display.

The receiver evaluation board contains the AD8122 and AD8120, and all the necessary support circuitry, including five potentiometers to manually adjust the high frequency boost, flat gain, and three delay lines. In addition, a serial interface is provided for optional serial control of the AD8120.

## Conclusion

The quality of the image presented at the far end is what is important in video distribution systems. The quality of the image is determined by the step response settling time to approximately 3.5 mV of the final value, which begins to affect image quality when it extends beyond a fraction of a pixel. Figure 7 shows an extreme case of an image received over 300 meters (1000 feet) of Cat-5e cable with no equalization or skew correction applied. Figure 7 shows significant dark smearing, indicative of a sluggish step response, and color offsets due to time skew. The fully corrected image is shown in Figure 8.



Figure 7. Unequalized and No Skew Correction Applied to Image Transmitted Over 300 Meter Cat-5e Cable



Figure 8. Equalized and Skew Corrected Image Transmitted over 300 Meter Cat-5e Cable

# **Circuit Note**

Photographs of the transmitter and receiver evaluation boards are shown in Figure 9 and Figure 10, respectively. A complete design support package for the EVAL-CN0275-TX-EBZ transmitter evaluation board and the EVAL-CN0275-RX-EBZ receiver evaluation board, including complete schematics, layout files, and bill of materials, is available at www.analog.com/CN0275-DesignSupport.

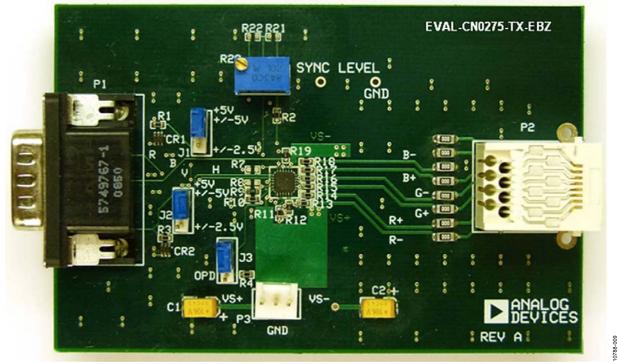


Figure 9. EVAL-CN0275-TX-EBZ Transmitter Evaluation Board



*Figure 10. EVAL-CN0275-RX-EBZ Receiver Evaluation Board* 

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# **COMMON VARIATIONS**

The lower cost AD8124 triple equalizer is a viable substitute for the AD8122 in systems that only need to drive up to 200 meters of UTP. The AD8124 is not pin-compatible with the AD8122 and is somewhat different in its control functions.

There are a number of options with regard to drivers besides the AD8147. The AD8146 provides the same functionality as the AD8147 but does not include the dedicated sync-on-commonmode circuitry. The AD8146 is typically used in systems that place the vertical and horizontal synchronization pulses in the blanking intervals of the video signal instead of on the common-mode voltages. The AD8148 is the same as the AD8147 but has a fixed gain of four instead of two, and it can be configured to provide pre-emphasis to drive up to 100 feet of UTP. For systems that require lower power consumption, the AD8133 and AD8134 provide the same functionality as the AD8146 and AD8147, respectively, and consume less power, but have less bandwidth. Finally, for the lowest cost systems that can run on 5 V, the AD8141 and AD8142 CMOS drivers may be the best choice.

UTP installations vary widely and can cover wide areas, pass through multiple patch bays, and at times have no ground reference. These and other conditions can cause large fluctuations in the received common-mode voltage relative to the local receiver ground reference. Placing a flat gain differential receiver with a wide common-mode range, such as the AD8143, in front of the equalizer can provide up to 21 V of input common-mode range in these demanding situations.

The AD8122 and AD8124 both support coaxial cable as well as UTP cable. The AD8122 can be pin strapped to either mode, and the AD8124 uses a  $V_{\text{POLE}}$  control to modify its frequency response to support either cable type.

# **CIRCUIT EVALUATION AND TEST**

Complete system level, plug-and-play driver and receiver evaluation boards were built that contained all of the necessary circuitry video graphics array (VGA) and RJ-45 connectors. Potentiometers with knobs were provided to control equalization and skew correction. The best test configuration was a simple video source, such as a PC and a good quality display. The PC and display were capable of supporting resolutions of up to UXGA at 60 Hz.

## **Equipment Needed**

The following equipment was used:

- An UXGA video source (laptop computer)
- The EVAL-CN0275-TX-EBZ transmitter evaluation board (not available for sale)
- The EVAL-CN0275-RX-EBZ receiver evaluation board (not available for sale)
- ±5 V power supplies (two: one for the Tx board and one for the Rx board)
- Cat-5e cable, 100 feet through 1000 feet in 100 foot increments (Stellar Labs U5E-24-CMR-665, MCM Electronics #24-10510)
- An UXGA video display

### Test

The simplified block diagram of the test setup is shown in Figure 11. After connecting the equipment, standard video tests were used to perform end-to-end testing.

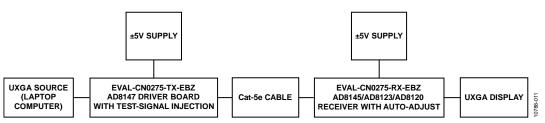


Figure 11. Video-Over-UTP Auto Adjust Test Configuration Functional Block Diagram

### LEARN MORE

CN-0275 Design Support Package: www.analog.com/CN0275-DesignSupport.

Ardizzoni, John. A Practical Guide to High-Speed Printed-Circuit-Board Layout. Analog Dialogue 39-09, September 2005.

MT-031 Tutorial, *Grounding Data Converters and Solving the Mystery of "AGND" and "DGND"*, Analog Devices.

MT-101 Tutorial, Decoupling Techniques, Analog Devices.

### Data Sheets and Evaluation Boards

AD8147 Data Sheet

AD8122 Data Sheet

AD8120 Data Sheet

### **REVISION HISTORY**

### 6/15-Rev. 0 to Rev. A

Changes to Evaluation and Design Support Section1
Changes to Circuit Evaluation and Test Section
Changes to Data Sheets and Evaluation Boards Section7

### 8/12-Rev. 0: Initial Version

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