ANALOG DEVICES

Using the AD813x

THEORY OF OPERATION

The AD813x differs from conventional op amps by the external presence of an additional input and output. The additional input, V_{OGM}, controls the output common-mode voltage. The additional output is the analog complement of the single output of a conventional op amp. For its operation, the AD813x makes use of two feedback loops as compared to the single loop of conventional op amps. While this provides significant freedom to create various novel circuits, basic op amp theory can still be used to analyze the operation.

One of the feedback loops controls the output common-mode voltage, $V_{OUT,cm}$. Its input is V_{OCM} (Pin 2) and the output is the common-mode, or average voltage, of the two differential outputs (+OUT and –OUT). The gain of this circuit is internally set to unity. When the AD813x is operating in its linear region, this establishes one of the operational constraints: $V_{OUT,cm} = V_{OCM}$.

The second feedback loop controls the differential operation. Similar to an op amp, the gain and gain-shaping of the transfer function is controllable by adding passive feedback networks. However, only one feedback network is required to "close the loop" and fully constrain the operation. But depending on the function desired, two feedback networks can be used. This is possible as a result of having two outputs that are each inverted with respect to the differential inputs.
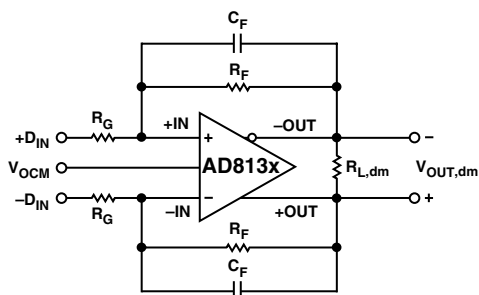
DEFINITION OF TERMS

Figure 1. Circuit Definitions

Differential voltage refers to the difference between two node voltages. For example, the output differential voltage (or equivalently output differential-mode voltage) is defined as:

$$V_{OUT,dm} = (V_{+OUT} - V_{-OUT}) \qquad (1)$$

V_{+OUT} and V_{-OUT} refer to the voltages at the +OUT and –OUT terminals with respect to a common reference.

Common-mode voltage refers to the average of two node voltages. The output common-mode voltage is defined as:

$$V_{OUT,cm} = (V_{+OUT} + V_{-OUT}) / 2 \qquad (2)$$

PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Function
1	–IN	Negative Input
2	V_{OCM}	Voltage applied to this pin sets the common-mode output voltage with a ratio of 1:1. For example, 1 V dc on VOCM will set the dc bias level on +OUT and –OUT to 1 V.
3	V+	Positive Supply Voltage
4	+OUT	Positive Output. Note: The voltage at $-D_{IN}$ is inverted at +OUT.
5	–OUT	Negative Output. Note: The voltage at $+D_{IN}$ is inverted at –OUT.
6	V–	Negative Supply Voltage
7	NC	No Connect
8	+IN	Positive Input

GENERAL USAGE OF THE AD813x

Several assumptions are made here for a first-order analysis, which are the typical assumptions used for the analysis of op amps:
- The input impedances are arbitrarily large and their loading effect can be ignored.
- The input bias currents are sufficiently small so they can be neglected.
- The output impedances are arbitrarily low.
- The open-loop gain is arbitrarily large, which drives the amplifier to a state where the input differential voltage is effectively zero.
- Offset voltages are assumed to be zero.

REV. 0

While it is possible to operate the AD813x with a purely differential input, many of its applications call for a circuit that has a single-ended input with a differential output.

For a single-ended-to-differential circuit, the R_G of the undriven input will be tied to a reference voltage. For now this is ground. Other conditions will be discussed later. Also, the voltage at V_{OCM}, and hence $V_{OUT,cm}$ will be assumed to be ground for now. Figure 2 shows a generalized schematic of such a circuit using an AD813x with two feedback paths.
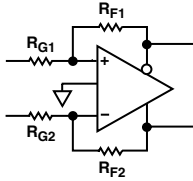

Figure 2. Typical Four-Resistor Feedback Circuit

For each feedback network, a feedback factor can be defined, which is the fraction of the output signal that is fed back to the opposite-sign input. These terms are:

$$\beta 1 = R_{G1} / (R_{G1} + R_{F1}) \qquad (3)$$

$$\beta 2 = R_{G2} / (R_{G2} + R_{F2}) \qquad (4)$$

The feedback factor $\beta 1$ is for the side that is driven, while the feedback factor $\beta 2$ is for the side that is tied to a reference voltage (ground for now). Note also that each feedback factor can vary anywhere between 0 and 1.

A single-ended-to-differential gain equation can be derived that is true for all values of $\beta 1$ and $\beta 2$:

$$G = 2 \times (1 - \beta 1) / (\beta 1 + \beta 2) \qquad (5)$$

This expression is not very intuitive. One observation that can be made right away is that a tolerance error in $\beta 1$ does not have the same effect on gain as the same tolerance error in $\beta 2$.

For $R_{F1}/R_{G1} = R_{F2}/R_{G2}$ the gain equation simplifies to $G = R_F/R_G$.

BASIC CIRCUIT OPERATION
One of the more useful and easy to understand ways to use the AD813x is to provide two equal-ratio feedback networks. To match the effect of parasitics, these networks should actually be comprised of two equal-value feedback resistors, R_F and two equal-value gain resistors, R_G. This circuit is diagrammed in Figure 1.

Like a conventional op amp, the AD813x has two differential inputs that can be driven with both a differential-mode input voltage, $V_{IN,dm}$, and a common-mode input voltage, $V_{IN,cm}$. Another input, V_{OCM}, is not present on conventional op amps, but provides another input to consider on the AD813x. It is totally separate from the above inputs. There are also two complementary outputs whose response can be defined by a differential-mode output, $V_{OUT,dm}$ and a common-mode output, $V_{OUT,cm}$.

Table I indicates the gain from any type of input to either type of output.

Table I. Differential and Common-Mode Gains

Input	$V_{OUT,dm}$	$V_{OUT,cm}$
$V_{IN,dm}$	R_F/R_G	0 (By Design)
$V_{IN,cm}$	0	0 (By Design)
V_{OCM}	0	1 (By Design)

The differential output ($V_{OUT,dm}$) is equal to the differential input voltage ($V_{IN,dm}$) times R_F/R_G. In this case, it does not matter if both differential inputs are driven, or only one output is driven and the other is tied to a reference voltage, like ground. As can be seen from the two zero entries in the first column, neither of the common-mode inputs has any effect on this gain.

The gain from $V_{IN,dm}$ to $V_{OUT,cm}$ is 0 and to first-order does not depend on the ratio matching of the feedback networks. The common-mode feedback loop within the AD813x provides a corrective action to keep this gain term minimized. The term "balance error" describes the degree to which this gain term differs from zero.

The gain from $V_{IN,cm}$ to $V_{OUT,dm}$ does directly depend on the matching of the feedback networks. The analogous term for this transfer function, which is used in conventional op amps, is "common-mode rejection ratio" or CMRR. Thus, if it is desirable to have a high CMRR, the feedback ratios must be well matched.

The gain from $V_{IN,cm}$ to $V_{OUT,cm}$ is also ideally 0, and is first-order independent of the feedback ratio matching. As in the case of $V_{IN,dm}$ to $V_{OUT,cm}$, the common-mode feedback loop keeps this term minimized.

The gain from V_{OCM} to $V_{OUT,dm}$ is ideally 0 only when the feedback ratios are matched. The amount of differential output signal that will be created by varying V_{OCM} is related to the degree of mismatch in the feedback networks.

V_{OCM} controls the output common-mode voltage $V_{OUT,cm}$ with a unity-gain transfer function. With equal-ratio feedback networks (as assumed above), its effect on each output will be the same, which is another way to say that the gain from V_{OCM} to $V_{OUT,dm}$ is zero. If not driven, the output common-mode will be at mid-supplies. It is recommended that a 0.1 µF bypass resistor be connected to V_{OCM}.

When unequal feedback ratios are used, the two gains associated with $V_{OUT,dm}$ become nonzero. This significantly complicates the mathematical analysis along with any intuitive understanding of how the part operates. Some of these configurations will be in another section.

ESTIMATING THE OUTPUT NOISE VOLTAGE

Similar to the case of a conventional op amp, the differential output errors (noise and offset voltages) can be estimated by multiplying the input referred terms, at +IN and –IN, by the circuit noise gain. The noise gain is defined as:

$$G_N = 1 + \left(\frac{R_F}{R_G} \right) \qquad (6)$$

To compute the total output referred noise for the circuit of Figure 1, consideration must also be given to the contribution of the resistors R_F and R_G. Refer to Table II for estimated output noise voltage densities at various closed-loop gains.

Table II. Recommended Resistor Values and Noise Performance for Specific Gains

Gain	R_G (Ω)	R_F (Ω)	Bandwidth –3 dB	Output Noise AD813x	Output Noise AD813x + R_G, R_F
1	499	499	360 MHz	16 nV/Hz	17 nV/Hz
2	499	1.0 k	160 MHz	24.1 nV/Hz	26.1 nV/Hz
5	499	2.49 k	65 MHz	48.4 nV/Hz	53.3 nV/Hz
10	499	4.99 k	20 MHz	88.9 nV/Hz	98.6 nV/Hz

CALCULATING AN APPLICATION CIRCUIT'S INPUT IMPEDANCE

The effective input impedance of a circuit such as that in Figure 1, at +D_{IN} and –D_{IN}, will depend on whether the amplifier is being driven by a single-ended or differential signal source. For balanced differential input signals, the input impedance ($R_{IN,dm}$) between the inputs (+D_{IN} and –D_{IN}) is simply:

$$R_{IN,dm} = 2 \times R_G \qquad (7)$$

In the case of a single-ended input signal (for example if –D_{IN} is grounded and the input signal is applied to +D_{IN}), the input impedance becomes:

$$R_{IN,dm} = \left(\frac{R_G}{1 - \dfrac{R_F}{2 \times (R_G + R_F)}} \right) \qquad (8)$$

The circuit's input impedance is effectively higher than it would be for a conventional op amp connected as an inverter because a fraction of the differential output voltage appears at the inputs as a common-mode signal, partially bootstrapping the voltage across the input resistor R_G.

INPUT COMMON-MODE VOLTAGE RANGE IN SINGLE-SUPPLY APPLICATIONS

The AD813x is optimized for level-shifting "ground" referenced input signals. For a single-ended input this would imply, for example, that the voltage at –D_{IN} in Figure 1 would be zero volts when the amplifier's negative power supply voltage (at V–) was also set to zero volts.

SETTING THE OUTPUT COMMON-MODE VOLTAGE

The AD813x's V_{OCM} pin is internally biased at a voltage approximately equal to the mid-supply point (average value of the voltages on V+ and V–). Relying on this internal bias will result in an output common-mode voltage that is within about 100 mV of the expected value. In cases where more accurate control of the output common-mode level is required, it is recommended that an external source, or resistor divider (with $R_{SOURCE} < 10$ kΩ), be used.

APPLICATION NOTES FOR THE AD813x DIFFERENTIAL AMPS ADC DRIVING
High-Performance ADC Driving

The circuit in Figure 3 shows a simplified front-end connection for an AD813x driving an AD9224, a 12-bit, 40 MSPS A/D converter. The A/D works best when driven differentially, which minimizes its distortion as described in its data sheet. The AD813x eliminates the need for a transformer to drive the ADC and performs single-ended-to-differential conversion, common-mode level-shifting, and buffering of the driving signal.

The positive and negative outputs of the AD813x are connected to the respective differential inputs of the AD9224 via a pair of 49.9 Ω resistors to minimize the effects of the switched-capacitor front-end of the AD9224. For best distortion performance it is run from supplies of ±5 V.

The AD813x can also be configured with unity gain for a single-ended input-to-differential output. The additional 23 Ω, 522 Ω total, at the input to –IN is to balance the parallel impedance of the 50 Ω source and its 50 Ω termination that drives the noninverting input.

The signal generator has a ground-referenced, bipolar output, i.e., it drives symmetrically above and below ground. Connecting V_{OCM} to the CML pin of the AD9224 sets the output common-mode of the AD813x at 2.5 V, which is the mid-supply level for the AD9224. This voltage is bypassed by a 0.1 μF capacitor.

The full-scale analog input range of the AD9224 is set to 4 V p-p, by shorting the SENSE terminal to AVSS. This has been determined to be the scaling to provide minimum harmonic distortion.

For the AD813x to swing a 4 V p-p, each output swings 2 V p-p, while providing signals that are 180 degrees out of phase. With a common-mode voltage at the output of 2.5 V, this means that each AD813x output will swing between 1.5 V and 3.5 V.

A ground-referenced 4 V p-p, 5 MHz signal at $D_{IN}+$ was used to test the circuit in Figure 3. When the combined-device circuit was run with a sampling rate of 20 MHz MSPS, the SFDR (spurious free dynamic range) was measured at –85 dBc.
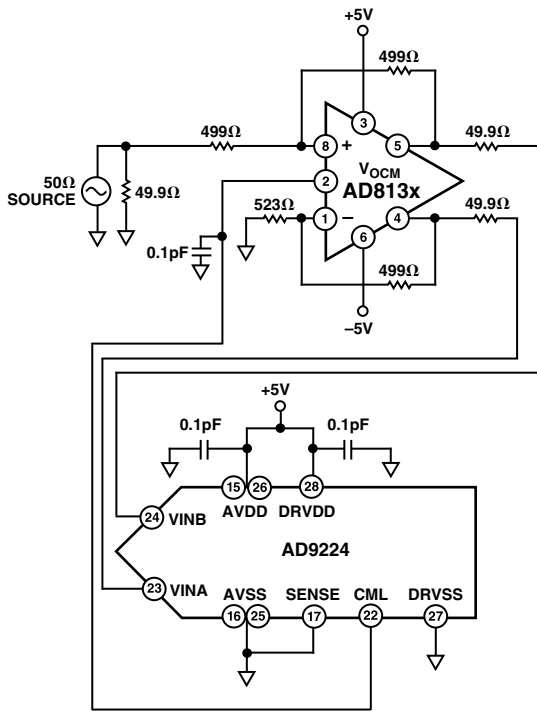

Figure 3. AD813x Driving an AD9224, a 12-Bit, 40 MSPS A/D Converter

SINGLE 3 V SUPPLY DIFFERENTIAL A-TO-D DRIVER

Many newer A-to-D converters can run from a single 3 V supply, which can save significant system power. In order to increase the dynamic range at the analog input, they have differential inputs, which doubles the dynamic range with respect to a single-ended input. An added benefit of using a differential input is that the distortion can be improved.

The low distortion and ability to run from a single 3 V supply make the AD813x suitable as an A-to-D driver for some 10-bit, single-supply applications. Figure 4 shows a schematic of a circuit for an AD813x driving an AD9203, 10-bit, 40 MSPS A-to-D converter.
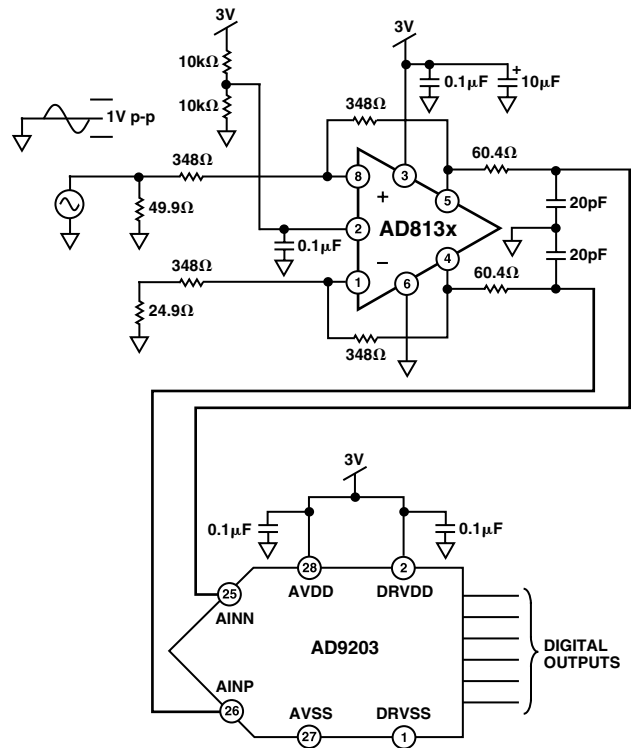

Figure 4. AD813x Driving AD9203, a 10-Bit 40 MSPS A/D Converter

The common-mode of the AD813x output is set at mid-supply by the voltage divider connected to V_{OCM}, and ac bypassed with a 0.1 μF capacitor. This provides for maximum dynamic range between the supplies at the output of the AD813x. The 110 Ω resistors at the AD813x output, along with the shunt capacitors form a one-pole, low-pass filter for lowering noise and antialiasing.

Figure 5 shows an FFT plot that was taken from the combined devices at an analog input frequency of 2.5 MHz

and a 40 MSPS sampling rate. The performance of the AD813x compares very favorably with a center-tapped transformer drive, which has typically been the best way to drive this A-to-D converter. The AD813x has the advantage of maintaining dc performance, which a transformer solution cannot provide.
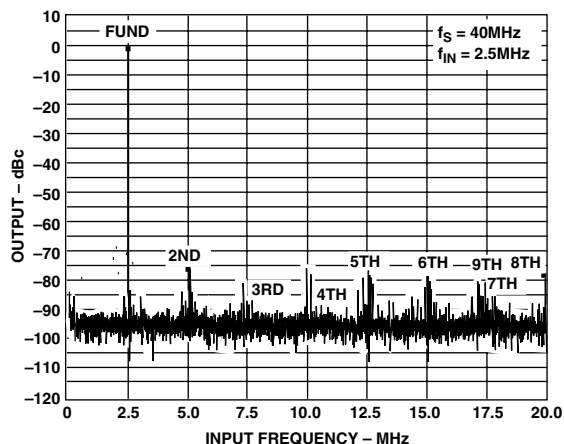

Figure 5. FFT Response for AD813x Driving AD9203

BALANCED LINE DRIVING
TWISTED-PAIR LINE DRIVER
When driving a twisted-pair cable, it is desirable to drive only a pure differential signal onto the line. If the signal is purely differential (i.e., fully balanced), and the transmission line is twisted and balanced, there will be a minimum radiation of any signal.

The complementary electrical fields will mostly be confined to the space between the two twisted conductors and will not significantly radiate out from the cable. The current in the cable will create magnetic fields that will radiate to some degree. However, with each twist, the two adjacent twists will have an opposite polarity magnetic field. If the twist pitch is tight enough, these small magnetic field loops will contain most of the magnetic flux, and the magnetic far-field strength will be negligible.

Any imbalance in the differential drive signal will appear as a common-mode signal on the cable. This is the equivalent of a single wire that is driven with the common-mode signal. In this case, the wire will act as an antenna and radiate. Thus, in order to minimize radiation when driving differential twisted-pair cables, the differential drive signal should be very well balanced.

The common-mode feedback loop in the AD813x helps to minimize the amount of common-mode voltage at the output, and therefore can be used to create a well-balanced differential line driver.

Figure 6 shows a circuit of an AD813x driving a twisted-pair line, like a Category 3 or Category 5 (Cat3 or Cat5), already installed in many buildings for telephony and data communications. The characteristic impedance of such transmission lines is usually about 100 Ω. The outstanding balance of the AD813x output will minimize the common-mode signal and therefore the amount of EMI generated by driving the twisted pair.
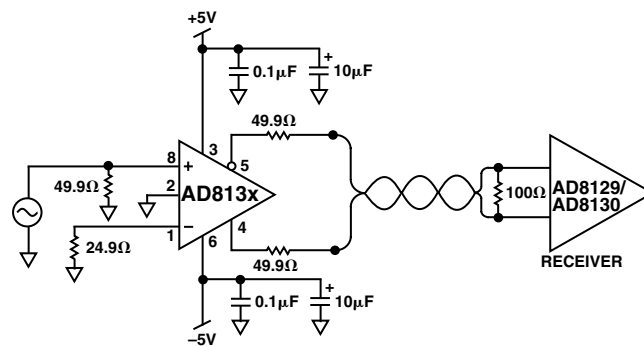

Figure 6. Single-Ended-to-Differential 100 Ω Line Driver

The two resistors in series with each output terminate the line at the transmit end. Since the impedances of the outputs of the AD813x are very low, they can be thought of as a short circuit, and the two terminating resistors form a 100 Ω termination at the transmit end of the transmission line. The receive end is directly terminated by a 100 Ω resistor across the line.

This back-termination of the transmission line divides the output signal by two. The fixed gain-of-two of the AD813x will create a net unity gain for the system from end to end.

In this case, the input signal is provided by a signal generator with an output impedance of 50 Ω. This is terminated with a 49.9 Ω resistor near $+D_{IN}$ of the AD813x. The effective parallel resistance of the source and termination is 25 Ω. The 24.9 Ω resistor from $-D_{IN}$ to ground matches the $+D_{IN}$ source impedance and minimizes any dc and gain errors.

If $+D_{IN}$ is driven by a low-impedance source over a short distance, such as the output of an op amp, no termination resistor is required at $+D_{IN}$. In this case, the $-D_{IN}$ can be directly tied to ground.

TRANSMIT EQUALIZER
Any length of transmission line will attenuate the signals it carries. This effect is worse at higher frequencies than at low frequencies. One way to compensate for this is to provide an equalizer circuit that boosts the higher frequencies in the transmitter circuit, so that at the receive end of the cable the attenuation effects are diminished.

By lowering the impedance of the RG component of the feedback network at higher frequency, the gain can be increased at high frequency. Figure 7 shows a gain of a two line driver that has its RGs shunted by 10 pF resistors. The effect of this is shown in the frequency response plot of Figure 8.
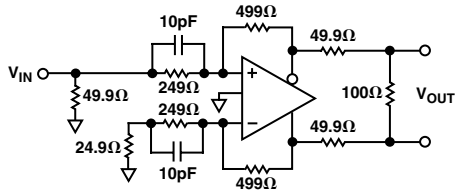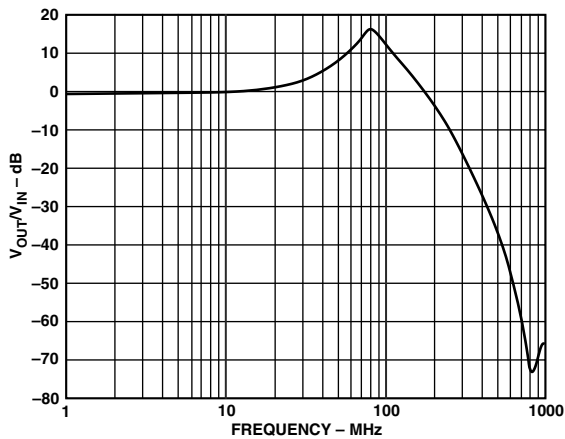

Figure 7. Frequency Boost Circuit

Figure 8. Frequency Response for Transmit Boost Circuit

MISCELLANEOUS APPLICATIONS
Balanced Transformer Driver

Transformers are among the oldest devices that have been used to perform a single-ended-to-differential conversion (and vice versa). Transformers also can perform the additional functions of galvanic isolation, step-up or step-down of voltages, and impedance transformation. For these reasons, transformers will always find uses in certain applications.

However, when driving a transformer single-endedly and then looking at its output, there is a fundamental imbalance due to the parasitics inherent in the transformer. The primary (or driven) side of the transformer has one side at dc potential (usually ground), while the other side is driven. This can cause problems in systems that require good balance of the transformer's differential output signals.

If the interwinding capacitance (C_{STRAY}) is assumed to be uniformly distributed, a signal from the driving source will couple to the secondary output terminal that is closest to the primary's driven side. On the other hand, no signal will be coupled to the opposite terminal of the secondary, because its nearest primary terminal is not driven (see Figure 9). The exact amount of this imbalance will depend on the particular parasitics of the transformer, but will mostly be a problem at higher frequencies.
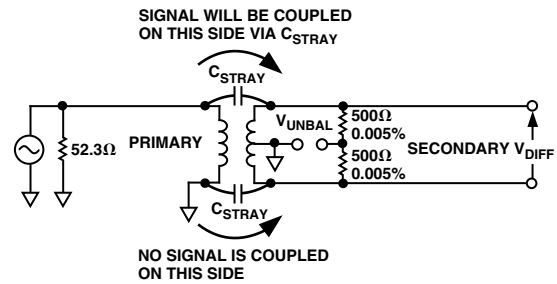

Figure 9. Transformer Single-Ended-to-Differential Converter Is Inherently Imbalanced

The balance of a differential circuit can be measured by connecting an equal-valued resistive voltage divider across the differential outputs and then measuring the center point of the circuit with respect ground. Since the two differential outputs are supposed to be of equal amplitude, but 180 degrees opposite phase, there should be no signal present for perfectly balanced outputs.

The circuit in Figure 9 shows a Minicircuits T1-6T transformer connected with its primary driven single-endedly and the secondary connected with a precision voltage divider across its terminals. The voltage divider is made up of two 500 Ω, 0.005% precision resistors. The voltage V_{UNBAL}, which is also equal to the ac common-mode voltage, is a measure of how closely the outputs are balanced.

The plots in Figure 10 show a comparison between the case where the transformer is driven single-endedly by a signal generator and driven differentially using an AD813x. The top signal trace of Figure 10 shows the balance of the single-ended configuration, while the bottom shows the differentially driven balance response. The 100 MHz balance is 35 dB better when using the AD813x.
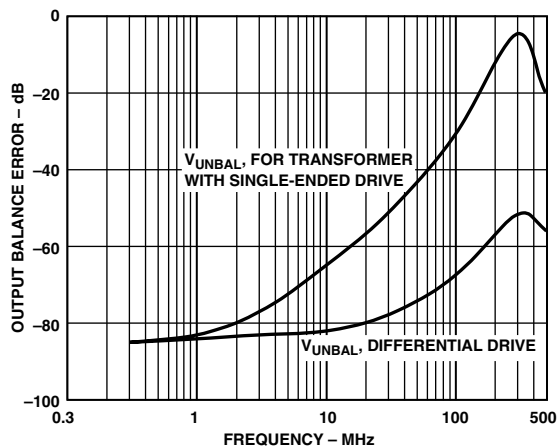
Figure 10. Output Balance Error for Circuits of Figure 9 and Figure 11

The well-balanced outputs of the AD813x will provide a drive signal to each of the transformer's primary inputs that are of equal amplitude and 180 degrees out of phase. Thus, depending on how the polarity of the secondary is connected, the signals that conduct across the interwinding capacitance will either both assist the transformer's secondary signal equally, or both buck the secondary signals. In either case, the parasitic effect will be symmetrical and provide a well-balanced transformer output. (See Figure 11.)
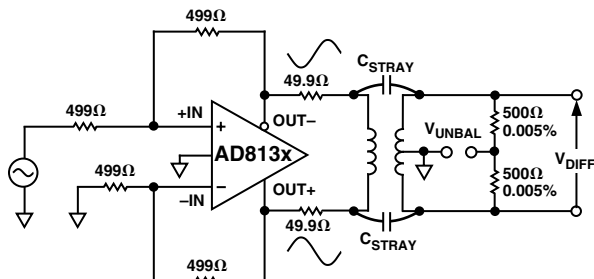

Figure 11. AD813x Forms a Balanced Transformer Driver

Full-Wave Rectifier

The balanced outputs of the AD813x, along with a couple of Schottky diodes, can create a very high-speed full-wave rectifier. Such circuits are useful for measuring ac voltages and other computational tasks.

Figure 12 shows the configuration of such a circuit. Each of the AD813x outputs drives the anode of an HP2835 Schottky diode. These Schottky diodes were chosen for their high-speed operation. At lower frequencies (approximately lower than 10 MHz), a silicon signal diode such as

a 1N4148 can be used. The cathodes of the two diodes are connected together and this output node is connected to ground by a 100 Ω resistor.
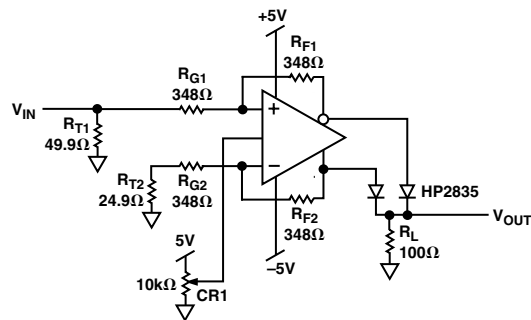

Figure 12. Full-Wave Rectifier

The diodes should be operated such that they are slightly forward-biased when the differential output voltage is zero. For the Schottky diodes, this is about 400 mV. The forward biasing can be conveniently adjusted by CR1, which, in this circuit, raises and lowers $V_{OUT,cm}$ without creating a differential output voltage.

One advantage of this circuit is that the feedback loop is never momentarily opened while the diodes reverse their polarity within the loop. This is the scheme that is sometimes used for full-wave rectifiers that use conventional op amps. These conventional circuits do not work well at frequencies above about 1 MHz.

If there is not enough forward bias ($V_{OUT,cm}$ too low), the lower sharp cusps of the full-wave rectified output waveform will be rounded off. Also, as the frequency increases, there tends to be some rounding of the lower cusps. The forward bias can be increased to yield sharper cusps at higher frequencies.

There is not a reliable, entirely quantifiable, means to measure the performance of a full-wave rectifier. Since the ideal waveform has periodic sharp discontinuities, it should have (primarily even) harmonics that have no upper bound on the frequency. However, for a practical circuit, as the frequency increases, the higher harmonics become attenuated and the sharp cusps that are present at low frequencies become significantly rounded.

The circuit was run at a frequency up to 300 MHz and, while it was still functional, the major harmonic that remained in the output was the second. This made it look like a sine wave at 600 MHz. Figure 13 is an oscilloscope plot of the output when driven by a 100 MHz, 2.5 V p-p input.

Sometimes a second harmonic generator is actually useful, such as creating a clock to oversample a DAC by a factor of two. If the output of this circuit is run through a low-pass filter, it can be used as a second harmonic generator.
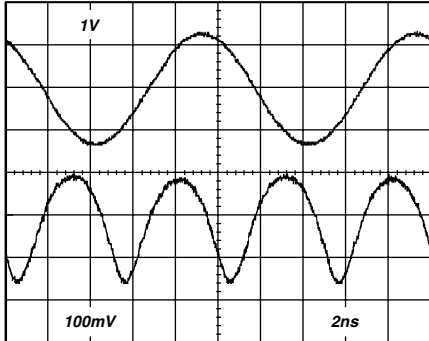

Figure 13. Full-Wave Rectifier Response with 100 MHz Input

Differential Filtering Applications
Similar to an op amp, various types of active filters can be created with the AD813x. These can have single-ended inputs and differential outputs, which can provide an antialias function when driving a differential A/D converter.

Figure 14 is a schematic of a low-pass, multiple feedback filter. The active section contains two poles, and an additional pole is added at the output. The filter was designed to have a –3 dB frequency of 1 MHz. The actual –3 dB frequency was measured to be 1.12 MHz as shown in Figure 15.
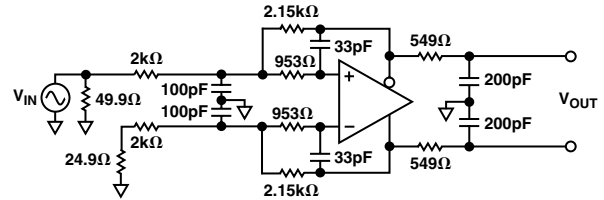

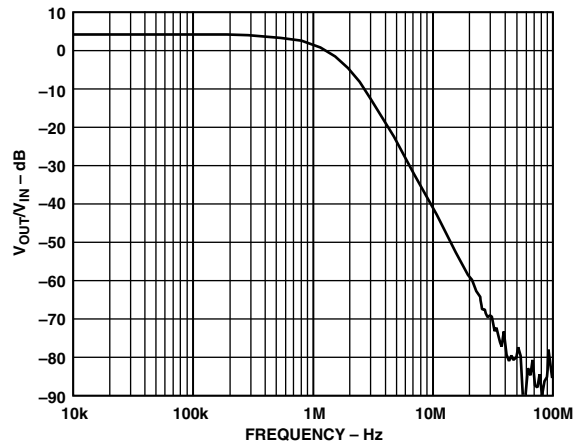*Figure 14. 1 MHz, 3-Pole Differential Output Low-Pass Multiple Feedback Filter*

Figure 15. Frequency Response of 1 MHz Low-Pass Filter