Single Chip Realizes
Direct-Conversion Rx

Direct-conversion Rxs offer advantages in simplicity compared to conventional superheterodyne approaches, although attention must be paid to some of the trade-offs.

direct conversion of RF signals to baseband has long been a goal of communications systems designers. The approach can eliminate expensive and bulky hardware, but at the cost of some trade-offs in performance. What follows is an examination of the trade-offs associated with designing a direct-conversion receiver (Rx) compared to a traditional superheterodyne architecture, as well as details on a new direct-conversion Rx integrated-circuit (IC) subsystem.

The function of a conventional superheterodyne Rx **(Fig. 1, left)** and a direct-conversion Rx **(Fig. 1, right)** is the same: translating and conditioning signals downward in frequency so that they can be sampled by low-frequency (baseband) analog-to-digital converters (ADCs). As is apparent from a comparison of the two block diagrams, the direct-conversion system achieves this function with considerably fewer components.

In a conventional single- or double-conversion superheterodyne Rx, the modulated RF signal is translated in frequency through one or more intermediate frequencies (IFs) before being converted back to its desired baseband format. At IF, the signal is filtered and amplified before being mixed to a lower frequency. In a direct-conversion Rx, the modulated RF signal is mixed with a local oscillator (LO) at exactly the same frequency.

The obvious reduction of compo-

nent count, along with the elimination of expensive filtering has made direct conversion very appealing as an architecture for transmit and receive functions. However, it is only recently that components which facilitate its practical implementation have become available.

Although the direct-conversion approach reduces the component count, it also adds design challenges. In the superheterodyne approach (Fig. 1, left), by driving the mixer with a frequency-agile LO, the frequency of the desired signal or channel (which is generally varies in a multi-user system) is converted to a fixed frequency. Once the desired signal has been converted to a fixed IF, it can be processed by highly selective narrowband filtering using a surface-acoustic-wave (SAW) filter. In addition, all subsequent frequency translations can be effected using fixed-frequency LOs.

The other important function performed at IF in a superheterodyne system is signal amplification. Fixed-gain amplification, in the form of low-noise amplifiers (LNAs), is generally applied at RF, while signal leveling is general-

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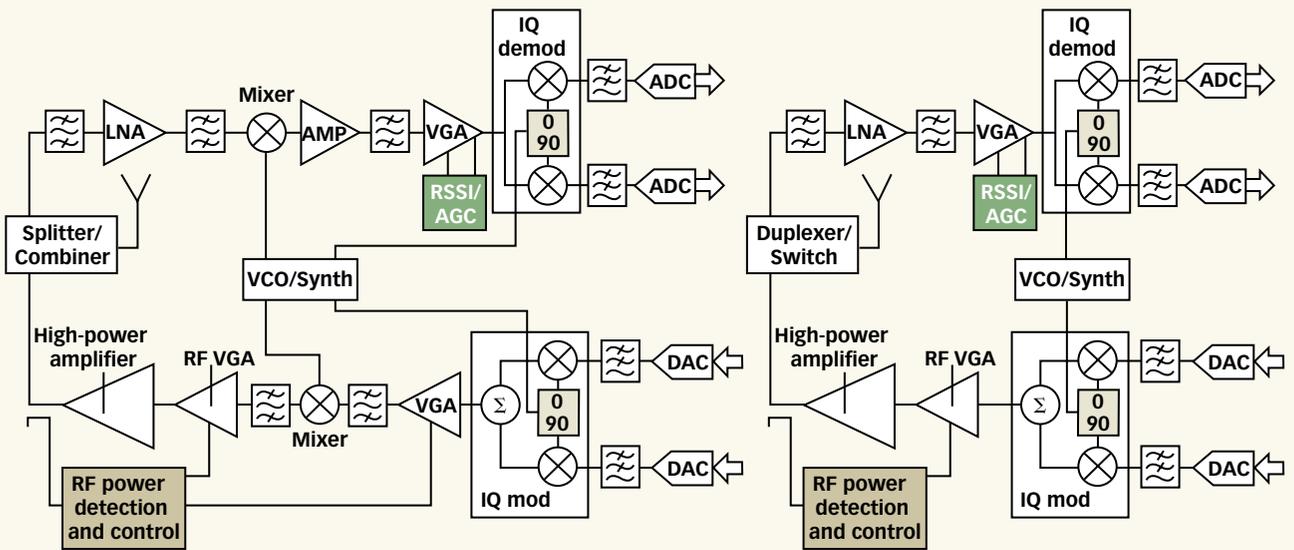
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1. A conventional single-conversion superheterodyne Rx translates the frequency of desired signals through one or more IFs before converting it to baseband. A direct-conversion Rx makes the transition directly from RF to baseband.

ly accomplished through the use of variable-gain amplifiers (VGAs). Since it is easier to design a high-gain-range VGA at lower frequencies, and because many unwanted signal components have already been removed from the carrier by the time it is translated to IF, variable-gain amplification is generally performed at IF or baseband frequencies. This "distribution" of gain avoids a concentration of high gain at the Rx's front-end portion, which can cause saturation of subsequent stages, especially if large in-band or out-of-band signal blockers are present.

While the appeal of a direct-conversion Rx lies in its elimination of IF stages, therein lies its weakness. Because there is no longer an IF stage at which signal leveling and filtering can be conveniently performed, all signal conditioning must be performed either at RF or baseband. In a multichannel system, the capabilities of RF filters are limited (they cannot be narrowband), at best screening out-of-band interferers. SAW filters are available for some RF uses (through approx-

imately 3 GHz), but they are generally more expensive than lower-frequency IF filters due to the higher quality-factor (Q) requirements.

A cost-effective means of realizing a direct-conversion Rx is through monolithic fabrication, by including as many of the required components on a single chip, such as the AD8347 direct-conversion Rx IC **(Fig. 2)** from Analog

Devices (Norwood, MA). This Rx IC can demodulate signals from 0.8 to 2.7 GHz. The device consists of a number of subcircuits that can be configured separately. The IC includes all of the components required for amplification, downconversion, and filtering in a direct-conversion demodulation circuit.

Since gain control in a direct-conversion design must be implemented at
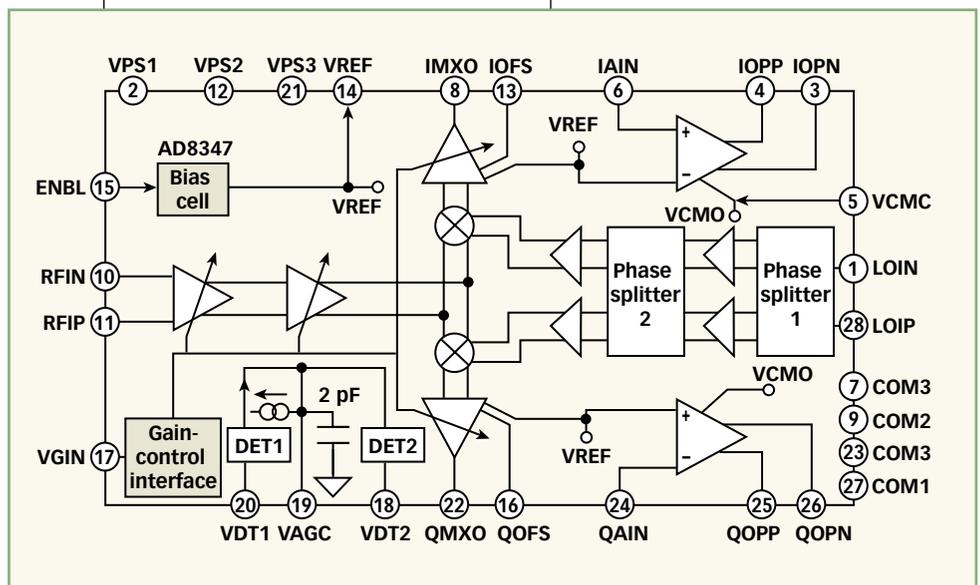

2. The AD8347 is comprised of a 70-dB VGA with AGC mode, an I/Q demodulator and two 30-dB-gain baseband amplifiers. An internal +1-VDC voltage reference provides biasing.

RF and/or at baseband, the AD8347 employs three stages of VGA. Two stages are employed at RF and one at baseband, following the I/Q demodulator. The three VGA stages, which have a convenient linear-in-dB gain-control relationship, are controlled in parallel. Each of the two RF VGAs has a gain range from –10 to +13 dB. The combined gain range of the mixer and the baseband VGA is –10 to +14 dBm. The overall gain range from the RF input to the mixer output is therefore –30 to +40 dB.

The gain of the VGA is set by the voltage on the AD8347's VGIN pin, which is a high-impedance input port. **Figure 3** shows a plot of the gain versus gain-control voltage, along with the linearity of the gain-control function. Note that the sense of the gain-control voltage is negative. As the gain-control voltage increases from +0.2 to +1.2 VDC, the gain decreases from +40 to –30 dB.

The VGA can be driven by an exter-
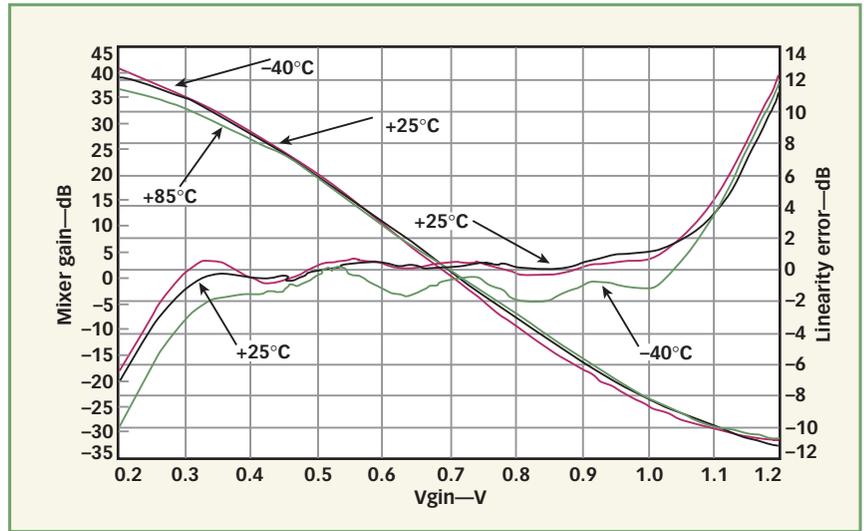
3. **The three-stage VGA (two stages at RF, one stage at baseband) varies gain from –30 to +40 dB. The gain-control function is linear-in-dB over its range**.

nal voltage source [generally a digital-to-analog converter (DAC)] or by an automatic-gain-control (AGC) circuit built into the device. The AGC circuit con-

sists of two root-mean-square (RMS) detectors and an error amplifier. When the AGC circuit is being used, the two mixer outputs are connected to the
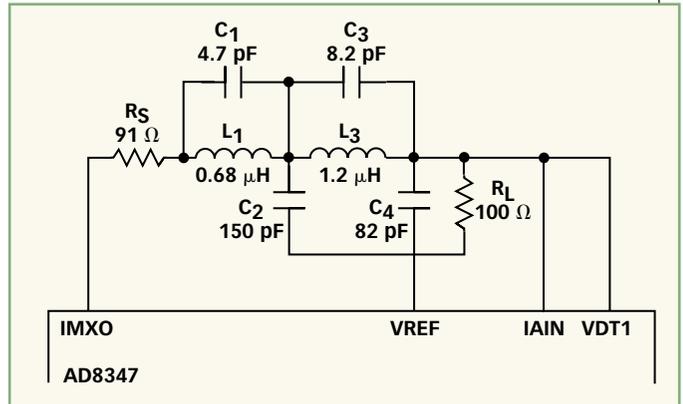
4. The demodulated output (baseband-mixer output) can be filtered off-chip before being applied to the final baseband amplifiers. The on-chip reference voltage signal (VREF) provides biasing for the filter circuit.

inputs of the two detectors. The signals (currents) from the detectors are compared with a set-point signal and an error signal is generated. The AGC circuit is completed by connecting the error signal to the Rx's VGIN gain-control input pin. With the AGC circuit activated, the mixer's output will remain constant for input levels from −55 to + 5 dBm. Because this output has a 90-MHz bandwidth, downconversion to a low IF is also possible.

The mixer is a quadrature demodulator between the RF and baseband VGAs. It produces in-phase (I) and quadrature (Q) baseband outputs. To achieve low error-vector magnitude (EVM) in (direct-conversion) digital demodulation, precise quadrature splitting and amplitude balance of the LO signal is required. The AD8347 achieves typical phase and amplitude balances of 3 deg. and 0.3 dB, respectively, from 0.8 to 2.7 GHz.

LO leakage within a direct-conversion system is one of the key challenges to implementing a high-sensitivity direct-conversion Rx. In direct-conversion and superheterodyne Rxs, some of the LO signal will leak through to the RF input. LO leakage to the RF input will cause self-mixing, which will produce a troublesome DC component at the mixer output. This DC component, if large enough, can lead to saturation of the baseband output signal (to either rail). In addition, because LO leakage is typically frequency dependent, the extent of the DC offset will also vary with frequency, making simple offset compensation difficult.

In a conventional Rx, even if the first downconversion produces a DC component, this component will be harmless as it will be removed by IF filtering. This is an argument for using a direct-conversion Rx to mix the signal down to a low IF (instead of all the way to baseband) and digitizing those signals using IF sampling. The 90-MHz bandwidth of the AD8347's mixer output easily facilitates this.

The AD8347 uses two techniques to minimize the effects of LO leakage. First, the use of an active mixer means that the LO level can be set quite low. In the case of the AD8347,

the recommended level is –8 dBm.

The device also contains a circuit that actively reduces DC offsets that appear at the output of the baseband VGA. Internally, the average level on the baseband outputs is compared to their nominal bias levels of +1 VDC. If there is any discrepancy between these two voltages, the average level at the mixer output is slowly servo-controlled back to +1 VDC. The settling time to this level-correcting circuit can be controlled through external capacitors.

Because the output of the mixer/VGA circuit and the input to the final baseband amplifiers are separately pinned out, baseband lowpass or bandpass filtering can be conveniently performed before the signal faces its final amplification stage. The mixer/VGA output and the baseband amplifier inputs are biased to the same reference voltage level (of +1 VDC at VREF), making a DC-coupled connection permissible.

Figure 4 shows a schematic diagram for a 100-Ω, fourth-order elliptic lowpass filter with a 3-dB cutoff of 20 MHz. Source and load impedances of approximately 100 Ω ensure that the filter experiences a matched source and load. This also ensures that the mixer output is driving an overall load of 200 Ω. Note that the shunt-termination resistor is tied to the reference voltage VREF and not to ground.

The AD8347's baseband amplifiers take single-ended input signals and boost them by 30 dB to produce a differential output which can be independently biased. The VOCM input pin, which sets the output common-mode level, can be driven by the AD8347's internal +1-VDC reference. Alternatively, the VOCM pin can be driven by an external reference voltage. In general, when the VOCM pin is driven externally, the drive voltage should come from the ADC that the AD8347 is driving. The differential outputs are capable of swinging from +0.4 VDC above ground to within +1.3 VDC of the supply voltage and have a 3-dB bandwidth of 65 MHz.

Figure 5 shows a block diagram of a complete Rx signal chain that can be used to demodulate various signal types,
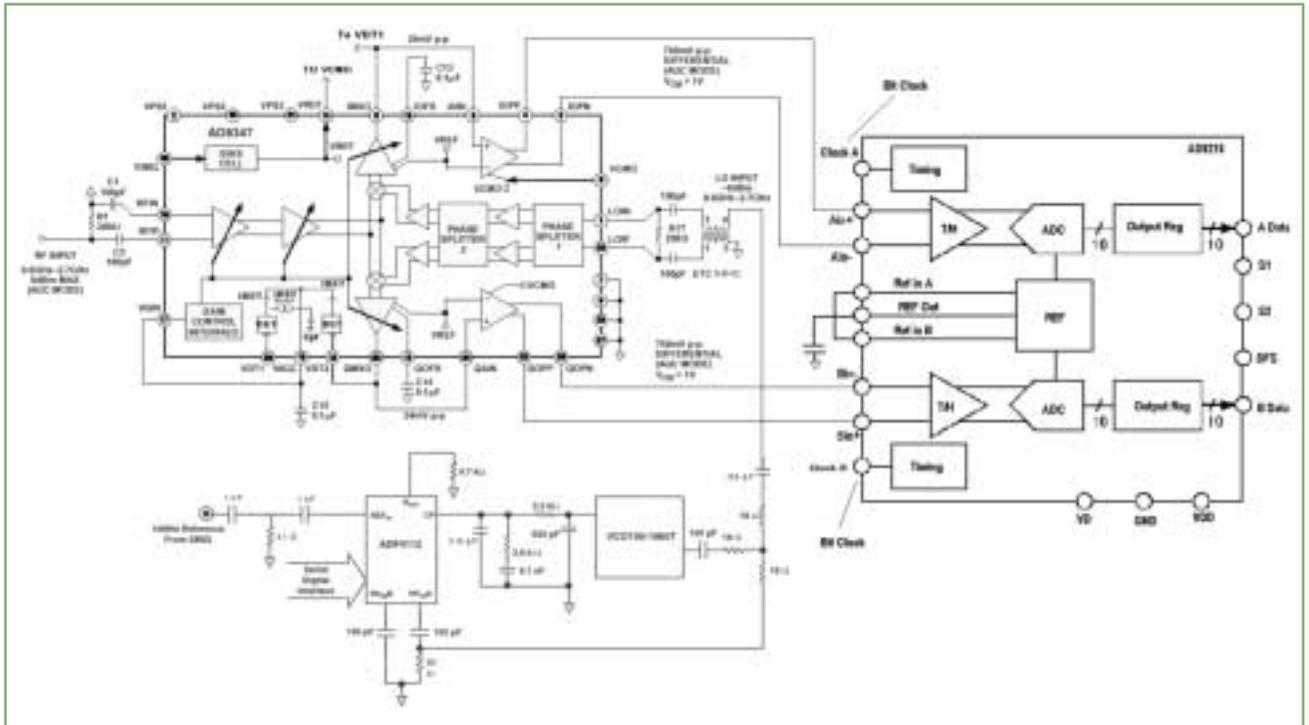
5. A complete direct-conversion Rx can be assembled using the ADF4112, AD8347, and AD9218 ICs.

including higher-order quadrature-amplitude-modulation (QAM) signals. The evaluation system includes the ADF4112 phase-locked loop (PLL), with a range of 0.2 to 3 GHz, which easily covers the 0.8-to-2.7-GHz LO range of the AD8347. In this evaluation system, a 1.9-GHz voltage-controlled oscillator (VCO) was used with the PLL, and a 1:1 balun was inserted between the PLL and the AD8347's LO input to provide a differential drive.

The I/Q outputs of the AD8347, biased to the AD8347's internal reference voltage, connect directly to the differential inputs of the AD9218 dual ADC. The AD9218 is a dual 10-b device available for sampling rates of 40, 65, 80, and 105 MSamples/s (the 105-MSamples/s version was used in this measurement setup). For lower-order modulation schemes, it is possible to use the AD9288, a dual 8-b ADC with versions avail-
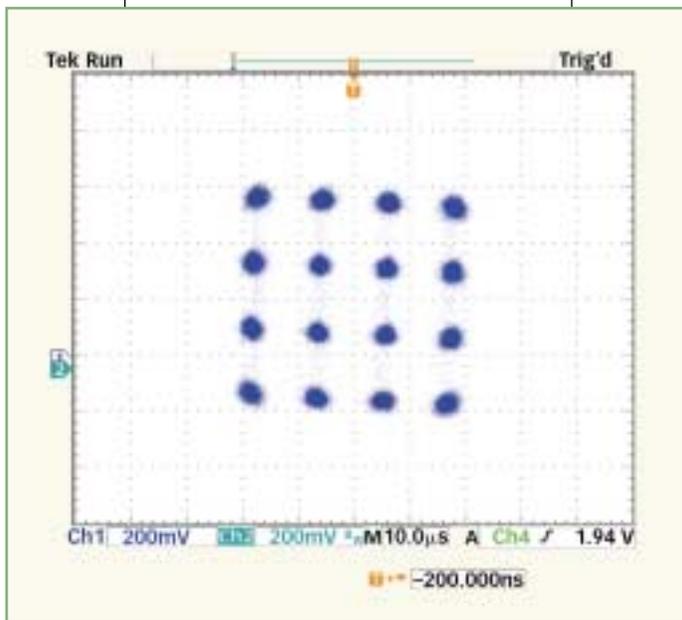
able for rates of 40, 60, 80, and 100 MSamples/s.

The high-encode-rate capability and high analog bandwidth of the AD8347 also make possible IF sampling applications. By running a 1.9-GHz LO with RF signals at 1.93 GHz, a (modulated)

6. Using a reconstruction DAC, the (digitized) demodulated constellation for a 2-MSymbol/s, 16-QAM signal can be displayed on a standard oscilloscope screen.

30-MHz frequency offset results. This 30-MHz offset (and including the frequency deviations of the modulation) is well-within the 65-MHz bandwidth of the AD8347's output amplifiers, as well as the analog bandwidth of the AD9218 ADC. The AD9218 successfully mixed down these 30-MHz offset signals to baseband frequencies, showing the AD8347/AD9218 combination to be suitable for some IF sampling applications. To evaluate the AD8347 as a direct-conversion Rx operating with complex modulation, RF input signals to the AD8347 were supplied from an SMIQ-series vector-signal generator from Rohde & Schwarz (Munich, Germany). The instrument is capable of providing clean 1.9-GHz RF signals with a variety of modulation formats, including 16QAM and 64QAM.

The AD8347 and ADF4112 can operate at

supply voltages from +3 to +5 VDC. For the evaluation setup, a +3-VDC supply was used, matching the power-supply level of the AD9218. Baseband filtering prior to final output amplification (to improve performance through the elimination of out-of-band noise) is possible on the AD8347 evaluation board, but was not done during this evaluation. The AD8347's VGA was set to run in AGC mode. In this mode, the mixer output settles to a level of approximately 24 mV peak to peak, resulting in a 760-mV peak-to-peak differential voltage at the baseband amplifier outputs. In addition to baseband lowpass filtering, the signal-to-noise ratio (SNR) of the demodulated signal can be

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improved by increasing the mixer output levels beyond this nominal 24-mV peak-to-peak level.[1]

The standard ADF4112 PLL printed-circuit board (PCB) is shipped with an 800-MHz external VCO. For this evaluation of the AD8347, the PLL module's 800-MHz VCO was replaced with a 1.9-GHz VCO. Tuning of the AD4112's output frequency was easily accomplished through the parallel port using a software package supplied with the PLL by Analog Devices. The PLL module's PCB also features an onboard 10-MHz crystal-oscillator reference source, which was bypassed to allow for synchronization with external RF source (the SMIQ-series vector-signal generator).

Before measurements could be made, the evaluation board for the AD9218 ADC required some modifications to enable common clocking and to meet

the limited drive capability of the clock source. The bit clock from the SMIQ-series vector-signal generator supplied the required encode clock for the AD9218. For a 2-Msymbol/s data rate, this corresponded to an 8-MHz clock rate for 16QAM. The analog input 50-Ω termination resistors on the PCB were switched to 1-kΩ terminations to accommodate the limited drive capability of the AD8347's baseband output amplifiers. This resulted in approximately 400-mV signal swings to the ADC (which has a full-scale input range of 500 mV). To minimize transmission-line effects, this meant keeping cabling between boards as short as possible. The evaluation setup supported the display of 16QAM and 64QAM constellations by reconstructing the ADC outputs using an AD9763 DAC and displaying the I and Q outputs on an oscilloscope in X-Y mode **(Fig. 6)**.

With an input range from 0.8 to 2.7 GHz, the AD8347 is suitable for a broad range of markets. Applications include point-to-point and point-to-multipoint radios, built-in-test-equipment (BITE) systems in cellular base stations, and auxiliary Rx systems in linear high-power amplifiers (HPAs). For systems operating beyond 2.7 GHz, it can also be used as an IF-to-baseband converter. **MRF**

REFERENCES

1. AD8347 0.8-2.7 GHz Direct Conversion Modulator, Analog Devices, Norwood, MA, 2001, pp 15-16.