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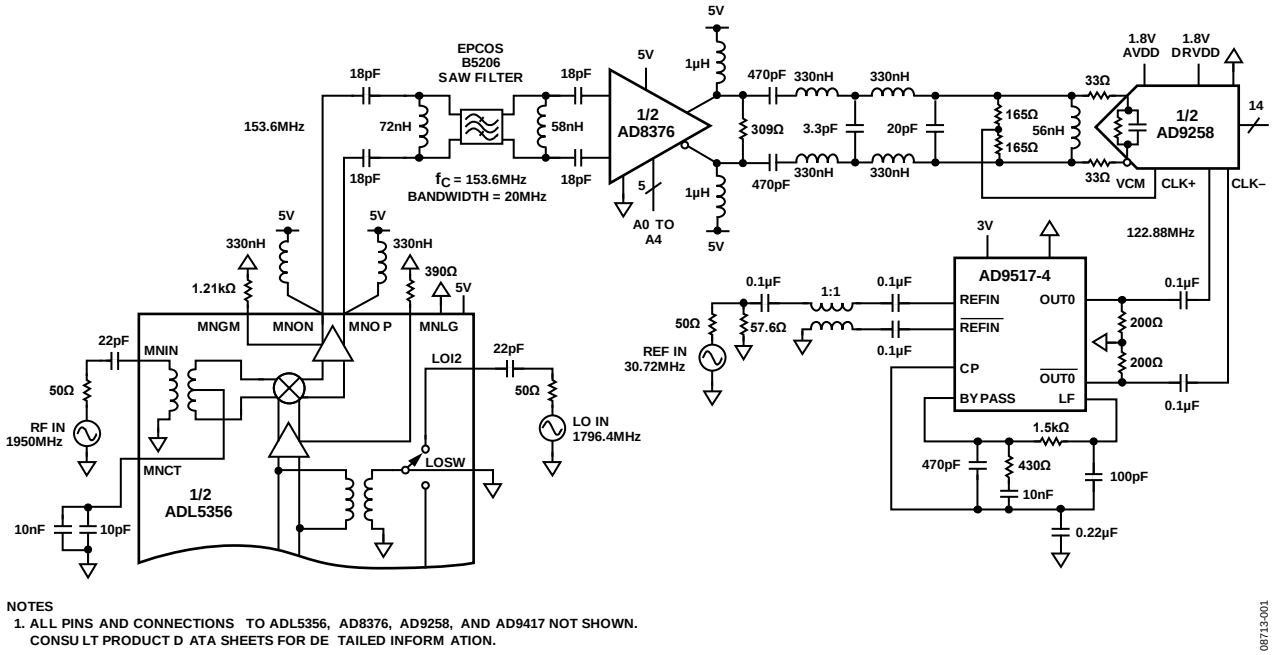
High Performance, Dual-Channel IF Sampling Receiver

CIRCUIT FUNCTION AND BENEFITS

This circuit is a high performance, dual-channel intermediate frequency (IF) sampling receiver that is also called a main receiver or diversity receiver in base station terminology. The downconverting receiver uses a single IF frequency of 153.6 MHz and includes a dual downconverting mixer, a digitally controlled dual variable gain amplifier (VGA), a dual analog-to-digital converter (ADC), and a clock synthesizer. The circuit takes an incoming radio frequency (RF) waveform and outputs a dual 14-bit resolution digital data stream. The circuit is optimized for high frequency IF sampling and provides spurious-free dynamic range (SFDR) performance of 79.61 dBc with a sampling rate of 122.88 MSPS at the high gain setting.

Figure 1 shows a simplified schematic of the circuit in which one half of the receiver is shown and not all connections and coupling are shown.



NOTES
1. ALL PINS AND CONNECTIONS TO ADL5356, AD8376, AD9258, AND AD9417 NOT SHOWN. CONSULT PRODUCT DATA SHEETS FOR DETAILED INFORMATION.

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Figure 1. Broadband, Dual-Channel IF Sampling Receiver Simplified Schematic

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REVISION HISTORY

10/2018—Rev. 0 to Rev. A

Document Title Changed from CN-0140 to AN-1589 ..... Universal
Changes to Circuit Function and Benefits Section 1
Changes to Circuit Description Section and Table 1 3
Changes to Common Variations Section 4
Deleted Data Sheets and Evaluation Board Section 4
Changed Learn More Section to References Section 5

1/2010—Revision 0: Initial Version

CIRCUIT DESCRIPTION

This circuit includes the RF front end, as well as the IF sampling receiver. The circuit is composed of a dual-balanced mixer, a broadband IF surface acoustic wave (SAW) filter, a digitally controlled dual VGA, and a dual ADC. The circuit also includes a synthesizer that generates the ADC sampling clock.

The ADL5356 dual-balanced mixer can downconvert RFs, primarily between 1200 MHz and 2500 MHz, to IFs between 30 MHz and 450 MHz.

The RF and local oscillator (LO) input ports are ac-coupled to prevent nonzero dc voltages from damaging the RF balun or LO input circuits, which are part of the ADL5356. The ADL5356 is configured for single-ended LO operation with a recommended LO drive of 0 dBm. When the LOSW pin of the mixer is grounded, only one of the two LO channels (LOI2) is used in this circuit.

The mixer differential IF interface requires pull-up choke inductors to bias the open-collector outputs and to set the output impedance match. Select the shunting impedance of the choke inductors used to couple dc current into the IF amplifier to provide the desired output return loss. The real part of the mixer output impedance is approximately 200 Ω, which matches many commonly used SAW filters without the need for a transformer.

The receiver channel filtering is mainly performed by a 153.6 MHz, 20 MHz bandwidth EPCOS B5206 SAW filter that follows the mixer. The typical insertion loss of this filter is approximately 9 dB. The natural matched impedance of this SAW filter is 100 Ω differential. A simple inductor capacitor network (LC reactive network) matches the SAW filter to the mixer 200 Ω differential output and the AD8376 VGA 150 Ω differential input impedance.

Table 1 details the cascaded performance of the dual mixer plus the SAW filter.

A receiver gain control of 24 dB is provided by the AD8376 dual, high output linearity VGA that is optimized for ADC interfacing. Two independent 5-bit binary codes change each attenuator setting in 1 dB steps such that the gain of each amplifier can be set from +20 dB to −4 dB. The output third-order intercept point (IP3) and noise floor essentially remain constant across the 24 dB available gain range. This consistency is a valuable feature in a variable gain receiver where it is desirable to maintain a constant instantaneous dynamic range as the receiver gain is modified. The output IP3 of the AD8376 and the subsequent antialiasing filter is in excess of 50 dBm with a 2 V p-p composite signal.

The AD8376 provides a 150 Ω input impedance and is tuned to drive a 150 Ω load impedance. The open-collector output structure requires dc bias through an external bias network. A set of 1 µH choke inductors are used on each channel output to provide bias to the open-collector output pins. An optimized differential fourth-order, band-pass antialiasing filter is implemented at the VGA outputs before analog-to-digital conversion. The antialiasing filter is terminated with shunt input and output resistances of approximately 300 Ω. The shunt resistances at either end of the filter of 309 Ω at the input and 330 Ω (through two 165 Ω bias setting resistors) at the output combine to provide the AD8376 with a nominal 150 Ω load impedance.

The band-pass antialiasing attenuates the output noise of the AD8376 outside of the intended Nyquist zone. In general, the signal-to-noise ratio (SNR) improves several dB by including a reasonable order antialiasing filter. The antialiasing filter is comprised of a fourth-order Butterworth filter with a resonant tank circuit. The resonant tank helps ensure that the ADC input looks like a real resistance at the target center frequency by resonating out the capacitive portion of the ADC load (see the AN-742 Application Note and AN-827 Application Note). In addition, the ac-coupling capacitors and the bias chokes introduce additional zeros into the transfer function. The overall frequency response takes on a band-pass characteristic, helping to reject noise outside of the intended Nyquist zone. The filter provides a 20 MHz pass band centered at 153.6 MHz with 0.3 dB flatness and an insertion loss of approximately 3 dB.

Table 1. Cascaded Performance of the Dual Mixer Plus SAW Filter[1]

Part Number	Gain (dB)	IP3 (dBm)	Input Referred −1 dB Compression Point, IP1dB (dBm)	Noise Figure, NF (dB)
ADL5356	8.2	30.0	11.5	9.7
ADL5356 + SAW	−0.3	28.6	11.7	10.9

[1] RF = 1950 MHz, LO = 1796.4 MHz, IF = 153.6 MHz, RF power = −10 dBm, and LO power = 0 dBm.

The ADC utilized is the 14-bit AD9258, which samples at rates up to 125 MSPS. The analog inputs of the AD9258 are driven by the AD8376 through the band-pass antialiasing filter. The ADC sampling rate is set to 122.88 MSPS with a full-scale input range of 2 V p-p. The AD9258 differential clock signal is provided by the AD9517-4, a clock generation IC with an on-chip voltage controlled oscillator (VCO). The low voltage positive emitter-coupled logic (LVPECL) level output, OUT0, is used for low jitter. The AD9517-4 uses its internal VCO frequency of 1474.56 MHz to derive the 122.88 MHz output clock to the ADC. A loop filter designed with the ADIsimCLK™ simulation software provides a 60 kHz cutoff frequency and 50° of phase margin, giving a timing jitter of approximately 160 fs rms. This jitter corresponds to a theoretical SNR of 76 dB, assuming a 153.6 MHz input, using the following formula:

$$SNR = 20\log(1/2\pi \times f_{IN} \times t_J)$$

where:
f_{IN} is input frequency.
t_J is timing jitter.

Using this circuit, SFDR performance of 79.61 dBc at 153.6 MHz is achieved at maximum gain, as shown in Figure 2.

COMMON VARIATIONS

Front-end low noise amplifiers (LNAs) and attenuators are not included in this circuit but can easily interface with the 50 Ω single-ended RF inputs of the ADL5356 mixer. For a complete receiver design, ADL5521/ADL5523 LNAs may be incorporated.

The standard configuration using the ADL5356 allows reception of RF signals from 1.2 GHz to 2.4 GHz, but it is also possible to use the ADL5358 mixer, which covers RF input frequencies from 500 MHz to 1700 MHz.

An EPCOS SAW filter follows the mixer and provides the necessary channel selectivity over a bandwidth ranging from 20 MHz to 40 MHz, depending on the chosen filter. The circuit shown in Figure 1 uses a 20 MHz bandwidth and 153.6 MHz centered SAW filter (the EPCOS B5206) but can also accommodate other pin-compatible filters.

Some empirical optimization may be necessary to help compensate for actual printed circuit board (PCB) parasitics in SAW filter matching and antialias filter implementation. Details of designing the interstage filters can be found in the AN-742 Application Note and AN-827 Application Note.

To ensure repeatability of band response, 1% capacitors are recommended for the SAW filter matching components and the antialiasing filter. In addition, Coilcraft 0603CS or similar inductors are recommended. Other resistors, capacitors, and inductors can be 10% values.

Utilize proper layout, grounding, and decoupling techniques to achieve the desired performance from the circuits discussed in this application note. As a minimum, use a 4-layer PCB with one ground plane layer, one power plane layer, and two signal layers.

Decouple all IC power pins to the ground plane with low inductance multilayer ceramic capacitors (MLCC) of 0.01 µF to 0.1 µF. Follow the recommendations on the individual data sheets and in Tutorial MT-101. Consult relevant product evaluation board documentation for recommended layout and critical component placement.

Although the AD8376 and AD9258 (or other ADCs) can be powered from different supplies, sequencing is not a problem because the input signal to the ADC is ac-coupled.

Consult the individual data sheet for the ADC regarding the proper sequencing of the AVDD and the DVDD power supplies (if separate supplies are used).

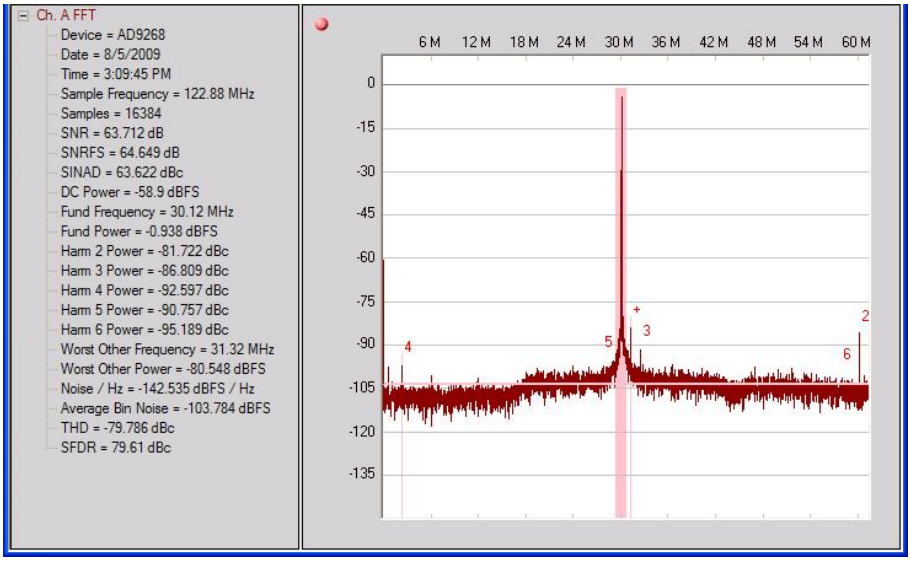

Figure 2. Measured Single-Tone Performance of the Circuit for a 1950 MHz RF Input Signal, Sampling Frequency = 122.88 MSPS, IF Input = 153.6 MHz

REFERENCES

AN-742 Application Note. *Frequency Domain Response of Switched Capacitor ADCs*. Analog Devices.

AN-827 Application Note. *A Resonant Approach to Interfacing Amplifiers to Switched-Capacitor ADCs*. Analog Devices.

AN-1408 Application Note. *Using the AD8376 VGA to Drive Wide Bandwidth ADCs for High IF AC-Coupled Applications*. Analog Devices.

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MT-073 Tutorial, *High Speed Variable Gain Amplifiers (VGAs)*, Analog Devices.

MT-075 Tutorial, *Differential Drivers for High Speed ADCs Overview*, Analog Devices.

MT-101 Tutorial, *Decoupling Techniques*, Analog Devices.

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