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APPLICATION NOTE

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Compensator Design for a Battery Charge/Discharge Unit Using the AD8450 or the AD8451

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INTRODUCTION

In response to the growing popularity of portable systems, the demand for rechargeable batteries has increased exponentially. The formation and testing of a rechargeable battery requires multiple charge and discharge cycles, during which the current and voltage of the battery must be precisely controlled. Accurately controlling the charge and discharge process extends the life of the battery and maximizes its capacity. Therefore, battery formation and test systems require high precision analog front ends and controllers to monitor and regulate the battery current and terminal voltage.

Rechargeable batteries frequently require a constant current-constant voltage (CC-CV) algorithm to charge or discharge them. This algorithm forces a constant current into or out of the battery until its voltage reaches a preset final value. At this point, the system switches to constant voltage mode and provides the necessary current to hold the battery voltage at this final value.

Most battery formation and test systems implement the CC-CV algorithm using high accuracy feedback loops that control the battery current and voltage. To ensure high battery quality, the feedback loops need to be stable and robust. This application note describes how to design and implement the compensation network for both the constant current and the constant voltage feedback loops in a battery test or formation system using the AD8450 or the AD8451 analog front end and controller.

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REVISION HISTORY

12/14—Revision 0: Initial Version

SYSTEM OVERVIEW

In a battery formation and test system, each charge/discharge unit is comprised of three major components—an analog front end, a controller, and a power converter. These components form the CC and CV feedback loops that control the battery voltage and current during the charge/discharge process.

The analog front end measures the battery voltage and current and forms the feedback path of the CC and CV control loops (see the Modeling section). The controller compares the measured battery voltage and current to the target values and generates the control signal for the power converter using the CC-CV algorithm. The power converter generates the battery current based on the applied control signal.

Figure 1 shows a simplified charge/discharge unit in a battery formation and test system using an AD8450 or an AD8451 analog front end and controller. In this configuration, the power converter extracts power from a common dc voltage bus, which can be shared by multiple charge/discharge units. The shunt resistor (R_S) converts the battery current (I_{BAT}) into a voltage across it (V_{RS}) that is read by the AD8450 or the AD8451. Note that the battery current I_{BAT} is the output current of the power converter. The battery voltage is read directly from the battery terminals. In both measurements, Kelvin connections to the shunt resistor and the battery terminals reduce errors due to voltage drops in the wires. Voltage sources ISET and VSET set the target current and voltage for the CC and CV feedback loops, while the external compensation networks set the frequency response of the controller.

AD8450 AND AD8451 OVERVIEW

The AD8450 and the AD8451 are precision analog front ends and controllers for battery formation and test systems. The analog front end of these devices includes a precision current sense programmable gain instrumentation amplifier (PGIA) to measure the battery current by means of an external shunt resistor (R_S in Figure 1) and a precision voltage sense programmable gain difference amplifier (PGDA) to measure the battery voltage.

The controllers of the AD8450 and the AD8451 include two feedback control loops—a constant current loop (CC) and a constant voltage loop (CV)—which transition automatically from CC to CV after the battery reaches the user defined target voltage. The feedback loops are implemented by means of two precision error amplifiers (A1 and A2 in Figure 1). These serve as error amplifiers and external feedback networks that set the frequency response of the CC and CV feedback loops. External voltage references set the battery target current and target voltage for the CC and CV feedback loops. A minimum output selector circuit combines the outputs of the precision amplifiers and implements the CC-CV algorithm of the controller.

The controllers of the AD8450 and the AD8451 can be operated in either charge or discharge mode. These modes are selected by switching the state of the MODE pin. Charge and discharge modes use independent compensation networks for the CC and CV loops, and the frequency response of these loops is set independently in each mode.

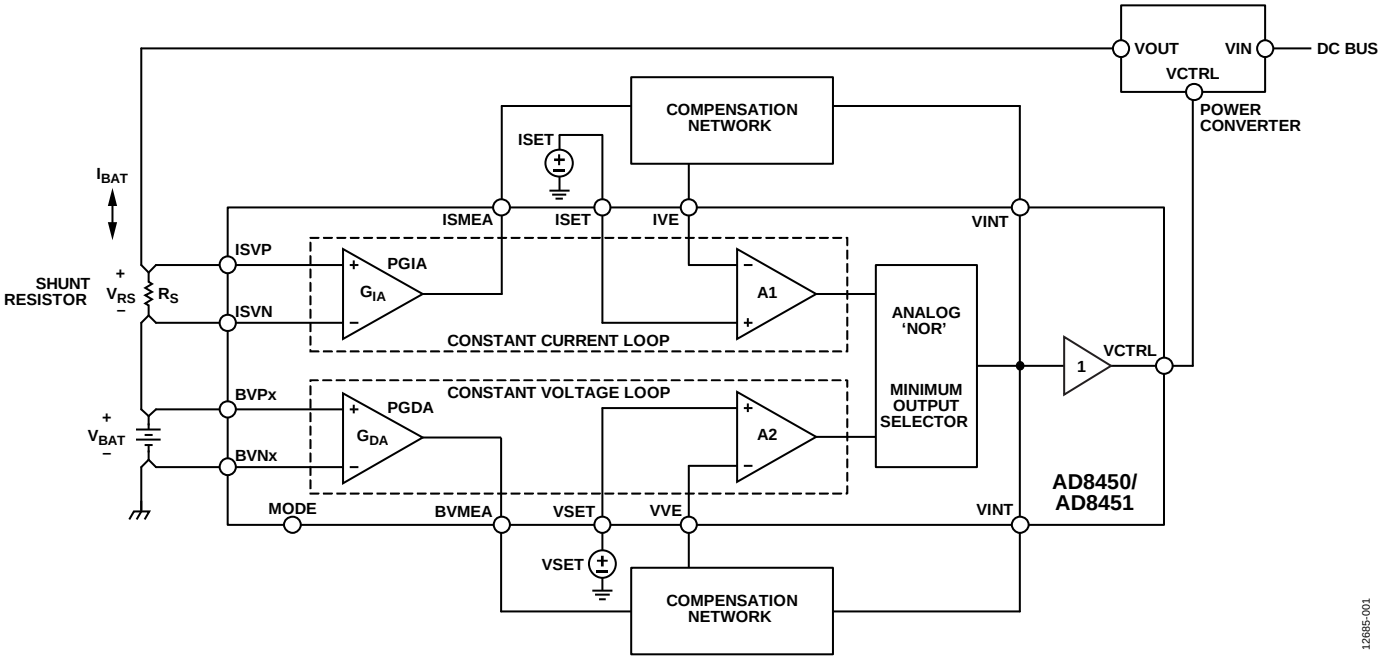

Figure 1. Simplified Charge/Discharge Unit in a Battery Formation and Test System

POWER CONVERTER OVERVIEW

Two types of power converters are commonly used to charge and discharge batteries—linear regulators and switching power converters. Linear regulators are implemented as voltage controlled voltage sources or voltage controlled current sources using a pass transistor. The output current/voltage of these regulators is proportional to their control voltage. While simple to compensate and use, the efficiency of linear regulators tends to be low if the battery voltage and the voltage of the dc bus differ greatly. Figure 2 shows a simple implementation of a charge linear regulator using a voltage controlled current source.

In contrast to linear regulators, switching power converters achieve higher levels of efficiency under most conditions but are more complex and more difficult to stabilize. However, due to their increased efficiency, switching power converters are gaining popularity, especially in high power battery formation and test systems.

Figure 3 shows a simplified nonisolated synchronous buck/boost switching converter. The control signal (V_{CTRL}), which is generated by the controller (AD8450 or AD8451), sets the duty cycle of the MOSFET switches and the average value of the voltage at Node V_M, by means of the pulse width modulator (PWM) of the converter (ADP1972). The inductor (L_O) and capacitor (C_O) form an LC low-pass filter that averages the voltage at Node V_M to generate a low ripple output voltage (V_{OUT}) and output current (I_{BAT}).

The nonisolated buck/boost converter is a bidirectional power converter that enables energy recycling in the system. During charge mode, the converter runs in buck mode, such that it pulls current from the dc bus to charge the battery. In discharge mode, the converter runs in boost mode, such that it pulls current from the battery and feeds it to the dc bus. Therefore, in boost mode, the energy stored in the battery is recaptured.

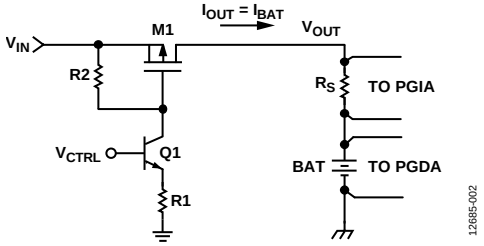

Figure 2. Charge Linear Regulator

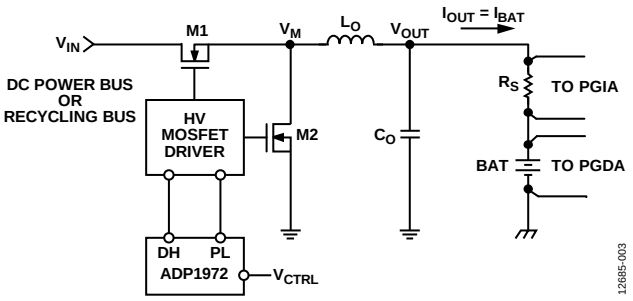

Figure 3. Nonisolated Synchronous Buck/Boost Converter Schematic System Modeling

MODELING

Designing the compensator for the constant current and constant voltage feedback loops requires linearized models for each of the components in the loops. This section presents these models.

BATTERY

The small signal model for a battery is simply its internal resistance, R_B. While the battery can be modeled as the series connection of the internal resistance and the storage capacitance, at any frequency of interest, the impedance of this connection is approximately R_B. Therefore, for simplicity, the storage capacitance is treated as a small signal short.

LINEAR REGULATORS

The small signal model for a linear voltage controlled current source is a transconductor with transconductance, G_M (see Figure 4). The transfer function for this block is

$$G_{PC}(s) = \frac{I_{OUT}}{V_{CTRL}} = \frac{G_M}{\tau \times s + 1}$$

where:

τ is the time constant of the block and models its finite bandwidth.
I_{OUT} is the output current.
V_{CTRL} is the input control voltage.

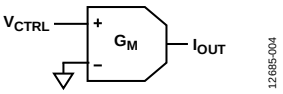

Figure 4. Linear Voltage Controlled Current Source, Small Signal Model

SWITCHING POWER CONVERTERS

Figure 5 shows the averaged linearized circuit of the nonisolated synchronous buck/boost converter. In this model circuit, the dc voltage bus, the PWM, and the switches are modeled as a linear amplifier with a voltage gain of A_V. In buck (charge) mode, the gain of the amplifier is V_{IN}/V_{RAMP}, where V_{IN} is the voltage of the dc bus and V_{RAMP} is the peak-to-peak voltage of the PWM ramp (4 V p-p in the ADP1972).

In boost (discharge) mode, the gain of the amplifier is $-V_{IN}/V_{RAMP}$. The linearized circuit in Figure 5 includes the parasitic resistance of the output inductor, R_L, and the output capacitor, R_C, of the power converter because they affect the transfer function of the converter.

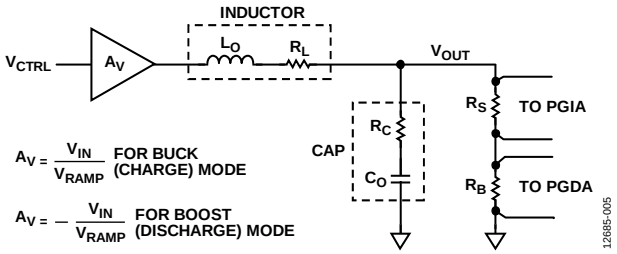

Figure 5. Averaged Linearized Circuit for the Nonisolated Synchronous Buck/Boost Converter

In buck (charge) mode, the buck/boost converter has the averaged transfer function shown in Equation 1.

$$G_{PC}(s) = \frac{V_{OUT}}{V_{CTRL}} = \frac{V_{IN}}{V_{RAMP}} \times \frac{R_D \times (R_C \times C_O \times s + 1)}{s^2 \times C_O \times L_O \times (R_D + R_C) + s \times (L_O + R_D \times R_C \times C_O + R_L \times C_O \times (R_D + R_C)) + R_D + R_L)} \quad (1)$$

where R_D is the load resistance of the converter ($R_B + R_S$).

In boost (discharge) mode, the buck/boost converter has the averaged transfer function shown in Equation 2.

$$G_{PC}(s) = \frac{V_{OUT}}{V_{CTRL}} = -\frac{V_{IN}}{V_{RAMP}} \times \frac{R_D \times (R_C \times C_O \times s + 1)}{s^2 \times C_O \times L_O \times (R_D + R_C) + s \times (L_O + R_D \times R_C \times C_O + R_L \times C_O \times (R_D + R_C)) + R_D + R_L)} \quad (2)$$

where R_D is the load resistance of the converter ($R_B + R_S$).

These equations show that the averaged linearized model of the buck/boost converter is a second order system with two poles and one zero. The two poles are generated by the LC filter, while the zero is caused by the series resistance of the output capacitor. Depending on the values of the circuit components, the transfer functions may be overdamped or underdamped. In the underdamped case, the poles are located at the resonant frequency of the LC filter, while, in the overdamped case, the poles may not be coincident. Figure 6 and Figure 7 show approximate Bode plots of the buck/boost converter.

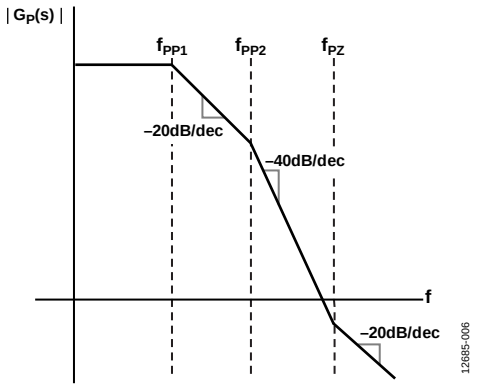

Figure 6. Magnitude Bode Plot of the Linearized Model of the Nonisolated Synchronous Buck/Boost Converter

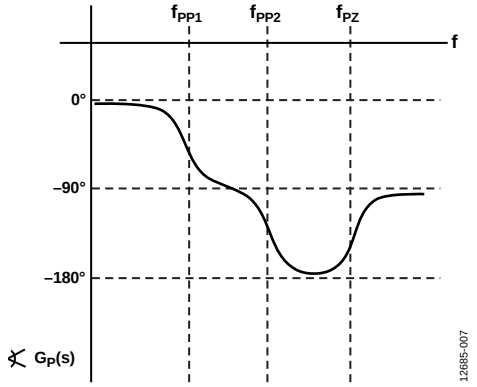

Figure 7. Phase Bode Plot of the Linearized Model of the Nonisolated Synchronous Buck/Boost Converter

CC AND CV FEEDBACK LOOPS

Given the CC-CV algorithm, only one of the two feedback loops can be in control of the power converter at any given time. Therefore, the two feedback loops can be modeled independently. These loops are modeled slightly differently depending on the output variable of the power converter, that is, if the power converter output variable is a voltage or a current.

Voltage Out Power Converters

For a voltage out power converter, like the nonisolated synchronous buck/boost power converter in Figure 3, the CC and CV loops are modeled using the block diagrams shown in Figure 8 and Figure 9.

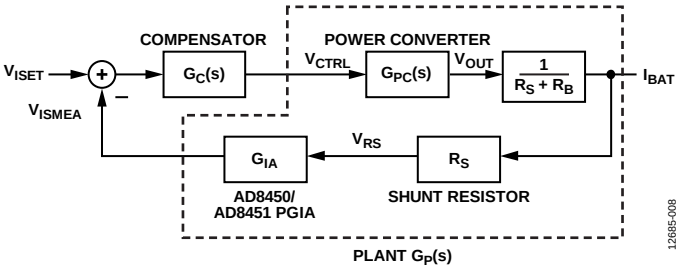

Figure 8. CC Loop Block Diagram for a Voltage Out Power Converter

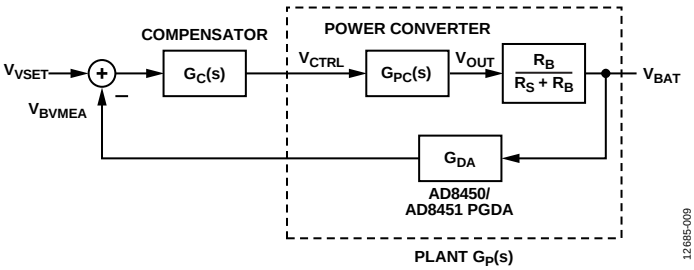

Figure 9. CV Loop Block Diagram for a Voltage Out Power Converter

The loop gain transfer function for the CC loop with a voltage out power converter is

$$L_{CC}(s) = G_C(s) \times G_{PC}(s) \times G_{IA} \times \frac{R_S}{R_S + R_B} \quad (3)$$

where:
$G_C(s)$ is the transfer function of the compensator.
$G_{PC}(s)$ is the transfer function of the power converter.
G_{IA} is the gain of the current sense instrumentation amplifier of the AD8450 or the AD8451.
R_S is the value of the current sense shunt resistor.
R_B is the value of the internal resistance of the battery.

Similarly, the loop gain transfer function for the CV loop is

$$L_{CV}(s) = G_C(s) \times G_{PC}(s) \times G_{DA} \times \frac{R_B}{R_S + R_B} \quad (4)$$

where G_{DA} is the gain of the voltage sense difference amplifier of the AD8450 or the AD8451.

Current Out Power Converters

For a current out power converter, like the linear regulator in Figure 2, the CC and CV loops are modeled using the block diagrams shown in Figure 10 and Figure 11.

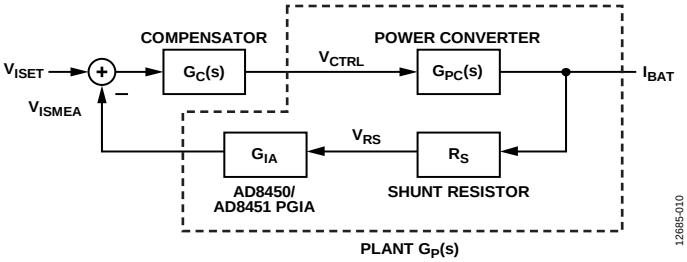

Figure 10. CC Loop Block Diagram for a Current Out Power Converter

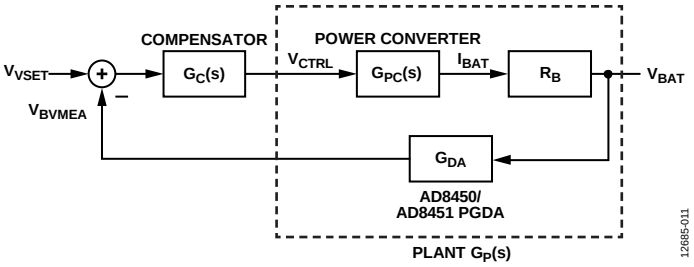

Figure 11. CV Loop Block Diagram for a Current Out Power Converter

The loop gain transfer function for the CC loop with a current out power converter is

$$L_{CC}(s) = G_C(s) \times G_{PC}(s) \times R_S \times G_{IA} \quad (5)$$

where:
$G_C(s)$ is the transfer function of the compensator.
$G_{PC}(s)$ is the transfer function of the power converter.
R_S is the value of the current sense shunt resistor.
G_{IA} is the gain of the current sense instrumentation amplifier of the AD8450 or the AD8451.

Similarly, the loop gain transfer function for the CV loop is

$$L_{CV}(s) = G_C(s) \times G_{PC}(s) \times R_B \times G_{DA} \quad (6)$$

where G_{DA} is the gain of the voltage sense difference amplifier of the AD8450 or the AD8451, and R_B is the value of the internal resistance of the battery.

COMPENSATOR DESIGN

The following steps establish the procedure to design the compensator of the CC and CV loops using the AD8450 or the AD8451:

1. Gather the parameters of the power converter and the analog front end (AD8450 or AD8451).
2. Determine the transfer function of the uncompensated system, $G_P(s)$, and calculate the location of the poles and zeros.
3. Determine the crossover frequency of the system.
4. Select the compensator type.
5. Select the compensator pole and zero locations.
6. Set the gain of the compensator at the crossover frequency.
7. Calculate the compensator component values.

UNCOMPENSATED SYSTEM

When designing the compensator for a system, all the elements in the feedback loop, excluding the compensator, form the uncompensated system or plant. For the CC and CV loops, see the uncompensated transfer functions, $G_P(s)$, in Table 1.

COMPENSATOR DESIGN STEPS FOR THE SYNCHRONOUS BUCK/BOOST CONVERTER

Step 1: Gather the Parameters for the Power Converter and the Analog Front End (AD8450 or AD8451)

The first step in designing the compensator for the CC and CV feedback loops is to extract the relevant parameters of the buck/boost converter and the analog front end of the AD8450 or the AD8451. These parameters include

- L_O, the output inductor of the converter
- C_O, the output capacitor of the converter
- R_L, the ESR of the output inductor
- R_C, the ESR of the output capacitor
- R_B, the ESR of the battery
- R_S, the value of the shunt resistor
- R_D, the load resistance ($R_S + R_B$) of the converter
- f_S, the switching frequency of the converter
- V_{IN}, the dc bus voltage
- V_{RAMP}, the ramp voltage
- G_{IA}, the PGIA gain of the AD8450 or the AD8451
- G_{DA}, the PGDA gain of the AD8450 or the AD8451

Step 2: Determine the Transfer Function of the Uncompensated System, $G_P(s)$, and Calculate the Location of the Poles and Zeros

After gathering the parameters of the power converter and front end of the AD8450 or the AD8451, determine the exact transfer function of the uncompensated system or plant. Because the nonisolated buck/boost converter is a voltage out power converter, for the CC feedback loop, the transfer function of the plant is

$$G_{P\text{-}CC}(s) = \frac{V_{IN}}{V_{RAMP}} \times \frac{(R_S + R_B) \times (s \times R_C \times C_O + 1)}{a \times s^2 + b \times s + c} \times G_{IA} \times \frac{R_S}{R_S + R_B} \quad (7)$$

where:

$a = L_O \times C_O \times (R_D + R_C)$

$b = R_D \times R_C \times C_O + L_O + R_L \times C_O \times (R_D + R_C)$

$c = R_D + R_L$

For the CV feedback loop, the transfer function of the plant is

$$G_{P\text{-}CV}(s) = \frac{V_{IN}}{V_{RAMP}} \times \frac{(R_S + R_B) \times (s \times R_C \times C_O + 1)}{a \times s^2 + b \times s + c} \times G_{DA} \times \frac{R_B}{R_S + R_B} \quad (8)$$

where:

$a = L_O \times C_O \times (R_D + R_C)$

$b = R_D \times R_C \times C_O + L_O + R_L \times C_O \times (R_D + R_C)$

$c = R_D + R_L$

Due to the equivalent series resistance (ESR) of the output capacitor of the converter, the transfer functions, $G_P(s)$, have a zero at

$$f_{PZ} = \frac{1}{2\pi \times R_C \times C_O} \quad (9)$$

Due to the LC filter of the converter, the transfer functions, $G_P(s)$, have two poles at

$$f_{PP1}, f_{PP2} = \left| \frac{b \pm \sqrt{b^2 - 4 \times a \times c}}{2 \times a \times 2\pi} \right| \quad (10)$$

Pole PP1 is the lower frequency pole, and it may be coincident with Pole PP2, depending on the value of the $b^2 - 4 \times a \times c$ term.

Table 1. Summary of Uncompensated Systems

Converter/Loop	Voltage Out	Current Out
Constant Current	$G_{P-CC}(s) = G_{PC}(s) \times G_{IA} \times \frac{R_S}{R_S + R_B}$	$G_{P-CC}(s) = G_{PC}(s) \times G_{IA} \times R_S$
Constant Voltage	$G_{P-CV}(s) = G_{PC}(s) \times G_{DA} \times \frac{R_B}{R_S + R_B}$	$G_{P-CV}(s) = G_{PC}(s) \times G_{DA} \times R_B$

Note that, unlike most buck/boost converters, it is not safe to assume that the converter poles are at $f_{PP1} = f_{PP2} = 1/\sqrt{(LC)}$. The battery and the shunt resistor present a heavy load to the converter that may move the converter poles away from $1/\sqrt{(LC)}$.

Step 3: Determine the Crossover Frequency of the System

Next, choose the crossover frequency of the system. To guarantee the accuracy of the linearized averaged model of the power converter, set the crossover frequency of the system to 10 times lower than the switching frequency. See Equation 11.

$$f_C = \frac{f_S}{10} \quad (11)$$

After selecting f_C, verify that the frequencies of the slowest converter pole (f_{PP1}) are at least a decade lower than the crossover frequency of the system. This requirement reduces the adverse effects of the LC resonance near crossover. Therefore, verify that

$$f_{PP1} \leq \frac{f_C}{10} \quad (12)$$

If this condition is not met, consider increasing the switching frequency, f_S, or decreasing the frequency of the converter poles, f_{PP1} and f_{PP2}.

Note that, at a given gain for the PGIA and PGDA of the AD8450 or the AD8451, there exists a maximum frequency that the analog front end can support. See the AD8450 and AD8451 Bandwidth Considerations section for the exact specifications.

Step 4: Select the Compensator Type

Depending on the location of f_C, with respect to f_{PP1}, f_{PP2}, and f_{PZ}, select the appropriate compensator type. For the nonisolated buck/boost converter, proportional integral (PI) Type II and proportional integral derivative (PID) Type III compensators are recommended. An integral Type I compensator may also be used, but it is not recommended due to the low system bandwidths it requires.

To maximize the open-loop gain of the CC and CV feedback loops, and therefore the accuracy of the system, the compensator must have a pole at the origin (the integral component of the compensator). This pole at the origin adds a −90° phase shift to the feedback loops, destabilizing them if their crossover frequency is higher than the converter poles, that is, if $f_C > f_{PP1}, f_{PP2}$. As a result, in addition to adding a pole at the origin, the compensator must provide a phase boost near the crossover frequency, f_C.

The Type II compensator implements a pole at the origin, a zero at a frequency below the crossover frequency of the system, and a high frequency pole. This compensator is used when the magnitude of the uncompensated system rolls off at −20 dB/dec at the desired crossover frequency, f_C. Figure 12, Figure 13, and Figure 14 show the magnitude Bode plots of the uncompensated system, $G_P(s)$, the Type II compensator, $G_C(s)$, and the compensated system, L(s), respectively.

The Type III compensator implements a pole at the origin, two zeros at frequencies below the crossover frequency of the system, and two high frequency poles. This compensator is used when the magnitude of the uncompensated system rolls off at −40 dB/dec at the desired crossover frequency, f_C. Figure 15, Figure 16, and Figure 17 show the magnitude Bode plots of the uncompensated system, $G_P(s)$, the Type III compensator, $G_C(s)$, and the compensated system, L(s), respectively.

The high frequency poles of the Type II and Type III compensators are usually placed at a frequency between f_C and f_S. These poles help attenuate the output ripple of the power converter without significantly affecting the phase margin of the compensated system.

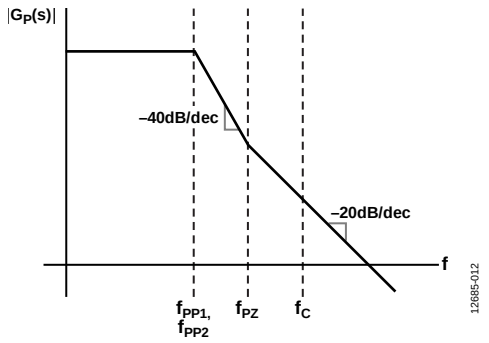

Figure 12. Magnitude Bode Plot of the Uncompensated System $G_P(s)$

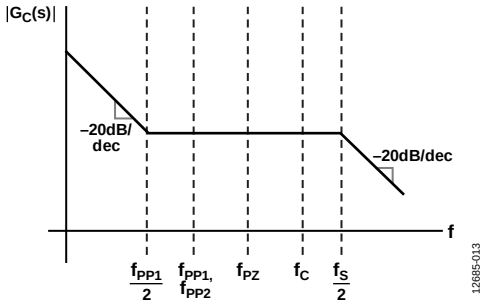

Figure 13. Magnitude Bode Plot of the Type II Compensator $G_C(s)$

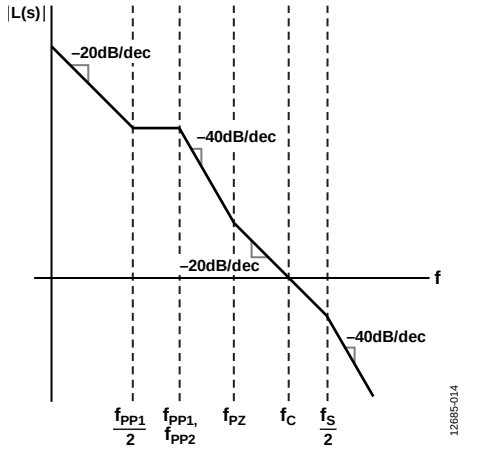

Figure 14. Magnitude Bode Plot of the Compensated System $L(s)$

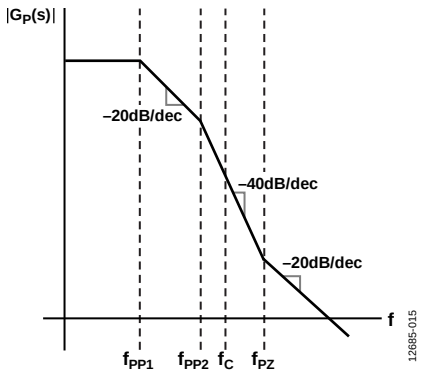

Figure 15. Magnitude Bode Plot of the Uncompensated System $G_P(s)$

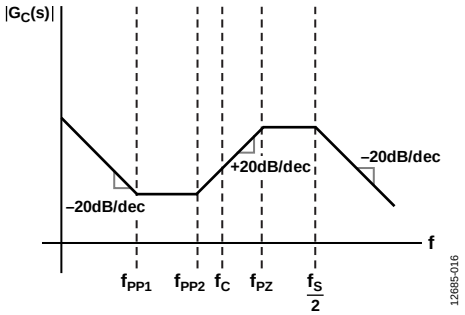

Figure 16. Magnitude Bode Plot of the Type III Compensator $G_C(s)$

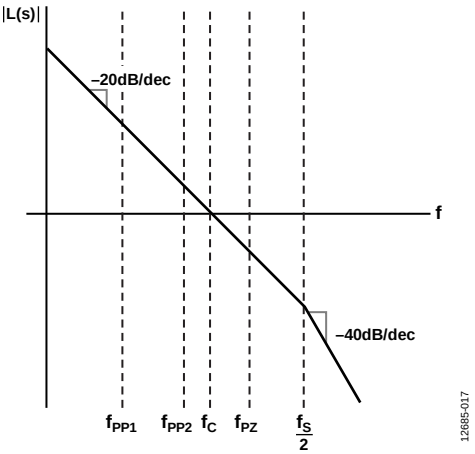

Figure 17. Magnitude Bode Plot of the Compensated System $L(s)$

Figure 12 through Figure 17 show that the selection between the Type II and Type III compensator depends on where the zero of the converter is located with respect to where the crossover frequency of the feedback loops is located. Therefore, the recommended rules for compensator type selection are

- If $f_{PZ} \times 3 \leq f_C$, use a Type II compensator
- If $f_{PZ} \times 3 \geq f_C$, use a Type III compensator

The Type II and Type III compensators are implemented using the CC and CV error amplifiers of the AD8450 or the AD8451 (Amplifier A1 and Amplifier A2 in Figure 1). In charge mode, the CC and CV feedback loops require inverting compensators to maintain negative feedback because there are no inversions in the loops. Figure 18 and Figure 19 show practical implementations of inverting Type II and Type III compensators.

In discharge mode, the converter is operated in boost mode, and the transfer function of the converter exhibits an inversion. Despite this inversion, in discharge mode, the CC feedback loop requires an inverting compensator because the MODE pin of the AD8450 and the AD8451 changes the gain polarity of the PGIA. However, because the gain polarity of the PGDA is not altered by the MODE pin in discharge mode, the CV loop requires a noninverting integrator. Figure 20 and Figure 21 show practical implementations of the noninverting Type II and Type III compensators.

Note that if the same resistor and capacitor values are used in the inverting and noninverting compensators, the transfer functions of the compensators of a given type are identical, except for the polarity of their dc gain.

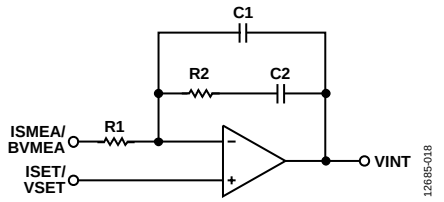

Figure 18. Inverting Type II Compensator

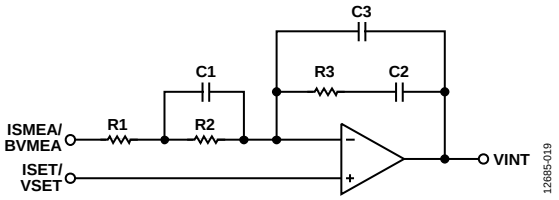

Figure 19. Inverting Type III Compensator

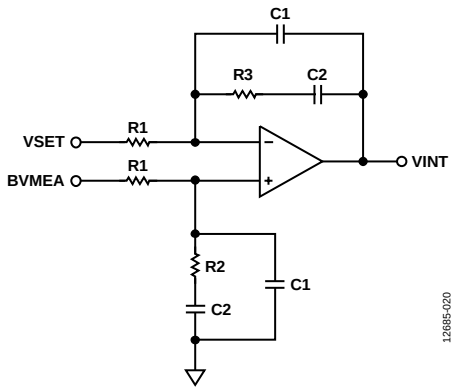

Figure 20. Noninverting Type II Compensator

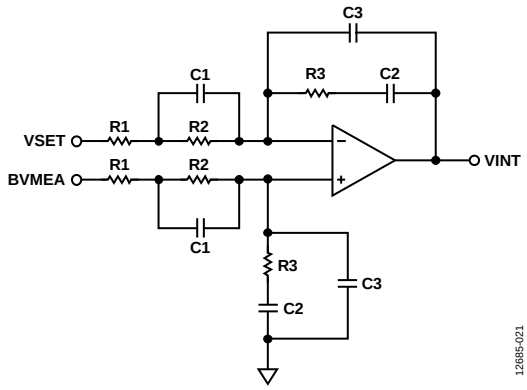

Figure 21. Noninverting Type III Compensator

Step 5: Choose the Compensator Pole and Zero Locations

The next step in compensating the CC and the CV feedback loops is to choose the locations of the compensator poles and zeros and to calculate their corresponding time constants.

Type II Compensator Pole and Zero Locations

Place the Type II compensator zero at a frequency significantly below f_C, such that the compensator pole at the origin induces only a small phase shift at the crossover frequency. Additionally, place the zero before the poles of the power converter to avoid a −180° phase shift in the loop gain before the crossover frequency. These two restrictions place the zero of the compensator at

$$f_{CZ} = \min\left\{\frac{f_C}{10}, \frac{f_{PP1}}{2}\right\} = \frac{1}{2\pi \times \tau_1} \quad (13)$$

To limit phase margin degradation, place the pole of the compensator at a frequency significantly higher than frequency f_C. Additionally, place the pole at a frequency below f_S to attenuate the switching ripple of the converter. These constraints place the pole at

$$f_{CP} = f_C \times 5 = \frac{f_S}{2} = \frac{1}{2\pi \times \tau_2} \quad (14)$$

Figure 12 through Figure 14 illustrate the suggested pole and zero placements for the Type II compensator. The uncompensated system magnitude Bode plot shows the magnitude of $G_P(s)$ rolling off at −20 dB/dec at f_C, because the zero of the converter is at a frequency below the crossover frequency. Also, at f_C, the slope of the compensator is approximately 0; therefore, the loop gain of the compensated system, L(s), crosses over with a slope of −20 dB/dec, ensuring a stable system.

Type III Compensator Pole and Zero Locations

Place the Type III compensator zeros at the same frequency of the poles of the converter, such that they cancel each other out. See Equation 15 and Equation 16.

$$f_{CZ1} = f_{PP1} = \frac{1}{2\pi} \times \tau_1 \quad (15)$$

$$f_{CZ2} = f_{PP1} = \frac{1}{2\pi} \times \tau_2 \quad (16)$$

Place the Type III compensator poles at $f_S/2$ to attenuate the switching ripple of the converter. If the power converter zero is located near the crossover frequency, f_C, place one of the compensator poles at f_{PZ} to cancel out the zero. This cancellation prevents the zero of the converter from altering the magnitude of the compensated system at f_C. These restrictions place the poles at

$$f_{CP1} = \min\left\{\frac{f_S}{2}, f_{PZ}\right\} = \frac{1}{2\pi \times \tau_3} \quad (17)$$

$$f_{CP2} = \frac{f_S}{2} = \frac{1}{2\pi \times \tau_4} \quad (18)$$

Figure 15 through Figure 17 illustrate the suggested pole and zero placements for the Type III compensator. The uncompensated system Bode plot shows the magnitude of $G_P(s)$ rolling off at −40 dB/dec at f_C, because the zero of the converter is at a frequency above the crossover frequency. Also, at f_C, the slope of the compensator is approximately +20 dB/dec; therefore, the loop gain of the compensated system, L(s), crosses over with a slope of −20 dB/dec, ensuring a stable system.

Step 6: Set the Gain of the Compensator at the Crossover Frequency

The crossover frequency of the CC and CV feedback loops is established by setting the gain of their compensator at the crossover frequency. At f_C, set the gain of the compensator to the inverse of the gain of the uncompensated system.

$$\left|G_C(f_C)\right| = \frac{1}{\left|G_P(f_C)\right|} \tag{19}$$

For the CC feedback loop, the gain of the uncompensated system at f_C is

$$\left|G_P(f_C)\right| = \frac{1}{\left|G_C(f_C)\right|} = \frac{V_{IN} \times G \times R_S}{V_{RAMP}} \times \sqrt{\frac{(2\pi \times f_C \times C_O \times R_C)^2 + 1}{(b \times 2\pi \times f_C)^2 + (c - a \times (2\pi \times f_C)^2)^2}} \tag{20}$$

where:
$a = L_O \times C_O \times (R_D + R_C)$
$b = R_D + R_C + C_O + L_O + R_L + C_O (R_D + R_C)$
$c = R_D + R_L$

For the CV feedback loop, the gain of the uncompensated system at f_C is

$$\left|G_P(f_C)\right| = \frac{1}{\left|G_C(f_C)\right|} = \frac{V_{IN} \times G \times R_B}{V_{RAMP}} \times \sqrt{\frac{(2\pi \times f_C \times C_O \times R_C)^2 + 1}{(b \times 2\pi \times f_C)^2 + (c - a(2\pi \times f_C)^2)^2}} \tag{21}$$

where:
$a = L_O \times C_O \times (R_D + R_C)$
$b = R_D + R_C + C_O + L_O + R_L + C_O (R_D + R_C)$
$c = R_D + R_L$

Step 7: Calculate the Compensator Component Values

Figure 18 through Figure 21 show practical implementations of the inverting and noninverting Type II and Type III compensators. The transfer function of the inverting Type II compensator is shown in Equation 22. The transfer function of the inverting Type III compensator is shown in Equation 23.

$$G_{CII-INV}(s) = -\frac{1}{s \times R1 \times (C1 + C2)} \times \frac{(1 + s \times R2 \times C2)}{\left(1 + s \times R2 \times \frac{C1 \times C2}{C1 + C2}\right)} = -\frac{K}{s} \times \frac{1 + s \times \tau_1}{1 + s \times \tau_2} \tag{22}$$

$$G_{CIII-INV}(s) = -\frac{1}{s \times (R1 + R2) \times (C2 + C3)} \times \frac{(1 + s + R3 \times C2) \times 1 + s \times R2 \times C1}{\left(1 + s \times R3 \times \frac{C2 \times C3}{C2 + C3}\right) \times \left(1 + s \times C1 \times \frac{R1 \times R2}{R1 + R2}\right)} = -\frac{K}{s} \times \frac{(1 + s \times \tau_1) \times (1 + s \times \tau_2)}{(1 + s \times \tau_3) \times (1 + s \times \tau_4)} \tag{23}$$

The transfer functions of the noninverting compensators are identical to the transfer functions of the inverting compensators, except for the inversion, which is not present. The transfer function of the noninverting Type II compensator is shown in Equation 24. The transfer function of the noninverting Type III compensator is shown in Equation 25.

$$G_{CII-NON-INV}(s) = -G_{CII-INV}(s) = \frac{1}{s \times R1 \times (C1 + C2)} \times \frac{(1 + s \times R2 \times C2)}{\left(1 + s \times R2 \times \frac{C1 \times C2}{C1 + C2}\right)} = -\frac{K}{s} \times \frac{1 + s \times \tau_1}{1 + s \times \tau_2} \tag{24}$$

$$G_{CIII-NON-INV}(s) = -G_{CIII-INV}(s) = \frac{1}{s \times (R1 + R2) \times (C2 + C3)} \times \frac{(1 + s + R3 \times C2) \times 1 + s \times R2 \times C1}{\left(1 + s \times R3 \times \frac{C2 \times C3}{C2 + C3}\right) \times \left(1 + s \times C1 \times \frac{R1 \times R2}{R1 + R2}\right)} = -\frac{K}{s} \times \frac{(1 + s \times \tau_1) \times (1 + s \times \tau_2)}{(1 + s \times \tau_3) \times (1 + s \times \tau_4)} \tag{25}$$

Note that the transfer functions of the compensators are only dependent on impedance ratios; therefore, there is a degree of freedom in the calculation of the component values. A practical starting point is to select a reasonable value for C2 (such as 10 nF) and then calculate the other values.

Type II Component Values

After choosing the value for C2, the remaining component values for the Type II compensator are calculated using Equation 26 through Equation 28.

$$R2 = \frac{\tau_1}{C2} \tag{26}$$

$$C1 = C2 \times \frac{\tau_2}{\tau_1 - \tau_2} \tag{27}$$

$$R1 = \left| \frac{G_P(f_C)}{2\pi \times f_C \times (C1 + C2)} \times \frac{1 + j \times 2\pi \times f_C \times \tau_1}{1 + j + 2\pi \times f_C \times \tau_2} \right| \tag{28}$$

where:

$\tau_1 = \frac{1}{2\pi \times f_{CZ}}$

$\tau_2 = \frac{1}{2\pi \times f_{CP}}$

Type III Component Values

After choosing the value for C2, the remaining component values for the Type III compensator are calculated similarly to the Type II compensator, using Equation 29 through Equation 33.

$$R3 = \frac{\tau_1}{C2} \quad (29)$$

$$C3 = C2 \times \frac{\tau_3}{\tau_1 - \tau_3} \quad (30)$$

$$C1 = \frac{\tau_2}{R2} \quad (31)$$

$$R1 = R2 \times \frac{\tau_4}{\tau_2 - \tau_4} \quad (32)$$

$$R2 = \left| \frac{G_P(f_C) \times (1 + j + 2\pi \times f_C \times \tau_1) \times (1 + j \times 2\pi \times f_C \times \tau_2)}{2\pi \times f_C \times (C2 + C3) \times (1 + j \times 2\pi \times f_C \times \tau_3) \times (1 + j + 2\pi \times f_C \times \tau_4) \times \left(\frac{\tau_2}{\tau_2 - \tau_4} \right)} \right| \quad (33)$$

where:

$\tau_1 = \frac{1}{2\pi \times f_{CZ1}}$

$\tau_2 = \frac{1}{2\pi \times f_{CZ2}}$

$\tau_3 = \frac{1}{2\pi \times f_{CP1}}$

$\tau_4 = \frac{1}{2\pi \times f_{CP2}}$

If any of the component values of the compensators are too large or too small to be practical, the component values may be scaled because the compensator transfer functions only depend on impedance ratios. If necessary, adjust the component values by scaling all the impedances equally, that is, scale all resistances by a factor α and all capacitances by 1/α.

AD8450 AND AD8451 BANDWIDTH CONSIDERATIONS

The sense amplifiers of the AD8450 and the AD8451, the PGIA and the PGDA, have finite bandwidths that are gain dependent. These finite bandwidths impose an upper limit on the crossover frequency of the CC and CV feedback loops. The recommended upper limit for the crossover frequency of a loop is a tenth of the bandwidth of the sense amplifier of the loop. Table 2 summarizes the recommended upper limit for the crossover frequency of the CC and CV feedback loops of the AD8450. Note that the AD8451 has one PGIA gain of 26 and one PGDA gain of 0.8, as shown in Table 3.

If extra filtering is required, the bandwidths of the sense amplifiers can be reduced by means of input filters. Note that reducing the bandwidth of the sense amplifiers also reduces the upper limit for the crossover frequency of the CC and CV feedback loops.

Table 2. Recommended Maximum Crossover Frequency for the CC and CV Feedback Loops of the AD8450

CC Feedback Loop		CV Feedback Loop	
PGIA Gain	Maximum CC f_C (kHz)	PGDA Gain	Maximum CV f_C (kHz)
26	150	0.2	42
66	63	0.27	73
133	33	0.4	94
200	22	0.8	100

Table 3. Recommended Maximum Crossover Frequency for the CC and CV Feedback Loops of the AD8451

CC Feedback Loop		CV Feedback Loop	
PGIA Gain	Maximum CC f_C (kHz)	PGDA Gain	Maximum CV f_C (kHz)
26	150	0.8	100

DESIGN EXAMPLES

CONSTANT CURRENT FEEDBACK LOOP WITH A TYPE II COMPENSATOR

Step 1: Gather the Parameters of the Power Converter and the Analog Front End (AD8450 or AD8451)

Table 4 shows the parameters of the power converter and analog front end for this example.

Table 4. Power Converter and Analog Front End Parameters for the Type II Design Example

Parameter	Value
L_O	150 µH
C_O	1000 µF
R_L	70 mΩ
R_C	50 mΩ
R_B	50 mΩ
R_S	20 mΩ
f_S	100 kHz
G_{IA}	200
V_{IN}	24 V
V_{RAMP}	4 V

Step 2: Calculate the Location of the Uncompensated System Poles and Zeros

After gathering the parameters of the power converter and the front end of the AD8450 or the AD8451, determine the exact transfer function of the uncompensated system or plant. Using Equation 7 and Equation 8, the denominator coefficients of the transfer function of the plant are

$$a = 1.8 \times 10^{-8}$$

$$b = 1.61 \times 10^{-4}$$

$$c = 1.4$$

Using Equation 9 and Equation 10, the power converter poles are at

$$f_{PP1} = 154 \text{ kHz}$$

$$f_{PP2} = 1.28 \text{ kHz}$$

The power converter zero is at

$$f_{PZ} = 3.18 \text{ kHz}$$

Step 3: Determine the Crossover Frequency of the System

Set the crossover frequency of the loop a decade below the switching frequency, such that

$$f_C = 10 \text{ kHz}$$

Using Equation 11, verify that the crossover frequency is not close to any potential resonance.

$$f_{PP1} = 154 \text{ Hz} < 1 \text{ kHz} = \frac{f_C}{10}$$

Step 4: Select the Compensator Type

Select a Type II compensator because the crossover frequency of the loop, f_C, is located after the converter poles and after three times the frequency of the converter zero.

Step 5: Select the Compensator Pole and Zero Locations

Using Equation 13 and Equation 14, the compensator pole and zero are at

$$f_{CZ} = 77 \text{ Hz}$$

$$f_{CP} = 50 \text{ kHz}$$

Step 6: Set the Gain of the Compensator at the Crossover Frequency

Using Equation 20, the magnitude of the uncompensated system at f_C is

$$\left|G_P(f)\right| = 1.104$$

Step 7: Calculate the Compensator Component Values

Using Equation 26 through Equation 28, the component values for the Type II compensator are

$$R1 = 22.3 \text{ kΩ}$$

$$R2 = 20.6 \text{ kΩ}$$

$$C1 = 154 \text{ pF}$$

$$C2 = 100 \text{ nF}$$

Figure 22, Figure 23, and Figure 24 show the magnitude Bode plots of the uncompensated system, the compensator, and the compensated system, respectively. As expected, the compensated system crosses over with a slope of −20 dB/dec at f_C = 10 kHz, guaranteeing a stable system.

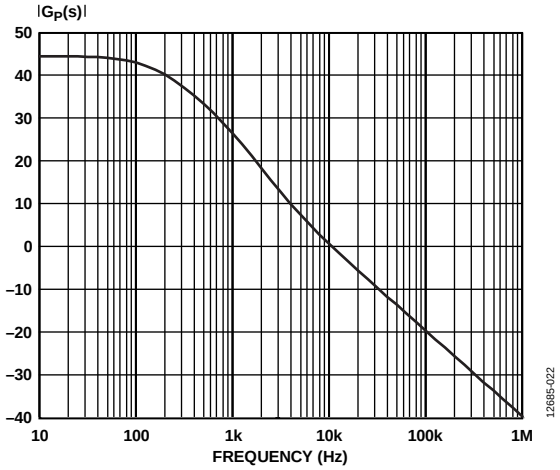

Figure 22. Magnitude Bode Plot of the Uncompensated System $G_P(s)$

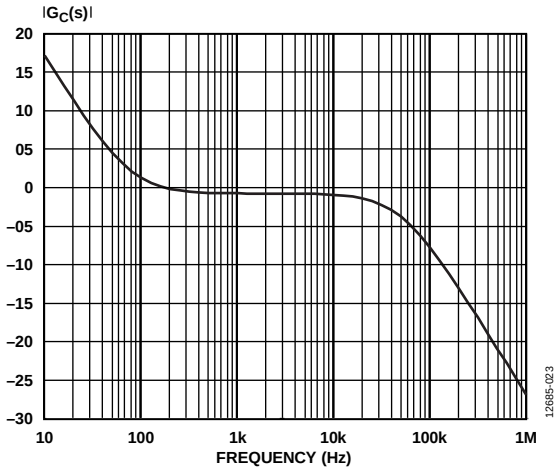

Figure 23. Magnitude Bode Plot of the Type II Compensator $G_C(s)$

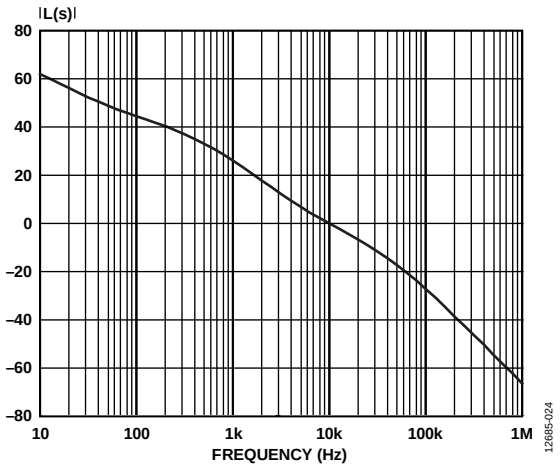

Figure 24. Magnitude Bode Plot of the Compensated System $L(s)$

CONSTANT CURRENT FEEDBACK LOOP WITH A TYPE III COMPENSATOR

Step 1: Gather the Parameters of the Power Converter and the Analog Front End (AD8450 or AD8451)

Table 5 shows the parameters of the power converter and analog front end for this example.

Table 5. Power Converter and Analog Front End Parameters for Type III Design Example

Parameter	Value
L_O	150 µH
C_O	250 µF
R_L	70 mΩ
R_C	7.5 mΩ
R_B	50 mΩ
R_S	20 mΩ
f_S	100 kHz
G_{IA}	200
V_{IN}	24 V
V_{RAMP}	4 V

Step 2: Calculate the Location of the Uncompensated System Poles and Zeros

After gathering the parameters of the power converter and front end of the AD8450 or the AD8451, determine the exact transfer function of the uncompensated system or plant. Using Equation 7 through Equation 8, the denominator coefficients of the transfer function of the plant are

$$a = 2.9 \times 10^{-9}$$

$$b = 1.51 \times 10^{-4}$$

$$c = 0.14$$

Using Equation 9 and Equation 10, the power converter poles are at

$$f_{PP1} = 150 \text{ Hz}$$

$$f_{PP2} = 8.15 \text{ kHz}$$

The power converter zero is at

$$f_{PZ} = 85 \text{ kHz}$$

Step 3: Determine the Crossover Frequency of the System

Set the crossover frequency of the loop a decade below the switching frequency, such that

$$f_C = 10 \text{ kHz}$$

Using Equation 12, verify that the crossover frequency is not close to any potential resonance.

$$f_{PP1} = 150 \text{ Hz} < 1 \text{ kHz} = \frac{f_C}{10}$$

Step 4: Select the Compensator Type

Select a Type III compensator because the crossover frequency of the loop, f_C, is located after the converter poles and before three times the frequency of the converter zero.

Step 5: Select the Compensator Pole and Zero Locations

Using Equation 15 through Equation 18, the compensator zeros are at

f_{CZ1} = 150 Hz

f_{CZ2} = 8.15 kHz

Because $f_S/2 < f_{PZ}$, the poles are located at

$f_{CP1} = f_{CP2}$ = 50 kHz

Step 6: Calculate the Plant Gain at Crossover

Using Equation 20, the magnitude of the uncompensated system at f_C is

$$\left|G_P(f_C)\right| = 1.63$$

Step 7: Calculate the Compensator Component Values

Using Equation 29 through Equation 33, the component values for the Type III Compensator are

$R1$ = 43 kΩ

$R2$ = 220 kΩ

$R3$ = 106 kΩ

$C1$ = 88.6 pF

$C2$ = 10 nF

$C3$ = 30 pF

Figure 25, Figure 26, and Figure 27 show the magnitude Bode plots of the uncompensated system, the compensator, and the uncompensated system, respectively. As expected, the compensated system crosses over with a slope of −20 dB/dec at f_C = 10 kHz, guaranteeing a stable system.

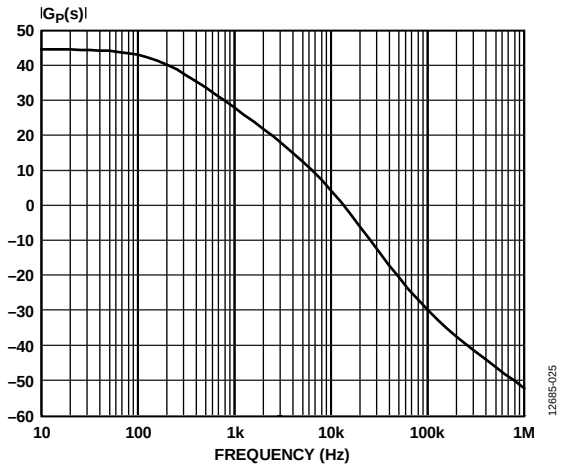

Figure 25. Magnitude Bode Plot of the Uncompensated System $G_P(s)$

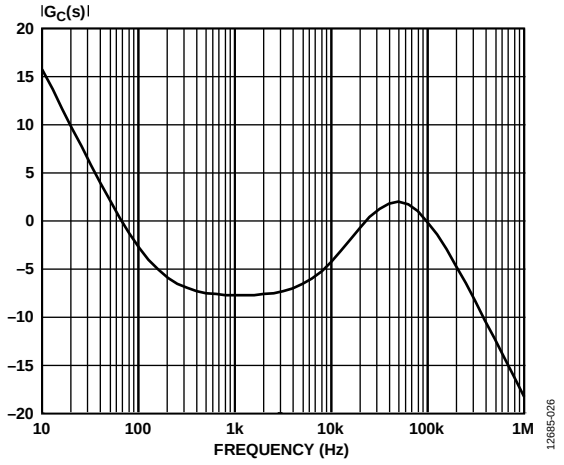

Figure 26. Magnitude Bode Plot of the Type III Compensator $G_C(s)$

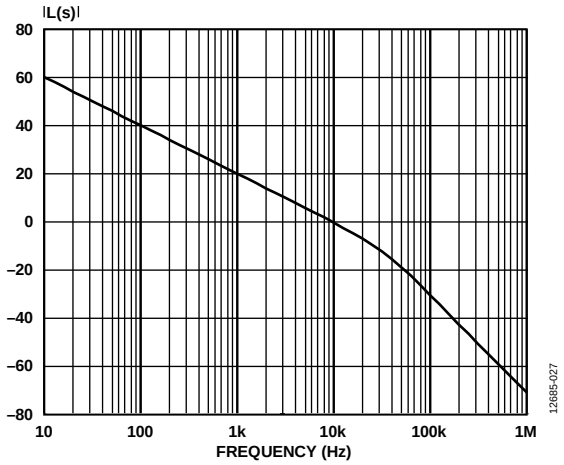

Figure 27. Magnitude Bode Plot of the Compensated System $L(s)$

SPECIAL CASES

CROSSOVER FREQUENCY BEFORE f_{PP2}

There may be cases where the desired crossover frequency occurs between the two converter poles, f_{PP1} and f_{PP2}. In these cases, use a Type II compensator. To maintain a 65° phase margin, use a Type II compensator if $f_{PP1} < f_C < f_C \times 3 < f_{PP2}$.

To calculate the pole and zero locations of the compensator and the component values of the associated circuit, follow the same steps described in the Compensator Design section.

LINEAR REGULATORS

Linear regulators are often used in low power battery testing and formation systems due to their simplicity. Linear regulators can be either voltage controlled voltage sources or voltage controlled current sources. A linear voltage controlled current source is modeled with the following transfer function:

$$G_{LPC}(s) = \frac{G_M}{\tau \times s + 1} \quad (34)$$

where G_M is the regulator transconductance, and the pole models the regulator finite bandwidth. For frequencies significantly below this pole, the power converter has a uniform gain and approximately 0° of phase.

For the CC feedback loop, the transfer function of the uncompensated system is

$$G_{P-CC}(s) = G_{IA} \times \frac{G_M}{\tau \times s + 1} \times R_S \quad (35)$$

For the CV feedback loop, the transfer function of the uncompensated system is

$$G_{P-CV}(s) = G_{DA} \times \frac{G_M}{\tau \times s + 1} \times R_B \quad (36)$$

STEPS FOR COMPENSATING LINEAR REGULATORS

Step 1: Gather the Parameters of the Uncompensated System

The first step in designing the compensator for the CC and CV feedback loops is to extract the relevant parameters of the linear regulator and the analog front end of the AD8450 or the AD8451. These parameters include

- G_M, the transconductance of the linear regulator
- τ, the time constant of the linear regulator (bandwidth = $1/(2\pi \times \tau)$)
- R_B, the ESR of the battery
- R_S, the value of the shunt resistor
- G_{IA}, the PGIA gain of the AD8450 or the AD8451
- G_{DA}, the PGDA gain of the AD8450 or the AD8451

Step 2: Determine the Crossover Frequency of the System

Choose the crossover frequency of the CC and CV feedback loops to be at least five times lower than the bandwidth of the linear regulator, as shown in Equation 37.

$$f_C \leq \frac{1}{2\pi \times \tau \times 5} \quad (37)$$

This condition minimizes the impact of the bandwidth of the linear regulator on the stability of the feedback loops.

Step 3: Calculate the Gain of the Compensator at the Crossover Frequency

The crossover frequency of the CC and CV feedback loops is established by setting the gain of their compensator at the crossover frequency. At f_C, set the gain of the compensator to the inverse of the gain of the uncompensated system. See Equation 38.

$$\left|G_C(f_C)\right| = \frac{1}{\left|G_P(f_C)\right|} \quad (38)$$

If f_C is sufficiently lower than the bandwidth of the linear regulator, for the CC feedback loop, the gain of the uncompensated system is approximately

$$\left|G_{P-CC}(f_C)\right| = G_{IA} \times G_M \times R_S$$

For the CV feedback loop, the gain of the uncompensated system is approximately

$$\left|G_{P-CV}(f_C)\right| = G_{DA} \times G_M \times R_B$$

Step 4: Choose the Compensator Type

Because the phase shift of the uncompensated system at f_C is less than −25° (due to f_C being five times less than the regulator bandwidth), a Type I or integral compensator is appropriate. Type I compensators implement a single pole at the origin and have a −90° phase shift for all frequencies. Therefore, at the crossover frequency, the phase of the loop is less than −125°, guaranteeing a phase margin of at least 65°. The transfer function for a Type I compensator is

$$G_{CI}(s) = \pm \frac{K}{s} \quad (39)$$

In charge mode, the CC and CV feedback loops require inverting compensators to maintain negative feedback. Figure 28 shows a practical implementation of an inverting Type I compensator.

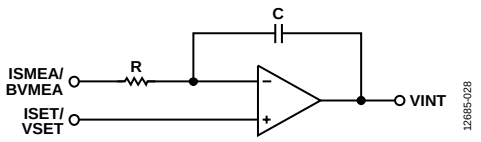

Figure 28. Inverting Type I Compensator

The transfer function of the inverting Type I compensator is

$$G_{CI\text{-}INV}(s) = -\frac{1}{R \times C \times s} \quad (40)$$

In discharge mode, the CC feedback loop requires an inverting compensator, but the CV feedback loop requires a noninverting compensator. Figure 29 shows a practical implementation of a noninverting Type I compensator.

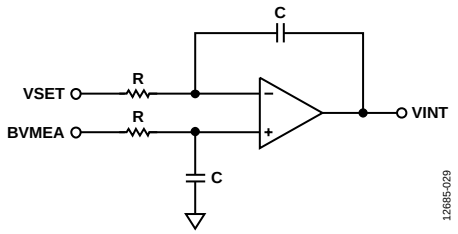

Figure 29. Noninverting Type I Compensator

The transfer function of the noninverting Type I compensator is

$$G_{CI\text{-}NON\text{-}INV}(s) = \frac{1}{R \times C \times s} \quad (41)$$

Step 5: Calculate the Compensator Component Values

The R and C values of the Type I compensators shown in Figure 28 and Figure 29 set the gain of the compensator at a given frequency, as well as the crossover frequency of the CC and CV feedback loops. The crossover frequency of the loops occurs when

$$\left|G_P(f_C)\right| = \frac{1}{\left|G_C(f_C)\right|} \quad (42)$$

For the CC feedback loop, this condition translates to

$$R \times C \times 2\pi \times f_C = G_{IA} \times G_M \times R_S$$

For the CV feedback loop, this condition implies

$$R \times C \times 2\pi \times f_C = G_{DA} \times G_M \times R_B$$

Therefore, for a given f_C, the product of R and C is chosen such that

$$R \times C = \frac{\left|G_P(f_C)\right|}{f_C \times 2\pi} \quad (43)$$

Because the transfer function of the Type I compensator depends on the product of R and C, there is a degree of freedom in the calculation of the component values. A practical starting point is to select a reasonable value for C (such as 10 nF) and then calculate the value of R to achieve the desired crossover frequency.

For the CC feedback loop, use Equation 44.

$$R = \frac{G_{IA} \times R_S \times G_M}{C \times 2\pi \times f_C} \quad (44)$$

For the CV feedback loop, use Equation 45.

$$R = \frac{G_{DA} \times R_B \times G_M}{C \times 2\pi \times f_C} \quad (45)$$

CONCLUSION

This application note describes a methodology to design the compensators of the CC and CV feedback loops present in a battery formation and test system using the AD8450 or the AD8451 analog front end and controller. The note presents models for linear regulators and buck/boost power converters, a step-by-step design procedure, and two specific design examples. While the design procedure described in this document always results in a stable system, the optimum solution is not guaranteed. Further optimization of the suggested designs can improve the response of the feedback loops.