AN-1582
APPLICATION NOTE

One Technology Way • P.O. Box 9106 • Norwood, MA 02062-9106, U.S.A. • Tel: 781.329.4700 • Fax: 781.461.3113 • www.analog.com

Automated Calibration Technique That Reduces the AD5360 16-Channel, 16-Bit DAC Offset Voltage to Less Than 1 mV

CIRCUIT FUNCTION AND BENEFITS

The circuit described in this application note and shown in Figure 1 provides a method of calibrating that removes an unknown offset error. When using high precision, high resolution digital-to-analog converters (DACs) in industrial process control and instrumentation applications, low offset is often a critical specification. This circuit uses built-in features of the AD5360 in conjunction with an external comparator and an operational amplifier to determine if the DAC output voltages are above or below a ground reference signal. With the amount of offset known, the user can adjust the codes sent to the DAC to null out the offset.

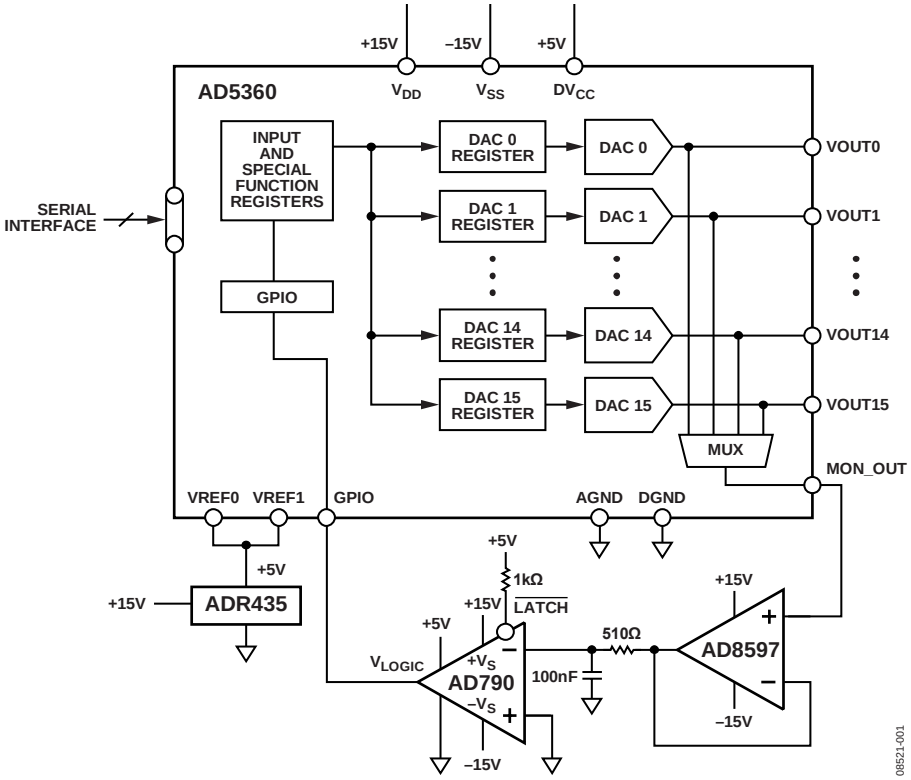

Figure 1. Autocalibration Circuit for AD5360 DAC That Reduces the Offset Voltage to Less Than 1 mV (Simplified Schematic: Decoupling and All Connections Not Shown), with the ADR435, AD790, and AD8597

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REVISION HISTORY

9/2018—Rev. 0 to Rev. A

Document Title Changed From CN0123 to AN-1582..Universal
Deleted Data Sheets and Evaluation Boards Section 2
Moved Revision History Section 2
Moved Circuit Description Section 3
Changes to Circuit Description Section 3
Changed Learn More Section to References Section 3
Moved Common Variations Section 3

9/2009—Revision 0: Initial Version

CIRCUIT DESCRIPTION

The AD5360 is a 16-channel, 16-bit DAC. The nominal output range is ±10 V when used with a +5 V reference. The AD5360 contains two offset DACs. Each offset DAC is connected to a group of eight DACs and is used to adjust the midscale point of the output span. For example, the offset DAC can be programmed to change the output span from ±10 V to −8 V to +12 V, or to other values as required by the application.

The AD5360 is factory trimmed to have a very low offset. The trimming is done with the offset DAC at its default value, and the offset error due to the offset DAC is effectively removed. When the value of the offset DAC is changed from its default value, however, its offset error affects the offset error of the main DACs.

The circuit described in this application note allows for the offset error of the main DACs to be measured and calibrated out under those conditions. The circuit relies on a general-purpose input/output (GPIO) pin and an analog multiplexer. The GPIO pin is set as an input, and by reading the GPIO internal register, the logic status of the GPIO pin is determined. The analog multiplexer is programmable to connect any of the 16 DAC outputs to a single MON_OUT pin. The multiplexer switches have a low but finite on resistance (R_{ON}) so that any current drawn from MON_OUT creates a voltage drop across R_{ON} and, therefore, an output error. To prevent this, MON_OUT is buffered by an AD8597 low noise amplifier. The low-pass filter following the amplifier reduces the amount of noise seen by the AD790 high speed precision comparator and prevents false triggering.

The AD790 can be operated on ±15 V supplies, making it compatible with the AD5360. The AD790 also requires an additional +5 V logic voltage (V_{LOGIC}) supply when operating on ±15 V supplies. In addition, the AD790 has a 15 V maximum differential input voltage. Therefore, the AD790 can tolerate the output voltages from the AD5360 without attenuation. In Figure 1, the comparator output is low if the channel offset is positive, indicating that the output voltage must be reduced to remove the offset. The comparator output is high if the channel offset is negative, indicating that the output voltage must be increased to remove the offset.

To calibrate a DAC, the DAC channel is loaded with the digital value, which ideally provides a voltage equal to SIGGNDx, which is equal to 0 V. In this example, the DAC channel is assumed to have a negative offset. Reading the GPIO register shows that the comparator output is low, indicating that the input must be incremented until the output toggles high. As progressively higher codes are written to the DAC input register, the GPIO register is read until the comparator trips to the high state. The AD790 has a maximum hysteresis band of 0.65 mV. Therefore, reducing the DAC code again allows a more accurate determination of the DAC offset.

When the comparator output trips back to the low state, SIGGNDx is somewhere between those two codes. Due to the errors of the components used in the circuit, there is typically a span of three or four codes between comparator trip points. There is no way to determine exactly which code gives the lowest offset output using this method, but by picking a code that is the average of the two trip point codes, the DAC channel offset is typically less than 1 mV from SIGGNDx.

Excellent layout, grounding, and decoupling techniques must be used to achieve the desired performance from the circuits discussed in this note (see MT-031 Tutorial and MT-101 Tutorial). It is recommended to use a 4-layer PCB at minimum, with one ground plane layer, one power plane layer, and two signal layers.

Use the EVAL-AD5360EBZ as a reference for how to properly layout the design.

COMMON VARIATIONS

The AD5362 is an 8-channel version of the AD5360. The AD5361 and AD5363 are 14-bit versions of the AD5360 and AD5362, respectively. The AD8599 is a dual version of the AD8597.

The circuit described in this application note can be used with the AD5360, AD5361, AD5362, and the AD5363 devices mentioned in the previous paragraph. The reference can also be changed to give different output ranges if required.

REFERENCES

MT-031 Tutorial, *Grounding Data Converters and Solving the Mystery of "AGND" and "DGND,"* Analog Devices.

MT-083 Tutorial, *Comparators*, Analog Devices.

MT-101 Tutorial, *Decoupling Techniques*, Analog Devices.

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