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## Evaluating the AD9148 Quad 16-Bit,1 GSPS DAC TxDAC+® Digital-to-Analog Converter

### **FEATURES**

Full featured evaluation board for the AD9148 Access to four DAC outputs (AD9148-EBZ) Output of two modulators (AD9148-M5375-EBZ)

### **EQUIPMENT NEEDED**

AD9148-EBZ or AD9148-M5375-EBZ evaluation board 5 V dc power supply PC running Windows® with USB 2.0 ports EVAL-SDP-CH1Z (SDP-H1) or AD-DPG3 AD-DAC-FMC-ADP (ordered separately) Sinusoidal clock source (at least 1.2 GHz) Sinusoidal clock source (for modulator LO) Spectrum analyzer Mini-USB cable

### **DOCUMENTS NEEDED**

AD9148 data sheet

SOFTWARE NEEDED

**DAC Software Suite** 

### **GENERAL DESCRIPTION**

The AD9148-EBZ or the AD9148-M5375-EBZ connects to a digital pattern generator (DPG3) or a system demonstration platform (SDP-H1) to evaluate the AD9148 device. The AD9148-EBZ is a digital-to-analog converter (DAC) only evaluation board, and the AD9148-M5375-EBZ has two ADL5375 modulators on-board.

The DAC Software Suite includes the DPGDownloader and the serial peripheral interface (SPI) application to control the evaluation board SPI port. Via the SPI port, the device under test (DUT) and clock circuitry can be programmed into any of the various operating modes. To ease the subsystem evaluation, the AD9516-0 clock distribution chip and two ADL5375 modulators are designed into the AD9148-M5375-EBZ.

For full details, see the AD9148 data sheet, which must be used in conjunction with this user guide and the AD9148-EBZ or the AD9148-M5375-EBZ evaluation board.

## AD9148-EBZ/AD9148-M5375-EBZ User Guide

## **TABLE OF CONTENTS**

Features	1
Equipment Needed	1
Documents Needed	1
Software Needed	1
General Description	1
Revision History	2
Evaluation Board Photographs	3

Evaluation Board Hardware	5
Hardware Setup	5
Jumper Configurations	8
Evaluation Board Software Quick Start Procedures	9
Single-Tone TestING Setup	9

### **REVISION HISTORY**

2/2020—Revision 0: Initial Version

## **EVALUATION BOARD PHOTOGRAPHS**



Figure 1. AD9148-EBZ

## UG-1631

## AD9148-EBZ/AD9148-M5375-EBZ User Guide



Figure 2. AD9148-M5375-EBZ

# EVALUATION BOARD HARDWARE HARDWARE SETUP

Take the following steps to setup the evaluation board hardware:

- Connect a 5 V dc power supply to P5 and P6, the red and black banana jacks, on the AD9148-EBZ or the AD9148-M5375-EBZ board.
- 2. If using the SDP-H1, connect the P1 and P2 male connectors on the AD9148-EBZ or the AD9148-M5375-EBZ board to the AD-DAC-FMC-ADP female connectors on the SDP-H1.
- 3. Connect the provided USB cable from the PC to the USB connector on the SDP-H1.
- For the AD9148-EBZ, connect a coaxial cable from the spectrum analyzer to the J3 (OUT1), J8 (OUT2), J16 (OUT3), or J9 (OUT4) jumpers for the DAC1, DAC2, DAC3, or DAC4 output, respectively.

- 5. For the AD9148-M5375-EBZ, connect the spectrum analyzer to J3 (TX\_MOD OUT1) for the Transmitter Channel 1 output or to J4 (TX\_MOD OUT2) for the Transmitter Channel 2 output.
- 6. For the AD9148-EBZ, connect a coaxial cable from the signal generator to J1 (CLK\_IN).
- 7. For the AD9148-M5375-EBZ, connect a coaxial cable from the signal generator to J5 (LO\_IN).
- 8. If using the DPG3, connect the P1 and P2 male connectors on the AD9148-EBZ or the AD9148-M5375-EBZ board to the DPG3 female connectors.
- 9. Install the DAC Software Suite before connecting the USB cable to the PC.
- 10. Connect the USB cable to the mini USB, XP2 connector on the AD9148-EBZ or the AD9148-M5375-EBZ evaluation board.



Figure 3. Bench Setup

## UG-1631

## AD9148-EBZ/AD9148-M5375-EBZ User Guide



Figure 4. AD9148-EBZ to DPG3 Connection



Figure 5. SDP-H1 and AD9148 Bench Setup (Note that the FMC connector is the interface on the bottom of the AD-DAC-FMC-ADP.)

## AD9148-EBZ/AD9148-M5375-EBZ User Guide



Figure 6. SDP-H1, AD-DAC-FMC-ADP, and AD9148-EBZ Evaluation Board

### JUMPER CONFIGURATIONS

Six pin jumpers are on the AD9148-M5375-EBZ or the AD9148-EBZ.

These pin jumpers consist of two pins with a pin header shunt loaded on these two pins, creating a short circuit between the pins. When the pins are shorted, the on-board low dropout (LDO) regulators supply voltage for the particular power domain. When a shunt is removed, apply an external supply.

JP1 selects the supply voltage level for IOVDD. When Pin 1 and Pin 2 are connected, IOVDD = 3.3 V. When Pin 2 and Pin 3 are connected, IOVDD = 1.8 V. The default configuration for IOVDD = 3.3 V. The other five jumpers are detailed in Table 1. On the back of the AD9148-M5375-EBZ or the AD9148-EBZ, solder jumpers, JP15 and JP18, determine whether the reference and synchronization clock of the AD9148 is from the AD9516-0 or an external source through J2 (REF\_IN). When the AD9516-0 is used for the clock source, configure the jumpers so that the center pad connects to the inner pad. When an external source is used, connect the center pad to the outer pad.

For the AD9148-M5375-EBZ, a local oscillator (LO) signal is required to drive the ADL5375 modulators. The LO signal is fed through J5 (LO\_IN) and shared between the two ADL5375 modulators.

### Table 1. Jumper Connections

Power Supply	If Jx Not Connected	Apply External Supply Voltage to TPx (Red)	Ground for the Supply to TPx (Black)
IOVDD	JP12	TP5	TP6
DVDD18	JP3	TP3	TP4
XCVDD33	JP9	TP9	TP10
CVDD18	JP2	TP1	TP2
AVDD33	JP8	TP7	TP8
VDDM <sup>1</sup>	JP4	TP12	TP16

<sup>1</sup> The VDDM power supply is present on the AD9148-M5375-EBZ board only to supply power to the modulators.

Take the following steps to run a single-tone test:

- 1. Ensure that the DAC Software Suite, which includes the SPI software (SPI application), is installed on the PC.
- Open the SPI software from Start > Programs > Analog Devices < 9148 > AD9148 SPI.
- 3. Select **2x** from the **Interpolation** dropdown menu in the **Data** tab (see Figure 7).



Figure 7. SPI Interface

- 4. Click the run arrow in the top left corner of the window to set the device to 2× interpolation mode.
- Open the DPGDownloader software from Start > Programs > Analog Devices > DPG > DPGDownloader.
- Within the DPGDownloader software, select Single Tone from the Add Generated Waveform dropdown menu (see Figure 9).
- 7. Set the Data Rate to 100.000 MHz (see Figure 9).
- 8. Set the Desired Frequency to 21.000 MHz (see Figure 9).
- 9. Clear the **Unsigned Data** check box (see Figure 9).

- Check off the Generate Complex Data (I & Q) check box (see Figure 9).
- Select a value for the generated I waveform in the Data Vector 1 box and the Data Vector 3 box (see Figure 9).
- Select a value for the generated Q waveform in the Data Vector 2 box and Data Vector 4 box (see Figure 9).
- Click the Download button ( ) in the lower right of the Data Playback section (see Figure 9).
- Click the Play button (<sup>N</sup>) to begin vector playback (see Figure 9). The signal frequency output then appears on the spectrum analyzer as shown in Figure 8.



Figure 8. Signal Frequency Output on the Spectrum Analyzer

DPGDownloader		
File Help		
🚰 Add Data File 🔹 🐷 Add Generated Waveform 👻 🗙 Remove Selected 📮 Remove All 🛛	Graph Selec	ted Vectors
Data Rate: 100.000 MHz + DAC Resolution: 16+ bits Record Length: 16384 + Offset: 0+		Sing
Desired Frequency: 21.000 MHz + Amplitude: 0.0 + dB (Full Scale) Relative Phase: 0.0 + or		gle T
Calculated Frequency: 21.002 MHz Cycles: 3441 🗌 Unsigned Data 🔲 Allow even cycle count 📝 Generate Complex Data (1 & Q)		one
SDP-H1 Unit 1		
Evaluation Board: AD9148   Data Playback		
Port Configuration: LVDS Data Vector 1: @11: Single Tone - 21.002 MHz; 0.0 dB; 0.0* (In-Phase)		•
Data Vector 2: 2102 Single Tone - 21.002 MHz; 0.0 dB; 0.0" (Quadrature)		•
Configuration Version: FPGA Image Loaded Data Vector 3: 🥥 11: Single Tone - 21.002 MHz: 0.0 dB; 0.0* (In-Phase)		•
Data Vector 4: 🧭 10: Single Tone - 21.002 MHz: 0.0 dB; 0.0° (Quadrature)		•
Interface Mode:		
Statt Offset		
V Hide disconnected Evaluation Boards Progress		
Advanced/Debug		
[Π]		

Figure 9. DPGDownloader Rev. 0 | Page 9 of 10

## UG-1631

## NOTES



### ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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Rev. 0 | Page 10 of 10