ANALOG DEVICES

AN-803
APPLICATION NOTE

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Pin-Compatible High Speed ADCs Simplify Design Tasks

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INTRODUCTION

Choosing an A/D converter can be the toughest choice a system designer makes. The converter's resolution and sampling rate determine the system's performance. Yet, often the design is based on a series of assumptions that can't be verified until the prototype system is put through its paces.

Depending on results, the system may be overspecified and a lower speed or resolution converter would work or be underdesigned, so a faster or higher resolution converter is needed. In the former case, there is an opportunity for cost reduction through a cheaper converter. In the latter case, major design changes increase time to market and increase development cost.

In addition, any change in a working design also introduces risk—the risk of "improving" a working design into a nonworking design. And the best way to minimize risk is to future-proof the design by using a single layout and converters that are pin compatible.

To that end, ADI has developed a family of A/D converters based on a common A/D core to allow the designer to increase or decrease sampling speeds and resolution without changing a PC board's layout.

FAMILY DESCRIPTION

The A/D converters come in single and dual versions. Each version shares a common package, pinout, and footprint. These allow the designer to change converter resolutions or sampling speeds or both during prototype and field testing if more or less performance is needed.

The converters (Table I) are available in 10-, 12-, and 14-bit pin-compatible versions at speeds from 20 MSPS to 105 MSPS. All are built around a common core in a CMOS process.

The converter core (Figure 1) consists of a sample-and-hold amplifier (SHA), followed by a multistage differential pipelined architecture with output error correction logic and an integrated voltage reference. The converter family provides from 10 to 14 bits of resolution at speeds ranging from 20 MSPS to 105 MSPS with no missing codes over the full operating temperature range.

Table I. Single and Dual A/D Converters

Bits	Single ADCs (32-Lead LFCSP)	Speeds (MSPS)	Dual ADCs (64-Lead LFCSP)	Speeds (MSPS)
10	AD9215	65, 80, 105	AD9216	65, 80, 105
12	AD9235	20, 40, 65	AD9238	20, 40, 65
12	AD9236	80		
12	AD9237	20, 40, 65		
14	AD9245	20, 40, 65, 80	AD9248	20, 40, 65

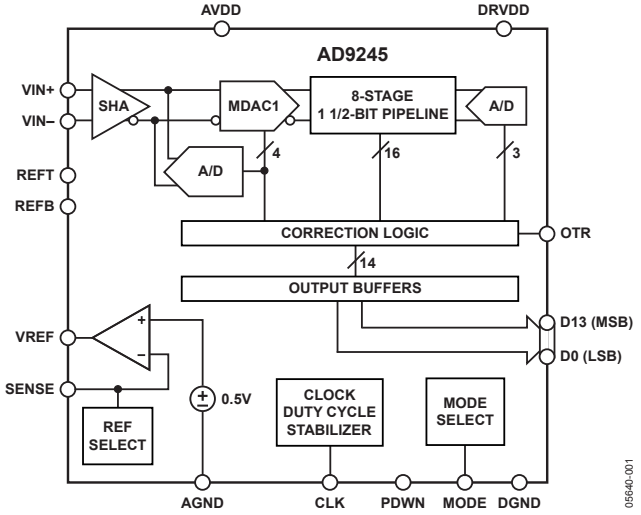

Figure 1. ADC Family Functional Block Diagram

The wide bandwidth, differential input SHA allows a variety of user-selectable input ranges and common-mode voltages, including single-ended applications. It suits both multiplexed applications that switch full-scale voltage levels in successive channels, and single-channel applications that undersample signals at frequencies well beyond the Nyquist rate.

A single-ended clock input controls all internal conversion cycles. A duty cycle stabilizer (DCS) compensates for wide variations in the clock duty cycle while maintaining excellent overall ADC performance. The digital output data is presented in straight binary or twos complement formats. An out-of-range (OTR) signal indicates an overflow condition that can be used with the most significant bit to determine low or high overflow.

Fabricated on an advanced CMOS process, each single ADC is available in a 32-lead LFCSP and is specified over the industrial temperature range (–40°C to +85°C).

DESIGN AND LAYOUT CONSIDERATIONS

For the layout designer, the only difference between the pinouts is in the assignment of the data out bits.

In all single converters, Pin 20 is the MSB, with the countdown towards the LSB proceeding clockwise around the package.

In all dual converters, Pin 57 and Pin 38 are the "A" and "B" MSBs, respectively, with the countdown towards the A and B LSBs proceeding clockwise around the package. Figures 3, 4, and 5 show pin diagrams and package outlines; Table II and Table III list pin function descriptions for the converters.

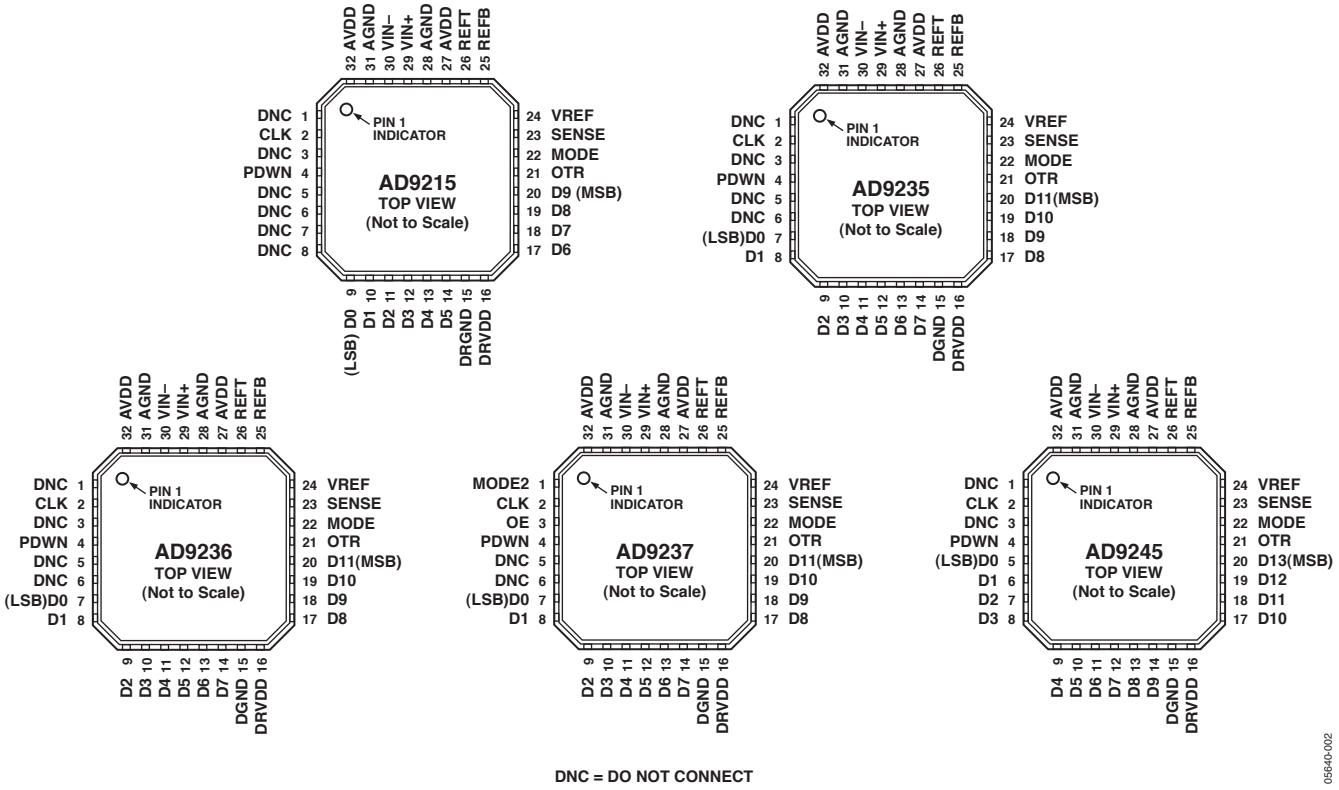

Figure 2. Pin Diagrams for the AD9215, AD9235, AD9236, AD9237, and AD9245 in a 32-Lead LFCSP

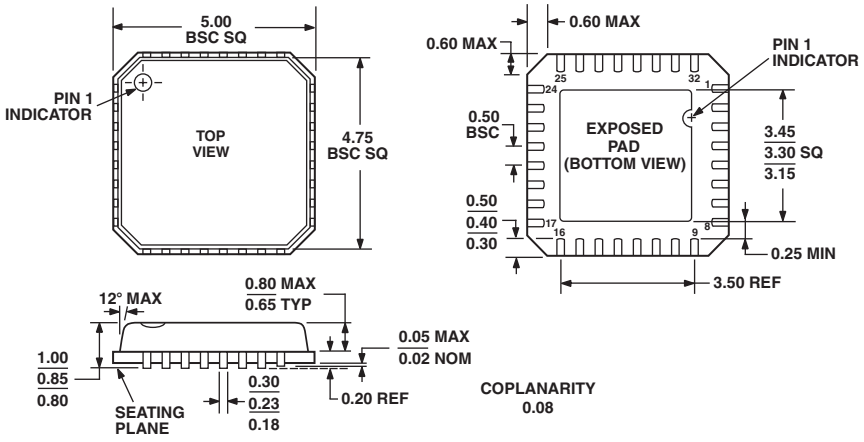

Figure 3. 32-Lead Lead Frame Chip Scale Package, Very Thin Quad (LFCSP_VQ)
(CP-32-3)
Dimensions shown in millimeters

Table II. Pin Function Descriptions for the AD9215, AD9235, AD9236, AD9237, and AD9245 Single ADCs in a 32-Lead LFCSP

Pin No.	AD9215 10-Bit ADC Pin Functions	AD9235, AD9236, AD9237 12-Bit ADC Pin Functions	AD9245 14-Bit ADC Pin Functions
1	DNC (Do Not Connect)	DNC (AD9237: MODE2)	DNC
2	CLK	CLK	CLK
3	DNC	DNC (AD9237: OE)	DNC
4	PDWN	PDWN	PDWN
5	DNC	DNC	D0 (LSB)
6	DNC	DNC	D1
7	DNC	D0 (LSB)	D2
8	DNC	D1	D3
9	D0 (LSB)	D2	D4
10	D1	D3	D5
11	D2	D4	D6
12	D3	D5	D7
13	D4	D6	D8
14	D5	D7	D9
15	DGND (Digital Output Ground)	DGND	DGND
16	DRVDD (Digital Output VDD)	DRVDD	DRVDD
17	D6	D8	D10
18	D7	D9	D11
19	D8	D10	D12
20	D9 (MSB)	D11 (MSB)	D13 (MSB)
21	OTR (Out-of-Range Indicator)	OTR	OTR
22	MODE (Data Format Select and DCS Mode Selection)	MODE	MODE
23	SENSE (Reference Mode Selection, see Data Sheet)	SENSE	SENSE
24	VREF (Voltage Reference Input/Output)	VREF	VREF
25	REFB (Differential Reference (–))	REFB	REFB
26	REFT (Differential Reference (+))	REFT	REFT
27	AVDD (Analog Power Supply)	AVDD	AVDD
28	AGND (Analog Ground)	AGND	AGND
29	VIN+ (Analog Input Pin (+))	VIN+	VIN+
30	VIN– (Analog Input Pin (–))	VIN–	VIN–
31	AGND (Analog Ground)	AGND	AGND
32	AVDD (Analog Power Supply)	AVDD	AVDD

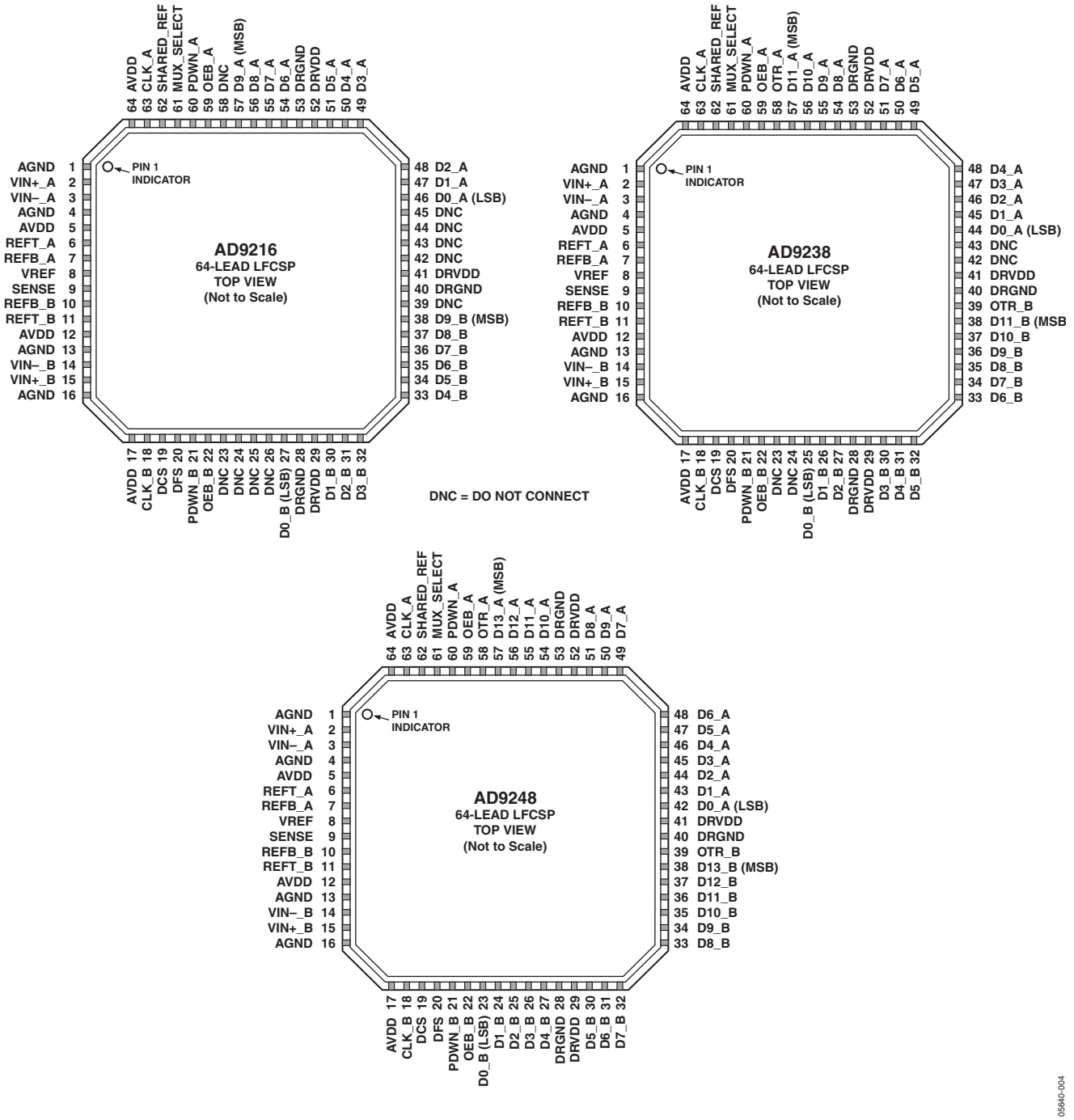

Figure 4. Pin Diagrams for the AD9216, AD9238, and AD9248 in an LFCSP-48

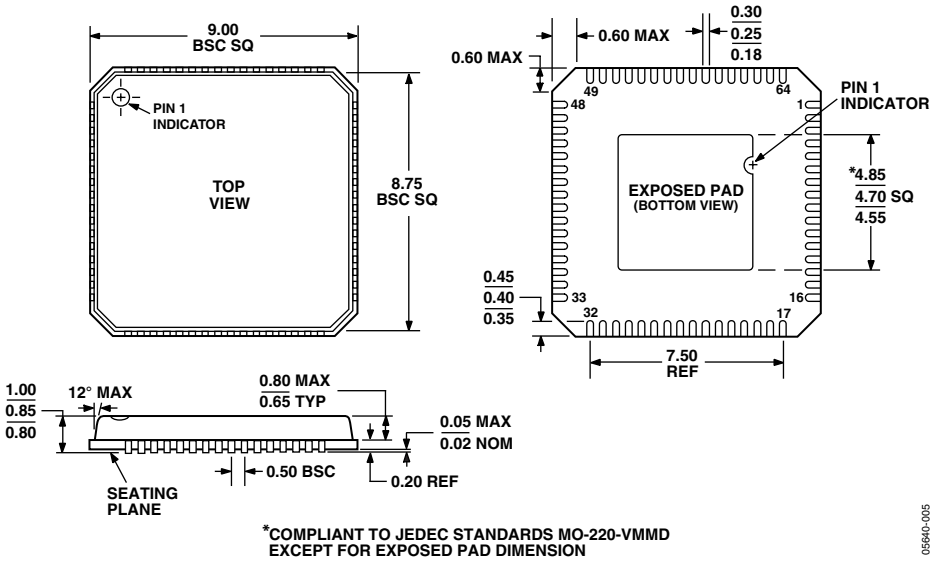

Figure 5. 64-Lead Lead Frame Chip Scale Package, Very Thin Quad (LFCSP_VQ) (CP-64-1)
Dimensions shown in millimeters

Table III. Pin Function Descriptions for the AD9216, AD9238, and AD9248 Dual ADCs in a 64-Lead LFCSP

Pin No.	AD9216 10-Bit ADC Pin Functions	AD9238 12-Bit ADC Pin Functions	AD9248 14-Bit ADC Pin Functions
1	AGND (Analog Ground)	AGND	AGND
2	VIN+_A (Analog Input Pin (+) for Channel A)	VIN+_A	VIN+_A
3	VIN–_A (Analog Input Pin (–) for Channel A)	VIN–_A	VIN–_A
4	AGND (Analog Ground)	AGND	AGND
5	AVDD (Analog Power Supply)	AVDD	AVDD
6	REFT_A (Differential Reference (+) for Channel A)	REFT_A	REFT_A
7	REFB_A (Differential Reference (–) for Channel A)	REFB_A	REFB_A
8	VREF (Voltage Reference Input/Output)	VREF	VREF
9	SENSE Reference Mode Selection (see Data Sheet)	SENSE	SENSE
10	REFB_B (Differential Reference (–) for Channel B)	REFB_B	REFB_B
11	REFT_B (Differential Reference (+) for Channel B)	REFT_B	REFT_B
12	AVDD (Analog Power Supply)	AVDD	AVDD
13	AGND (Analog Ground)	AGND	AGND
14	VIN–_B (Analog Input Pin (–) for Channel B)	VIN–_B	VIN–_B
15	VIN+_B (Analog Input Pin (+) for Channel B)	VIN+_B	VIN+_B
16	AGND (Analog Ground)	AGND	AGND
17	AVDD (Analog Power Supply)	AVDD	AVDD
18	CLK_B (Clock Input Pin for Channel B)	CLK_B	CLK_B
19	DCS (Duty Cycle Stabilizer Mode Pin—Active High)	DCS	DCS
20	DFS (Data Output Format Pin (Low for Offset Binary, High for Twos Complement)	DFS	DFS
21	PDWN_B (Power Down for Channel B—Active High)	PDWN_B	PDWN_B
22	OEB_B (Output Enable for Channel B—Low Enables Channel B Data Bus, High Sets Outputs at High Impedance)	OEB_B	OEB_B
23	DNC (Do Not Connect)	DNC	D0_B (LSB)
24	DNC (Do Not Connect)	DNC	D1_B
25	DNC (Do Not Connect)	D0_B (LSB)	D2_B
26	DNC (Do Not Connect)	D1_B	D3_B
27	D0_B (LSB)	D2_B	D4_B
28	DRGND (Digital Output Ground)	DRGND	DRGND
29	DRVDD (Digital Output VDD)	DRVDD	DRVDD
30	D1_B	D3_B	D5_B
31	D2_B	D4_B	D6_B
32	D3_B	D5_B	D7_B
33	D4_B	D6_B	D8_B
34	D5_B	D7_B	D9_B
35	D6_B	D8_B	D10_B
36	D7_B	D9_B	D11_B
37	D8_B	D10_B	D12_B

Pin No.	AD9216 10-Bit ADC Pin Functions	AD9238 12-Bit ADC Pin Functions	AD9248 14-Bit ADC Pin Functions
38	D9_B (MSB)	D11_B (MSB)	D13_B (MSB)
39	OTR_B (Out-of-Range Indicator for Channel B)	OTR_B	OTR_B
40	DRGND (Digital Output Ground)	DGND	DGND
41	DRVDD (Digital Output VDD)	DRVDD	DRVDD
42	DNC (Do Not Connect)	DNC	D0_A (LSB)
43	DNC (Do Not Connect)	DNC	D1_A
44	DNC (Do Not Connect)	D0_A (LSB)	D2_A
45	DNC (Do Not Connect)	D1_A	D3_A
46	D0_A (LSB)	D2_A	D4_A
47	D1_A	D3_A	D5_A
48	D2_A	D4_A	D6_A
49	D3_A	D5_A	D7_A
50	D4_A	D6_A	D8_A
51	D5_A	D7_A	D9_A
52	DRVDD (Digital Output VDD)	DRVDD	DRVDD
53	DRGND (Digital Output Ground)	DGND	DGND
54	D6_A	D8_A	D10_A
55	D7_A	D9_A	D11_A
56	D8_A	D10_A	D12_A
57	D9_A (MSB)	D11_A (MSB)	D13_A (MSB)
58	OTR_A (Out-of-Range Indicator for Channel A)	OTR_A	OTR_A
59	OEB_A (Output Enable for Channel A—Low Enables Channel A Data Bus, High Sets Outputs at High Impedance)	OEB_A	OEB_A
60	PDWN_A (Power Down for Channel A—Active High)	PDWN_A	PDWN_A
61	MUX_SELECT (Data Multiplexed Mode)	MUX_SELECT	MUX_SELECT
62	SHARED_REF (Low = Independent, High = Shared)	SHARED_REF	SHARED_REF
63	CLK_A (Clock Input for Channel A)	CLK_A	CLK_A
64	AVDD (Analog Power Supply)	AVDD	AVDD

LAYOUT FOR 10, 12, OR 14 BITS

For the circuit designer, the only difference in designing with the different pinouts is to account for the unused data out bits, which means adding optional terminations to the pins assigned to Bits 11 through 14, that is, the least significant bits.

It's assumed that the ADC's output drives either a DSP or FPGA and that the user will design the circuit and layout to accommodate resolutions of 10, 12, or 14 bits.

The general technique is to have a resistor in series with the ADC's output to terminate the PCB trace and a nominal 10 kΩ resistor to ground or VDD at the input of the DSP or FPGA. The resistor configuration will depend on the manufacturer's recommendations for the FPGA or DSP that's used.

Either resistor can be populated (or not) depending on whether the bit is used (or not). Figure 6 shows a design example.

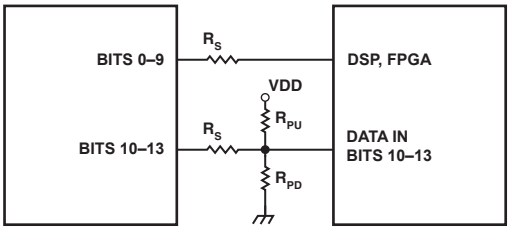

Figure 6. Flexible Design for Pin-Compatible Converters

Either R_{PU} or R_{PD} is used if a termination resistor is required for unused bits. Some devices terminate unused bits internally and do not require external termination resistors. The most flexible design for the pin-compatible converters is to layout the PC board with a series termination resistor followed by pads for both pull-up (R_{PU}) and pull-down (R_{PD}) resistors. Depending on the DSP or FPGA, only one of R_{PU} or R_{PD} will be used if an external termination is required, or neither when the termination is internal.

PCB DESIGN GUIDELINES FOR CHIP SCALE PACKAGES

The lands on the chip scale package (CP-32 and CP-64) are rectangular. The printed circuit board pad for these should be 0.1 mm longer than the package land length, and 0.05 mm wider than the package land width. The land should be centered on the pad to ensure that the solder joint size is maximized. The bottom of the chip scale package has a central thermal pad. The thermal pad on the printed circuit board should be at least as large as this exposed pad.

On the printed circuit board, there should be a clearance of at least 0.25 mm between the thermal pad and the inner edges of the pad pattern. This will ensure that shorting is avoided. Thermal vias may be used on the printed circuit board thermal pad to improve the thermal performance of the package.

If vias are used, they should be incorporated in the thermal pad at 1.2 mm pitch grid. The via's diameter should be between 0.3 mm and 0.33 mm and the via barrel should be plated with 1 oz. copper to plug the via. The user should connect the printed circuit board's thermal pad to AGND.

CONCLUSION

This application note explains the common pinout and footprints of single and dual high speed ADCs and how a designer can take advantage of their pin compatibility. It lists the pin functions for the converters and shows the differences in the data out bits so a user is able to design a single board that can accommodate different resolutions and speeds to changing the converter's speed or resolution without changing a layout, thus saving time to market.

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