

Devices Connected/Referenced

ADA4930-1/ ADA4930-2	Ultralow Noise Single/Dual Drivers for Low Voltage ADCs
AD9265	16-Bit, 125 MSPS/105 MSPS/80 MSPS, 1.8 V Analog-to-Digital Converter

Single-Supply DC-Coupled 16-Bit, 125 MSPS Analog Front End for Bipolar Input Signals

EVALUATION AND DESIGN SUPPORT

Design and Integration Files

[Schematics](#), [Layout Files](#), [Bill of Materials](#)

CIRCUIT FUNCTION AND BENEFITS

The circuit shown in Figure 1 solves a problem often encountered in dc-coupled, single-supply systems when interfacing bipolar input signals to differential input, low voltage analog-to-digital converters (ADCs). The technique ensures the proper common-mode voltage level at the input to the differential drive amplifier by controlling the input common-mode level using two level shifting resistors. The output common-mode voltage is established independently by applying the correct voltage to the V_{OCM} pin of the ADA4930-1 differential driver.

This flexible arrangement allows the ADA4930-1 differential driver to operate on a single 3.3 V supply, while the AD9265 16-bit 125 MSPS ADC operates on a 1.8 V supply, thereby minimizing the total circuit power dissipation.

In broadband applications, the frequency range of interest often includes dc. To maximize the dynamic range of a differential input ADC, typical input signals can be relatively large, thereby requiring the differential driver to operate at lower gain settings. Under these conditions, the input common-mode voltage of the differential driver must stay within the specified range.

Independent control of the input and output common-mode voltage of differential amplifiers is often required in direct coupled single-supply applications such as processing demodulator outputs with high input common-mode voltages, x-ray applications with a dc component added to a differential component, and other places where the differential driver must handle low value input common-mode voltages. Low input common-mode voltage applications can include either single-ended or differential inputs, with zero, bipolar, or negative inputs.

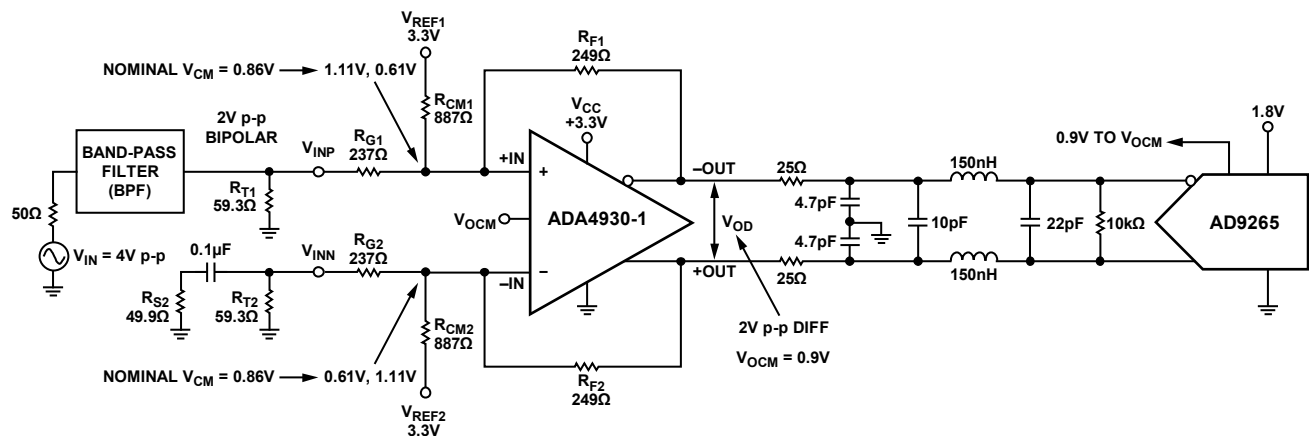


Figure 1. High Speed, Single-Ended to Differential ADC Driver (Simplified Schematic: All Connections and Decoupling Not Shown)

Rev. A

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CIRCUIT DESCRIPTION

Modern high speed ADCs are normally driven by differential amplifiers for best performance. Typical differential drivers give best ac performance when operating at gains of two or less, and in single-supply applications, full-scale input signals frequently exceed the input common-mode voltage range of the ADC driver.

To avoid common-mode voltage problems with differential amplifiers, the circuit must be carefully analyzed. The design equations and analysis for the [ADA4930-1](#) differential driver are contained in its data sheet; however, the Analog Devices, Inc., Differential Amplifier Calculator ([DiffAmpCalc™](#) design tool) allows complete analysis of the circuit by applying nodal analysis and presents the results in graphical format.

The circuit in Figure 1 uses the [ADA4930-1](#) because of its ability to operate on a 3.3 V single supply with an output common-mode voltage (V_{OCM}) of 0.9 V, the common-mode level best suited for 1.8 V ADCs, such as the [AD9265](#).

To optimize noise performance and minimize its negative impact on the signal-to-noise-and-distortion ratio (SINAD), an R_{EX} value of 249 Ω was selected. The values for the R_{GX} and R_{TX} were then determined using the [DiffAmpCalc](#) design tool set for a gain of 0.511 measured from V_{IN} to the differential output voltage (V_{OD}).

The input signal of Figure 1 comes from a 50 Ω RF source and drives the band-pass filter. To keep the differential amplifier source impedances balanced, an ac coupling capacitor of 0.1 μF in series with a 49.9 Ω resistor is connected to the unused input, as shown in Figure 1. The impedance of this capacitor is low enough to act as an ac short circuit for a 70 MHz center frequency signal.

The input common-mode range for the [ADA4930-1](#) operating on a single 3.3 V supply is 0.3 V to 1.2 V. The two input common-mode resistors, R_{CM1} and R_{CM2} , connect between the differential amplifier input pins and the reference voltages, V_{REF1} and V_{REF2} , ensure that the input common-mode voltage does not go below 0.3 V for full-scale bipolar input signals.

Without the common-mode bias resistors, the input common-mode voltage of the [ADA4930-1](#) goes below 0.3 V, and clipping occurs for a full-scale signal.

For convenience, V_{REF1} and V_{REF2} are each connected to V_{CC} , the 3.3 V single supply. The connection to 3.3 V raises the nominal input common-mode voltage to accommodate the negative input signal swing. The technique for calculating the values for the common-mode resistors is described in the [ADA4930-1](#) data sheet.

It is common practice to include small valued snubber resistors in series with the outputs of the differential amplifier. This practice minimizes high frequency peaking and isolates the amplifier output from the capacitance of the filter. In the Figure 1 circuit, these resistor values are 25 Ω .

The three-pole Butterworth low-pass filter helps to roll off second-order and third-order harmonics and reduces noise at the ADC input. An odd-order filter was selected so that the final filter capacitor is in parallel with the input capacitance of the [AD9265](#).

The Butterworth filter was designed for a cutoff frequency of 100 MHz, an input impedance of 50 Ω , and an output impedance of 1 k Ω . Filter components were rounded to standard values and further optimized for best system performance.

The 10 k Ω resistor in parallel with the ADC input was chosen to be as large as possible to minimize attenuation drops in the signal path. The proximity of the [ADA4930-1](#) to the [AD9265](#) minimizes transmission line effects at 70 MHz. Therefore, traditional double termination methods between the driver output and the ADC input were not implemented.

When driving the [AD9265](#), care was taken to not overdrive the input of the ADC. The maximum output of the [ADA4930-1](#) operating on a 3.3 V supply is 1.74 V, which is within the maximum input voltage specification of the [AD9265](#).

Common-Mode Voltage Analysis

The basic starting point of the design is shown in Figure 2 after inputting the appropriate values into the [DiffAmpCalc](#) tool. Note that the input signal is 1.4 V p-p, resulting in signals at the +IN and -IN inputs that go as low as 0.305 V. Larger signals cause clipping, as is shown in Figure 3.

One solution to the problem is to add a negative supply; however, the maximum supply voltage of 5.5 V cannot be exceeded, which prevents the use of ± 3.3 V supplies. Although a +3.3 V, -1 V dual supply system works, this is inconvenient and adds power.

The addition of the two R_{CMx} resistors, as shown in Figure 1, is the ideal solution and raises the nominal common-mode voltage on the [ADA4930-1](#) from 0.489 V to 0.860 V using 887 Ω resistors. The maximum negative and positive swings at the +IN and -IN inputs are now 0.61 V and 1.11 V, respectively, which are within the allowable range of 0.3 V to 1.2 V.

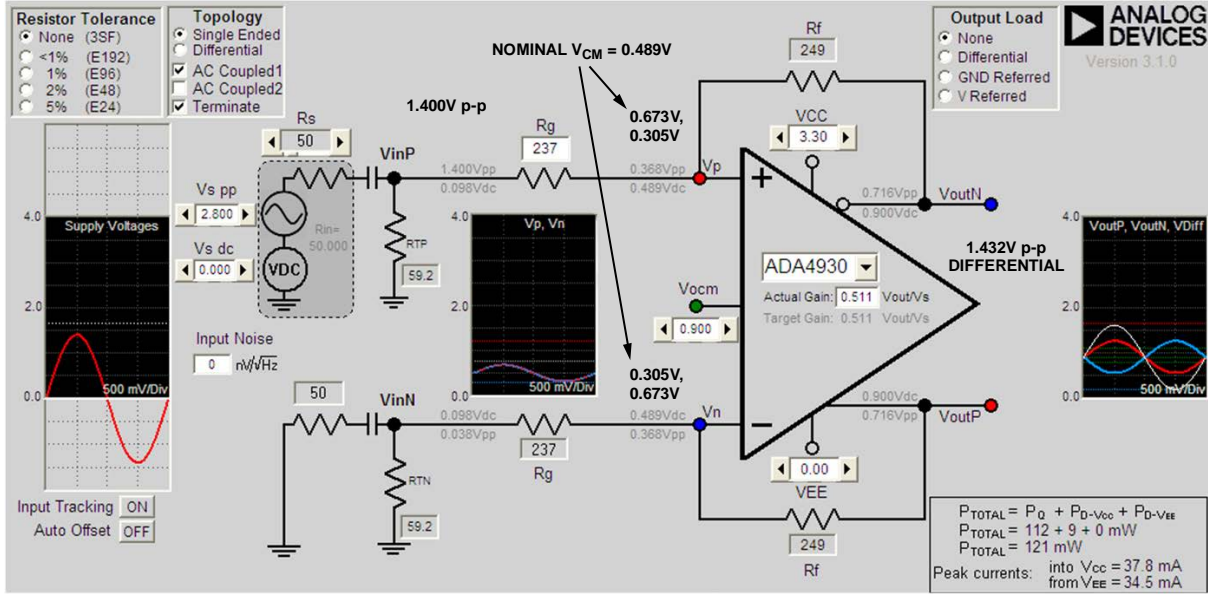


Figure 2. DiffAmpCalc Design Analysis for Low Level Input Signal, Single 3.3 V Supply, $V_{OCM} = 0.9 V$

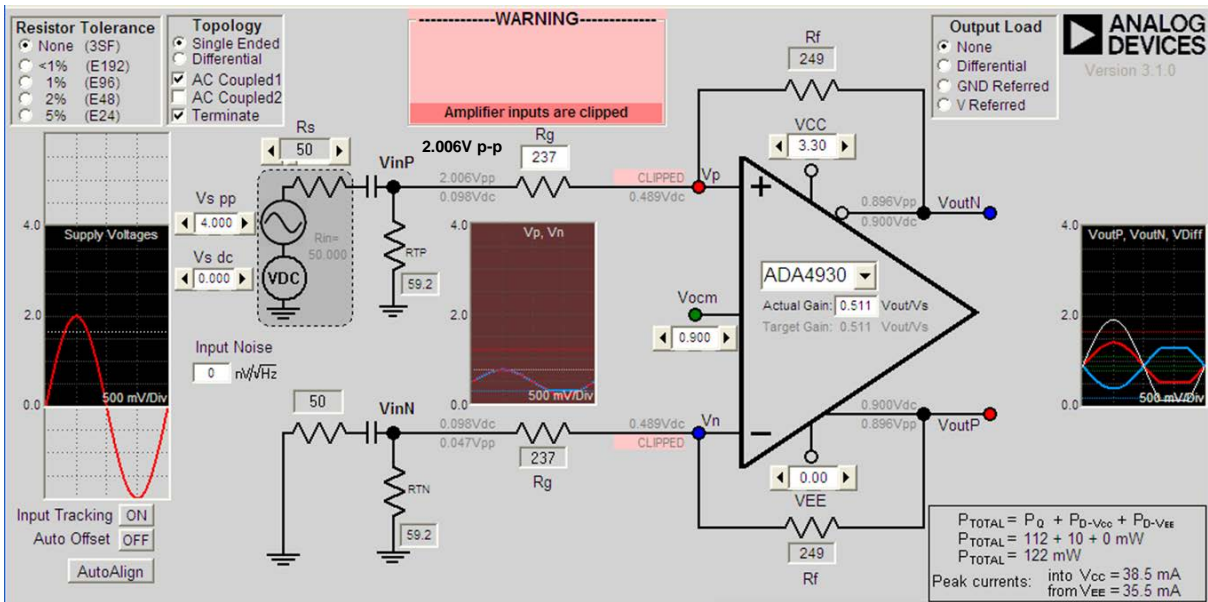


Figure 3. DiffAmpCalc Design Analysis for Full-Scale Input Signal, 3.3 V Supply, $V_{OCM} = 0.9 V$, Showing the Effects of Clipping

Circuit Performance

Figure 4 shows the performance of the AD9265 evaluation board directly coupled to an external band-pass filter with a 70 MHz center frequency and a sampling rate of 125 MSPS. The standard AD9265 evaluation board configuration converts the signal from single-ended to differential with an RF balun.

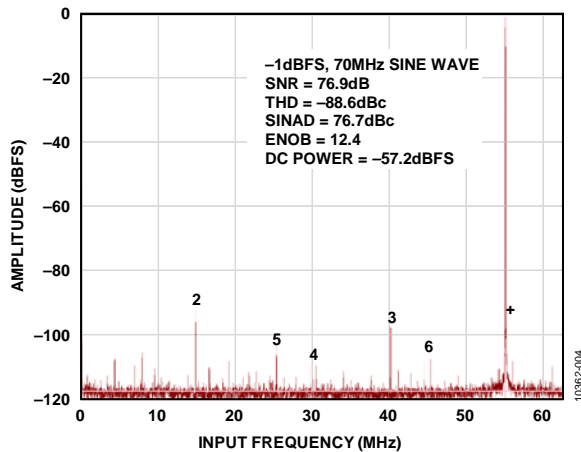


Figure 4. VisualAnalog FFT of the AD9265 Driven with Balun

Figure 5 shows the Figure 1 single-supply design using the AD9265 and the ADA4930-1 without the 887 Ω bias resistors. The effects of clipping are evident. The DiffAmpCalc analysis also shows this clipping (see Figure 3).

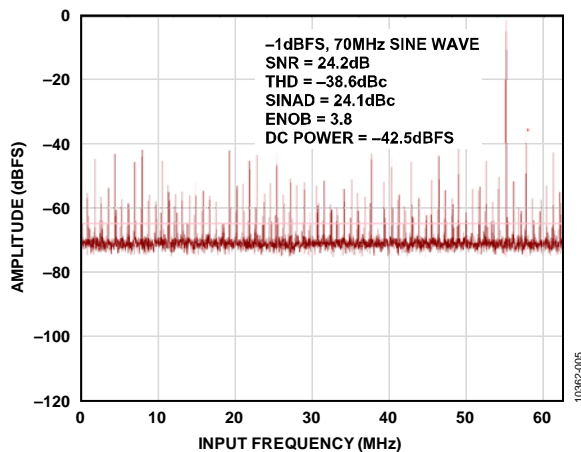


Figure 5. VisualAnalog FFT of the ADA4930-1 and AD9265 with R_{CM1} and R_{CM2} Removed Shows Effects of Clipping

Figure 6 shows the performance of the ADA4930-1 operating on a 3.3 V single supply, with the input common-mode resistors, R_{CM1} and R_{CM2}, connected. Additionally, the balun and the RC filter on the AD9265 evaluation board were removed and replaced with a three-pole Butterworth filter, as shown in Figure 1.

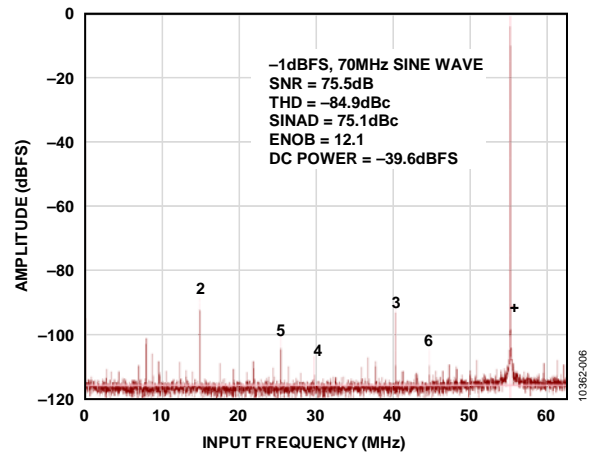


Figure 6. VisualAnalog FFT of the ADA4930-1 and AD9265 with R_{CM1} and R_{CM2} as shown in Figure 1

Using effective number of bits (ENOB), SINAD, and signal-to-noise ratio (SNR) as figure of merits, Table 1 compares the results from Figure 4, Figure 5, and Figure 6.

Table 1. Summary of ENOB, SINAD, and SNR Results

Figure of Merit	Baseline (See Figure 4)	No R _{CM} Resistors (See Figure 5)	R _{CM} Resistors (See Figure 6)
ENOB	12.4	3.8	12.1
SINAD (dBc)	76.7	24.1	75.1
SNR (dB)	76.9	24.2	75.5

The inclusion of input common-mode resistors with the primary function of independently shifting the input common-mode level minimally affects performance, as shown in Table 1. For example, ENOB is 12.4 before the inclusion of the R_{CM} resistors and 12.1 with the R_{CM} resistors. The slight reduction of ENOB can be attributed to the small increase of the noise floor due to the 4.7 nV/√Hz output noise density of the ADA4930-1 in the configuration shown in Figure 1. This value was calculated using the DiffAmpCalc tool. Therefore, the input and output common-mode levels of an ADC driver can be controlled independently with the addition of two resistors, R_{CM1} and R_{CM2}, while maintaining excellent ENOB, SINAD, and SNR performance.

COMMON VARIATIONS

Changing the feedback and gain resistors of the [ADA4930-1](#) is one variation to the circuit shown in Figure 1. Increasing the feedback and gain resistors to 499 Ω marginally increases the noise floor such that performance is slightly impacted (see Figure 7).

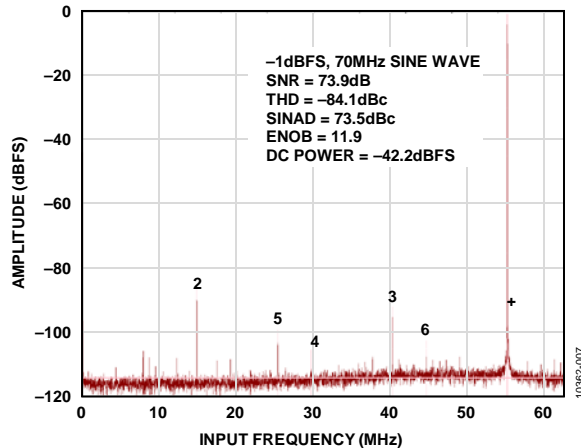


Figure 7. *VisualAnalog* FFT of [ADA4930-1](#) and [AD9265](#) Using Feedback and Gain Resistors of 499 Ω

Although the impact of changing the gain and feedback resistors is not significant, ENOB, for example, decreases from 12.1 bits to 11.9 bits.

Another variation to Figure 1 includes using alternate ADCs, such as the [AD9255](#) (14-bit, 125 MSPS), [AD9258](#) (dual 14-bit, 125 MSPS), or [AD9268](#) (dual 16-bit, 125 MSPS).

For applications requiring a dual driver, such as I/Q receivers based on the dual [AD9258](#) or [AD9268](#), the [ADA4930-2](#) driver is available.

CIRCUIT EVALUATION AND TEST

Equipment Required

The following equipment is required:

- A PC with a USB port and Windows® XP, Windows Vista® (32-bit), or Windows 7 (32-bit)
- The [EVAL-FDA-1CPZ-16](#) evaluation board
- The [AD9265-125EBZ](#) evaluation board
- The [HSC-ADC-EVALCZ](#) FPGA-based data capture kit
- [VisualAnalog](#) software
- Analog Devices [DiffAmpCalc](#) tool
- A 3.3 V at 100 mA power supply
- A 0.9 V at 100 mA power supply
- Two 6 V at 2 A wall mounted power supplies
- A 125.127 MHz Wenzel crystal oscillator (Part #500-25341)
- A 70 MHz band-pass filter
- A 125 MHz band-pass filter
- An RF source: Rohde & Schwarz SMA100A signal generator
- Coaxial cables with BNC and SMA connectors

Getting Started

Software Installation

The [VisualAnalog](#) software for the [AD9265](#) is located at www.analog.com/visualanalog, and the FPGA data capture kit user guides are available at www.analog.com/fifo. The software is compatible with Windows XP (SP2), Windows Vista, and Windows 7 (32-bit or 64-bit). Download the [VisualAnalog](#) software and install it.

Install the evaluation software before connecting the FPGA-based data capture kit to the USB port of the PC to ensure that the evaluation system is correctly recognized when connected to the PC.

Setup and Test

See the [UG-074 User Guide](#) for complete setup details on using the software and running the tests. A functional block diagram of the test setup is shown in Figure 8.

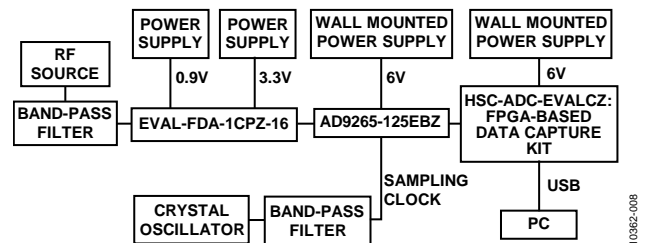


Figure 8. Test Setup Functional Diagram

The following minor hardware changes are required on the [AD9265](#) evaluation board to test the circuit shown in Figure 1:

- Install a SMA input connector at J2, INPUT-.
- Remove baluns from T3 and T6.
- Remove capacitors from C2 to C4, C15, C96, and C71.
- Remove resistors from R1, R15, R16, R22, R23, and R47.
- Install 0 Ω in R1, R22, R23, R32, C3, C25, C71, and C96.
- Install 4.7 pF capacitors at R37 and R47.
- Install a 150 nH inductor across Pin 1 and Pin 6 of the T6 footprint.
- Install a 150 nH inductor across Pin 3 and Pin 4 of the T6 footprint.
- Install a 10 pF capacitor across Pin 1 and Pin 3 of the T6 footprint.
- Remove the P18 jumper.

LEARN MORE

CN-0252 Design Support Package:

www.analog.com/CN0252-DesignSupport

UG-074 User Guide, *Evaluating the AD9265/AD9255 Analog-to-Digital Converters*.

UG-132 User Guide, *Differential Amplifier Evaluation Board for Single 16-lead 3 mm × 3 mm LFCSP Packages*.

AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*.

AN-905 Application Note, *VisualAnalog Converter Evaluation Tool Version 1.0 User Manual*.

DiffAmpCalc™ Differential Amplifier Calculator:

www.analog.com/diffampcalc

Ardizzoni, John. *A Practical Guide to High-Speed Printed-Circuit-Board Layout*, Analog Dialogue 39-09, September 2005.

MT-003 Tutorial, *Understanding SINAD, ENOB, SNR, THD, THD + N, and SFDR so You Don't Get Lost in the Noise Floor*, Analog Devices.

MT-031 Tutorial, *Grounding Data Converters and Solving the Mystery of "AGND" and "DGND"*, Analog Devices.

MT-074 Tutorial, *Differential Drivers for Precision ADCs*, Analog Devices.

MT-075 Tutorial, *Differential Drivers for High Speed ADCs Overview*, Analog Devices.

MT-076 Tutorial, *Differential Driver Analysis*, Analog Devices.

MT-101 Tutorial, *Decoupling Techniques*, Analog Devices.

Data Sheets and Evaluation Boards

ADA4930-1 Data Sheet

Evaluation Board for Single Differential Amplifiers in 16-Lead LFCSP (EVAL-FDA-1CPZ-16)

ADA4930-2 Data Sheet

AD9265 Data Sheet

AD9265 Evaluation Board (AD9265-125EBZ)

FPGA-Based Data Capture Kit (HSC-ADC-EVALCZ)

REVISION HISTORY**9/2016—Rev. 0 to Rev. A**

Changed ADA4930-1YCP-EBZ to

EVAL-FDA-1CPZ-16..... Throughout

Changes to Equipment Required Section and Figure 85

Changes to Data Sheets and Evaluation Board Section6

4/2013—Revision 0: Initial Version

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