LVDS Data Outputs for High-Speed Analog-to-Digital Converters

by Cindy Bloomingdale and Gary Hendrickson

Analog-to-digital converter (ADC) sample rates have been increasing steadily for years to accommodate newer bandwidth-hungry applications in communication, instrumentation, and consumer markets. Coupled with the need to digitize signals early in the signal chain to take advantage of digital signal processing techniques, this has motivated the development of high-speed ADC cores that can digitize at greater than 100 MHz to 200 MHz clock rates with 8- to 12-bit resolution.

In standalone converters, the ADC needs to be able to drive receiving logic and accompanying PCB trace capacitance. Current switching transients due to driving the load can couple back to the ADC analog front end, adversely affecting performance. One approach to minimize this effect has been to provide the output data at one-half the clock rate by multiplexing two output ports, reducing required edge rates, and increasing available settling time between switching instants. The AD9054A, AD9884, AD9410, and AD9430 are recent examples.

A new approach to providing high-speed data outputs while minimizing performance limitations in ADC applications is the use of LVDS (low voltage differential signaling). ADI is incorporating LVDS output capability in a new 170 MSPS, 12-bit ADC—the AD9430—and will include LVDS in some of its future high-speed ADCs and DACs (digital-to-analog converters).

LVDS is, as the name says, a low voltage differential signaling scheme. The operative words here are *low voltage* (~350 mV) and *differential*. Standards bodies have developed specifications that will be discussed later in this note. Lower voltage signal swings have the intrinsic advantage of shorter switching times as well as reduced EMI concerns (adjacent differential traces tend to cancel each others' EMI).
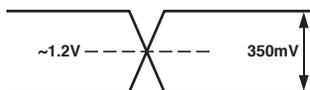

Figure 1. LVDS Output Levels

Differential signaling also has the well-known common-mode rejection benefit. Noise that is coupled to the signals tends to be common to both signal paths and cancelled out by a well designed differential receiver. LVDS outputs are current output stages requiring a 100 Ω terminating resistor at the receiver, differing from CMOS outputs that generally do not require termination. The current output results in a fixed dc load current on the output supplies—avoiding current spikes on the supply that can couple to the sensitive analog front end.
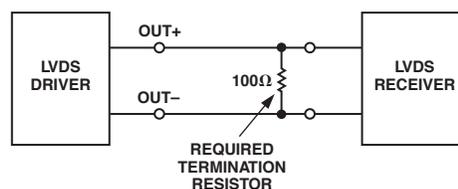

Figure 2. LVDS Requires Far End Termination

STANDARDS

Two standards have been written to define LVDS. One is the ANSI/TIA/EIA-644 which is titled, "Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits." The other is IEEE Standard 1596.3 which is titled, "IEEE Standard for Low-Voltage Differential Signals (LVDS) for Scalable Coherent Interface (SCI)." A brief summary of these two standards is provided below.

ANSI/TIA/EIA-644

The ANSI/TIA/EIA Standard was developed under the Telecommunications Industry Association (TIA) Subcommittee TR-30.2 and contains only generic electrical specifications for LVDS. Its purpose was to create a general high-speed interface standard for use in point-to-point connections between data communications equipment. The maximum data signaling rate is 655 Mbps. The TIA Subcommittee intended other standards bodies to reference ANSI/TIA/EIA-644 in more complete interface specifications between transmitters and receivers.

REV. 0

IEEE Standard 1596.3

The IEEE Standard 1596.3 was developed as an extension to the 1992 SCI protocol (IEEE Standard 1596-1992). The original SCI protocol was suitable for high-speed packet transmissions in high-end computing and used ECL levels. However, for low-end and power-sensitive applications, a new standard was needed. LVDS signals were chosen because the voltage swing is smaller than that of ECL outputs, allowing for lower power supplies in power-sensitive designs.

AD9430 LVDS Specifications

As mentioned above, the AD9430 is the first in a series of high-speed A/D converters designed with an LVDS output option (CMOS outputs are also available). It is a 12-bit, 170 MSPS ADC optimized for outstanding dynamic performance in wideband carrier systems. A simplified equivalent circuit for the AD9430 LVDS outputs is shown in Figure 3.
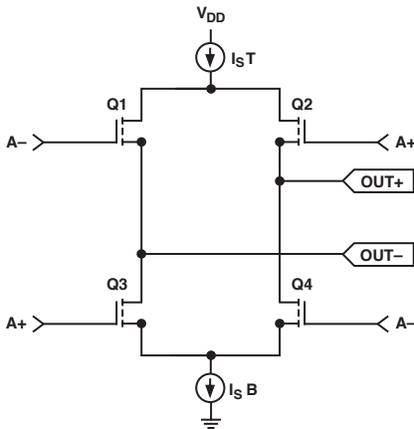

Figure 3. LVDS Data Outputs

The differential outputs are indicated in Figure 3 by OUT+, the positive or true data output, and OUT–, the complement data output of the differential signal. Circuit operation can be explained as follows (also see Figure 4). A current source (I_ST) is established on-chip from V_{DD} and is steered through Q2. In this example, a logic 1 is being transmitted (V+ > V–). The 100 Ω receiver termination resistor provides a current path for the current to return back to the driver to the lower current sink (I_SB) to ground through Q3. The nominal current source/sink is set to approximately 3.5 mA, resulting in a 350 mV swing for an external termination resistor of 100 Ω.
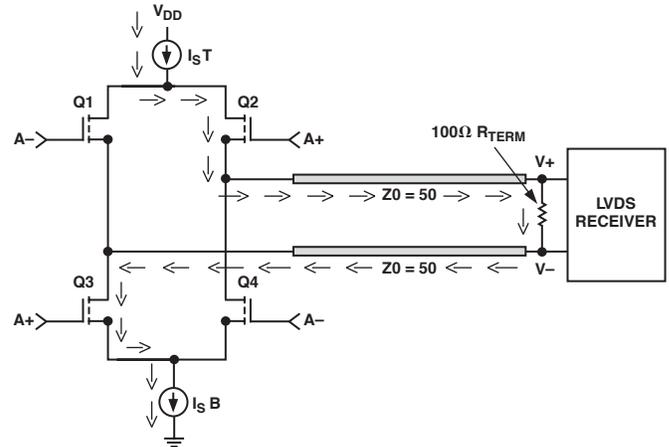

Figure 4. LVDS Output Current

Assuming an output common-mode voltage of approximately 1.2 V (common-mode control circuitry not shown), the output resistor can be modeled as two 50 Ω resistors in series with their center-tap sitting at 1.2 V. This provides a match to a typical PCB trace characteristic impedance (Z_O) of 50 Ω and minimizes reflections.

The AD9430 LVDS outputs are more closely aligned with the ANSI/TIA/EIA-644 specification. Table I compares the ANSI/TIA/EIA-644 and AD9430-170 specifications.

Table I. Summary of ANSI/TIA/EIA-644 and AD9430 Specifications

Specification	ANSI/TIA/EIA-644		AD9430-170
	Min	Max	Typ
Output Current	2.47 mA	4.54 mA	Determined by RSET (nominally 3.5 mA)
Differential Output Voltage Magnitude	247 mV	454 mV	350 mV
Output Offset Voltage (Common Mode)	1.125 V	1.375 V	1.2 V
Transition Time: Rise Time (t_R) and Fall Time (t_F); 20% to 80%		$\leq 0.3 \times t_{UI} = 0.3 \times 5.88$ ns $= 1.76$ ns	0.5 ns

Output Current
Unlike CMOS, which is typically a voltage output, LVDS is a current output technology. The AD9430 output current is set by a resistor with a typical value of 3.7 kΩ. This 3.7 kΩ resistor sets the output current to 3.5 mA. Note that the nominal output current (I_S) of 3.5 mA can be varied in the AD9430, allowing some system design flexibility. See the AD9430 data sheet for more information.

Differential Output Voltage and Offset Voltage
The ANSI specification defines the differential output voltage swing to be between 247 mV and 454 mV. Assuming that the ADC outputs are set for a 3.5 mA output current and the receiver input impedance is 100 Ω, the nominal differential output voltage is 350 mV.

The output drivers of the AD9430 were designed for a nominal 1.2 V common mode, which is well within the ANSI specification. The common mode was specified in the range 1.1 V to 1.375 V to account for ground shifts of as much as ±1 V between the driver and receiver grounds. For best performance, the ADC outputs should be located very close to the receiver inputs on the same PCB, so ground shifts should not be a concern in this application.

Transition Time
In Table I, the ANSI/TIA/EIA-644 specification defines the signal transition times for data signal rates less than or equal to 200 MHz as less than or equal to $0.3 \times t_{UI}$. The value of t_{UI} is defined as the inverse of the data signaling rate. In the case of the AD9430, the maximum signaling rate is 170 MHz, so t_{UI} is equal to 5.88 ns. Substituting 5.88 ns for t_{UI} in the specification equation results in 0.3×5.88 ns = 1.76 ns. Therefore, the rise time (t_R) and fall time (t_F) for the sum of the differential signals should be less than 1.76 ns. For the AD9430, the rise and fall time values are nominally 0.5 ns. The definitions of the rise and fall times for the LVDS differential output voltage are shown in Figure 5. LVDS rise and fall times are defined as the time for the signal to change from 20% to 80% of the maximum magnitude of the signal, as opposed to CMOS outputs, which are usually defined as the change from 10% to 90%.
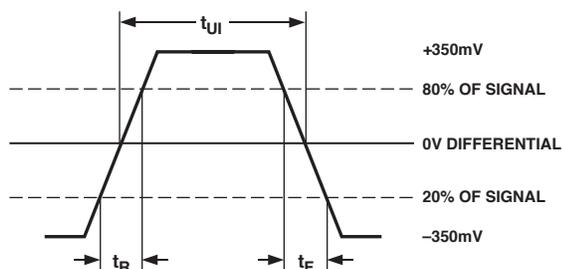

Figure 5. Timing Diagram

LVDS PCB DESIGN CONSIDERATIONS
LVDS outputs for high-performance ADCs should be treated differently than standard LVDS outputs used in digital logic. While standard LVDS can drive 1 to 10 meters in high-speed digital applications (dependent on data rate), it is *not* recommended to let a high-performance ADC drive that distance. It is recommended to keep the output trace lengths short (< 2 in.), minimizing the opportunity for any noise coupling onto the outputs from the adjacent circuitry, which may get back to the analog inputs.

The differential output traces should be routed close together, maximizing common-mode rejection with the 100 Ω termination resistor close to the receiver. Users should pay attention to PCB trace lengths to minimize any delay skew.

A typical differential microstrip PCB trace cross section is shown in Figure 6.
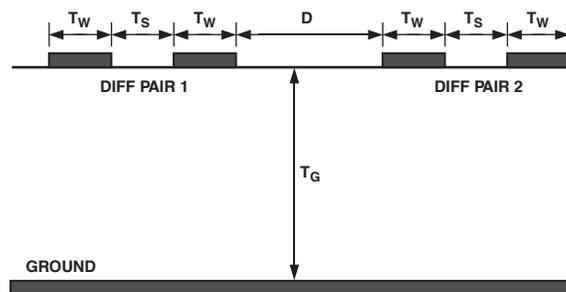

Figure 6. PCB Trace Spacing

Layout Guidelines
- Keep T_W, T_S, and D constant over the trace length
- Keep $T_S \sim < 2\ T_W$
- Avoid use of vias where possible
- Keep $D > 2\ T_S$
- Avoid 90°C bends if possible
- Design T_W and T_G for ~50 Ω

Power supply decoupling is very important with these fast (< 0.5 ns) edge rates. A low inductance, surface-mount capacitor should be placed at every power supply and ground pin as close to the ADC as possible. Placing the decoupling caps on the other side of the PCB is not recommended, since the via inductance will reduce the effective decoupling. The differential Z_O will tend to be slightly lower than twice the single-ended Z_O of each conductor due to proximity effects—the Z_O of each line should be designed to be slightly higher than 50 Ω. Simulation can be used in critical applications to verify impedance matching. In short runs, this should not be critical.

OTHER CONSIDERATIONS

LVDS also offers some benefit in reduced EMI. The EMI fields generated by the opposing currents will tend to cancel each other (for matched edge rates). Trace length, skew, and discontinuities will reduce this benefit and should be avoided.

LVDS also offers simpler timing constraints compared to a demuxed CMOS solution at similar data rates. A demuxed databus requires a synchronization signal that is not required in LVDS. In demuxed CMOS buses, a clock equal to one-half the ADC sample rate is needed, adding cost and complexity, that is not required in LVDS. In general, the LVDS is more forgiving and can lead to a simpler, cleaner design by the customer.

SUMMARY

The advantages LVDS offers in high-speed signaling can provide performance and system benefits in converter applications. ADI's portfolio of this technology within the ADC and TxDAC® products is in response to the ever increasing high-speed converter performance requirements.

REFERENCES

1. ANSI/TIA/EIA-644, *Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits*, March 1996.

2. IEEE Std 1596.3-1996, *IEEE Standard for Low-Voltage Differential Signals (LVDS) for Scalable Coherent Interface (SCI)*, March 1996.

REV. 0