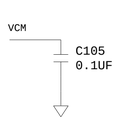
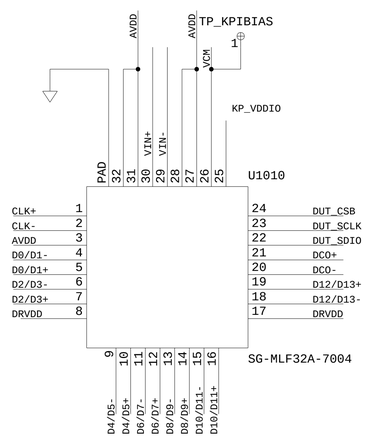
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

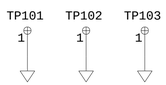
AD9642/AD9634 ENG (SOCKET)

DUT

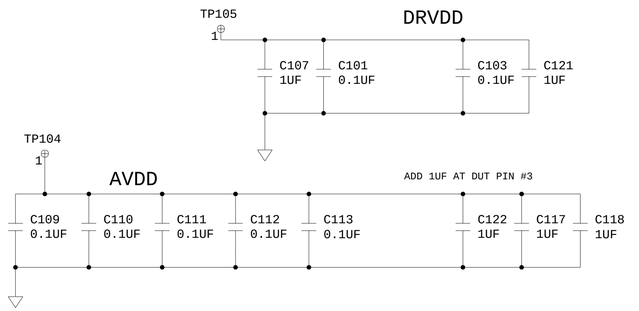
THE FOOTPRINT FOR THIS SOCKED NEEDS TO BE CHECKED AGAINST THE DRAWING







LAYOUT: DECOUPLING QUANTITY MAY VARY LAYOUT DEPENDING



ANALOG DEVICES

SCHEMATIC

9642 & 9634 ENGINEERING EVAL. PCB
AD9642
Engineering Board

DESIGN VIEW	DRAWING NO.	REV
<DESIGN_VIEW>	9642EE01	B
PTD ENGINEER	SIZE: D / SCALE: NONE	SHEET 1 OF 6
<PTD_ENGINEER>		

POWER

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

P201 PJ-202A
F201 1.1A
C201 10UF
FL201 BNX016-01
CR201
CR202 SK33A-TP
CR203 LNJ314G8TRA (GREEN)
R201 261
VIN

CR204 S2A-TP
U202 ADP150AUJZ-3.3-R7
C204 4.7UF
C205 DNI
0.01UF
C206 4.7UF
E202 100MHZ
P104
3P3V_ANALOG
DNI E203 100MHZ
U203 ADP150AUJZ-3.3-R7
C207 4.7UF
C208 DNI
0.01UF
C209 4.7UF
E204 100MHZ
P105
3P3V_DIGITAL

CR205 S2A-TP
CR206 S2A-TP
JP201 0

C210 22UF
C211 22UF
R206 10
VIN R204 0 DNI EN1
R205 1.00K
C212 1UF
R207 100K
R208 100K
C213 2200PF
C214 100PF
R214 10.5K
U206 ADP2114_PRELIM
VDD SCFG FREQ SYNC_CLKOUT OPCFG EN1 V1SET FB1 SS1 EN2 V2SET FB2 SS2 GND
VIN1 VIN2 VIN3 VIN4 VIN5 VIN6
PGOOD1 COMP1 SW1 SW2 PGOOD2 COMP2 SW3 SW4 PAD
PGND1 PGND2 PGND3 PGND4
SW_FREQ EN1 VOUTA EN2 VOUTB
R209 27K
R210 4.64K
R211 15K
C217 0.01UF
R212 15K
C218 0.01UF
VIN R221 0 DNI EN2
R222 1.00K
R213 13K
C215 1500PF
C216 100PF

VOUTA
R216 0 DNI
E210 100MHZ
R217 0
L201 2.2UH DNI
C220 22UF
C221 22UF
R215 TBD0603 DNI
C219 TBD0603 DNI
VOUTB
R218 0 DNI
E211 100MHZ
R219 0
L202 2.2UH DNI
C223 22UF
C224 22UF
R220 TBD0603 DNI
C222 TBD0603 DNI

OPTIONAL SWITCHING SUPPLY

U207 ADP150AUJZ-1.8-R7
C241 4.7UF
C242 DNI
0.01UF
C243 4.7UF
E217 100MHZ
P110
1P8V_CLOCK

P106
E208 100MHZ
U204 ADP1706ARDZ-1.8-R7
EN SENSE IN IN2 SS GND1 PAD
OUT OUT2 PAD
C225 4.7UF
C226 0.01UF
C227 4.7UF
P107
E205 100MHZ
AVDD
DNI E206 100MHZ
TO EVALUATE SHARING OF AVDD AND DVDD

U205 ADP1706ARDZ-1.8-R7
C228 4.7UF
C229 0.01UF
C230 4.7UF
P108
E207 100MHZ
DRVDD
P109
E209 100MHZ

P202
E212 100MHZ
C231 0.1UF
C232 10UF
3P3V_DIGITAL
E213 100MHZ
C233 0.1UF
C234 10UF
DRVDD
Z5.531.3625.0
E214 100MHZ
C235 0.1UF
C236 10UF
AVDD

P203
Z5.531.3425.0
E216 100MHZ
C239 0.1UF
C240 10UF
3P3V_ANALOG

ANALOG DEVCES	SCHEMATIC		
	9642 & 9634 ENGINEERING EVAL. PCB AD9642 Engineering Board		
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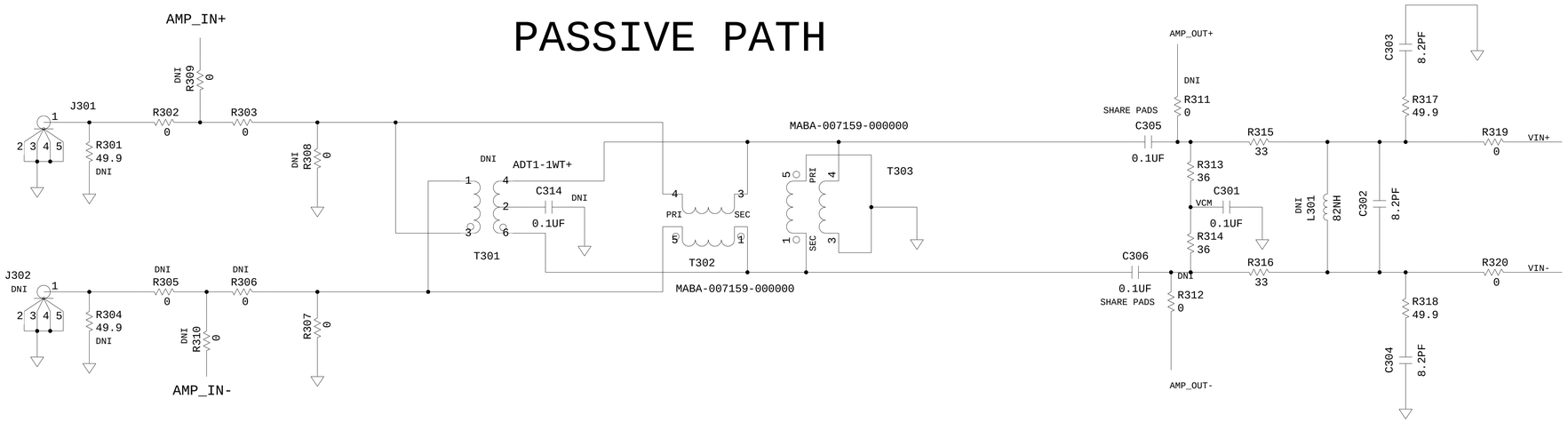
	PTD ENGINEER <PTD_ENGINEER>	SIZE D / SCALE NONE	SHEET 2 OF 6

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

ANALOG INPUT

AIN

PASSIVE PATH



LAYOUT: SMA'S SHOULD BE PLACED 540 MILS CENTER TO CENTER

ANALOG DEVICES

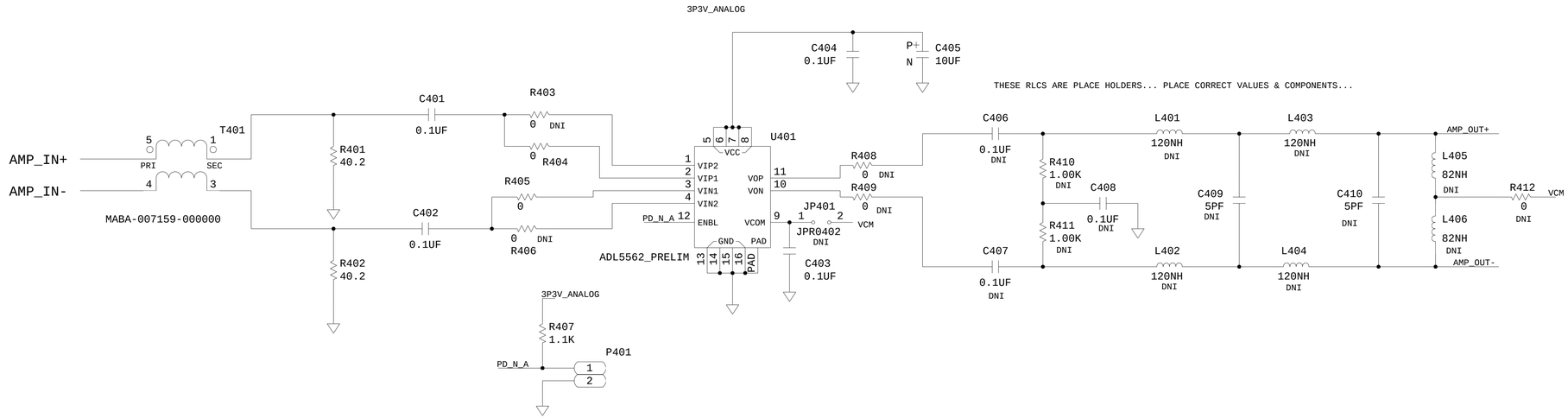
SCHEMATIC

9642 & 9634 ENGINEERING EVAL. PCB
AD9642
Engineering Board

DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 9642EE01	REV B
PTD ENGINEER <PTD_ENGINEER>	SIZE D / SCALE NONE	SHEET 3 OF 6

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

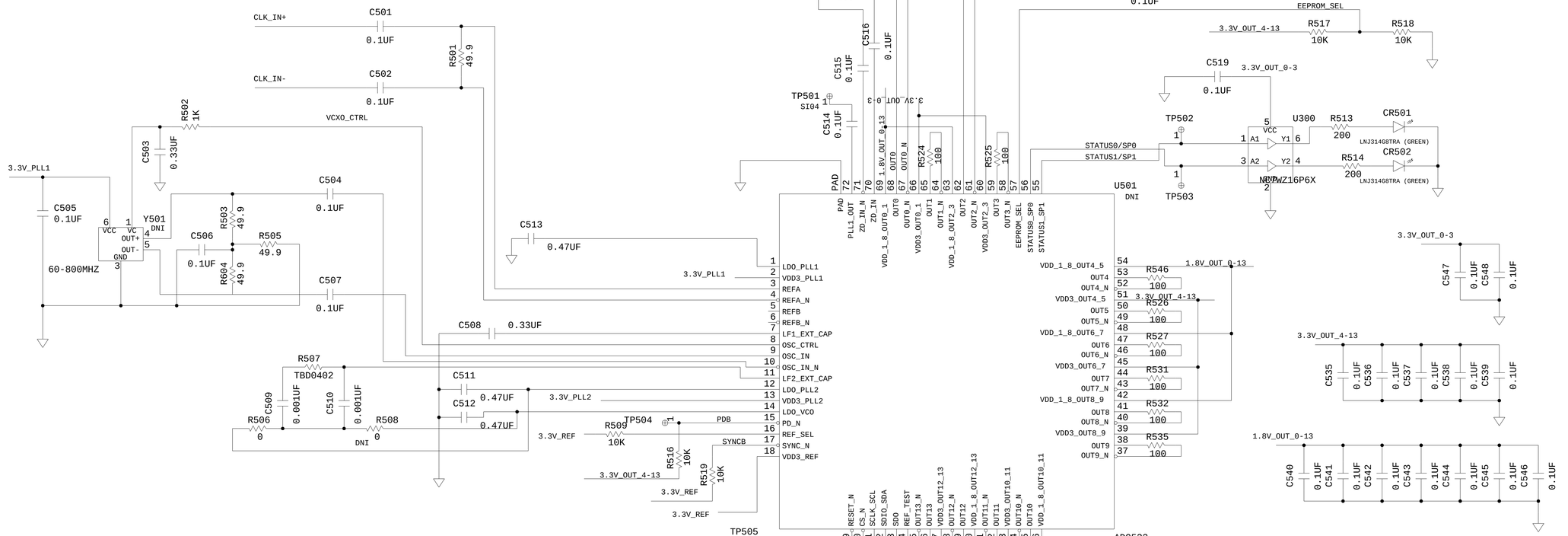
ACTIVE PATH



ANALOG DEVCES	SCHEMATIC		
	9642 & 9634 ENGINEERING EVAL. PCB AD9642 Engineering Board		
	DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 9642EE01	REV B
	PTD ENGINEER <PTD_ENGINEER>	SIZE D / SCALE NONE	SHEET 4 OF 6

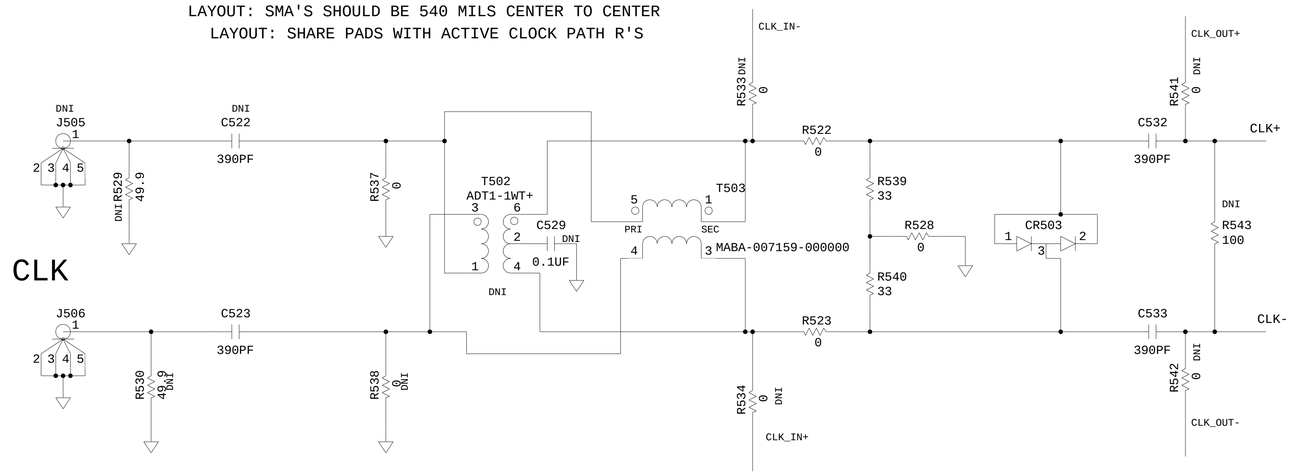
ACTIVE CLOCK PATH

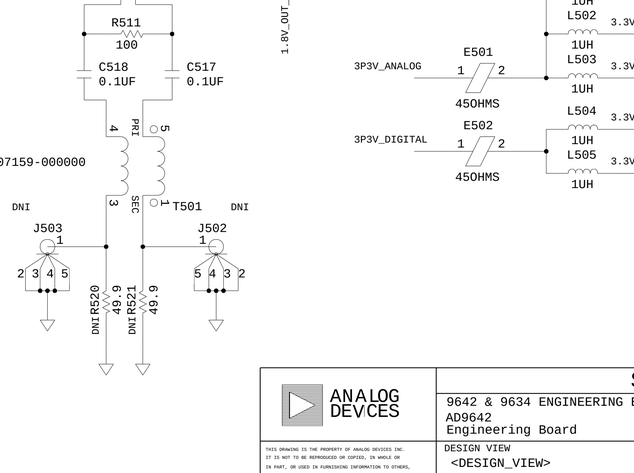
PECL/CML/LVDS CLK CIRCUITRY

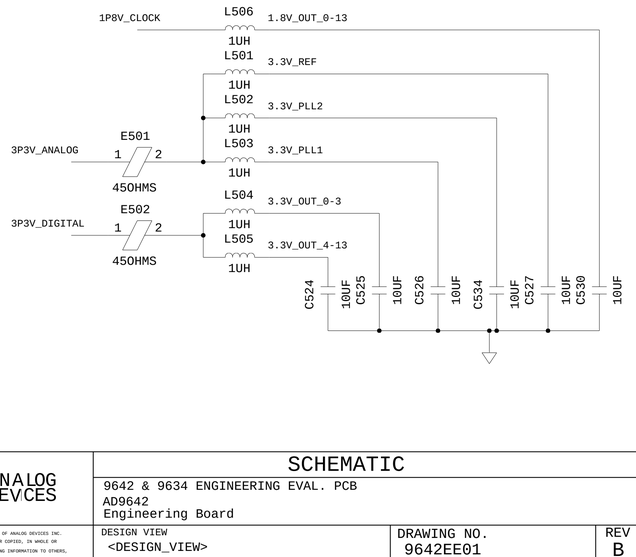


PASSIVE CLOCK

LAYOUT: SMA'S SHOULD BE 540 MILS CENTER TO CENTER
LAYOUT: SHARE PADS WITH ACTIVE CLOCK PATH R'S







REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

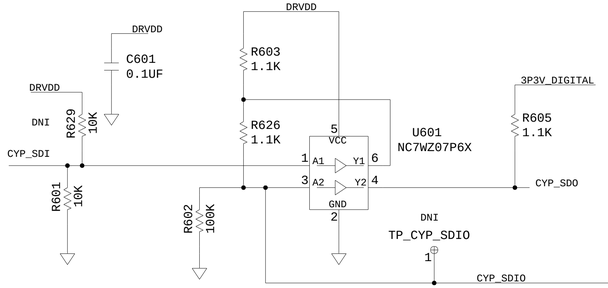
ANALOG DEVICES

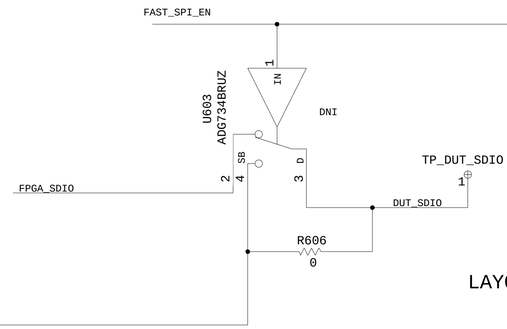
SCHEMATIC

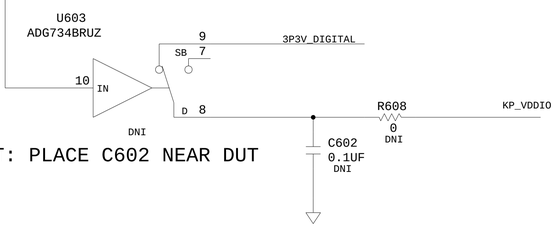
9642 & 9634 ENGINEERING EVAL. PCB
AD9642
Engineering Board

DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 9642EE01	REV B
PTD ENGINEER <PTD_ENGINEER>	SIZE D / SCALE NONE	SHEET 5 OF 6

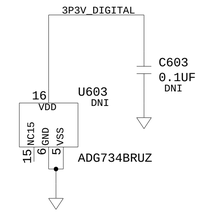
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



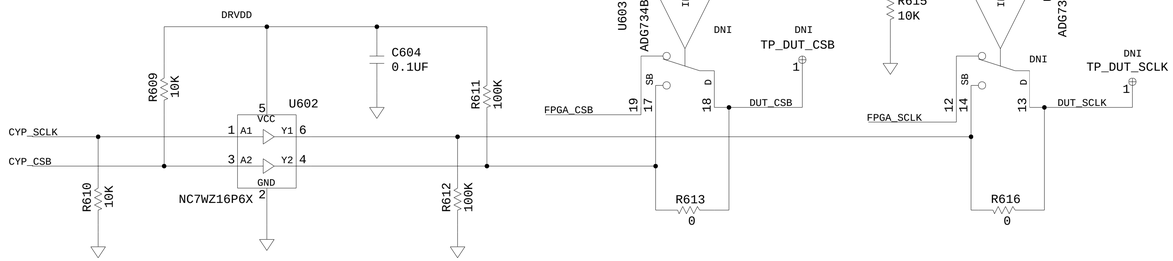




LAYOUT: PLACE C602 NEAR DUT

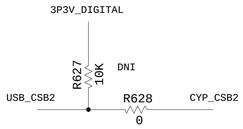


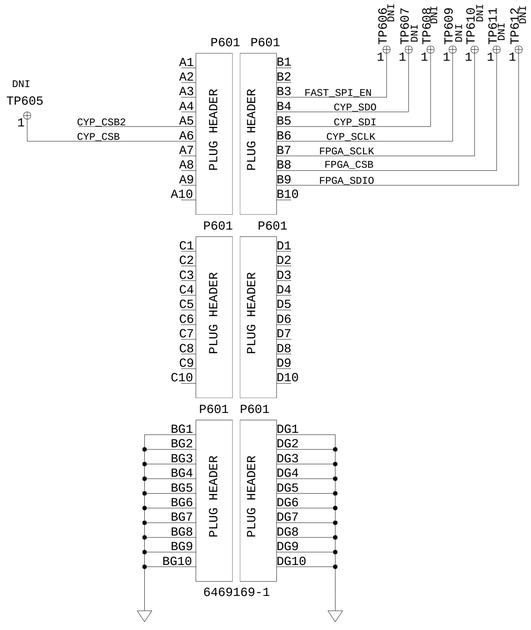
NOTE: THIS SYMBOL IS DRAWN GIVEN INPUT 1 LOGIC

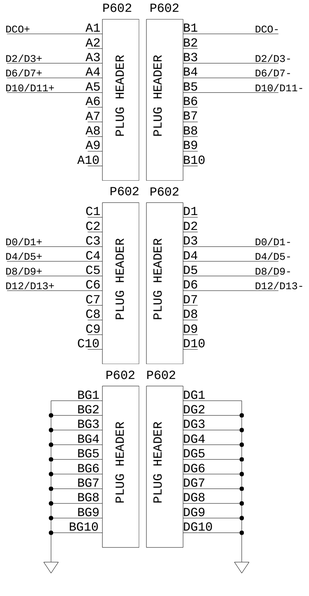


SPI & FPGA CONN.

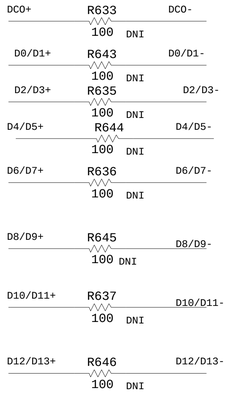
LAYOUT: ROUTE ALL TRACES TO THE TYCO CONN ON TOP OF BOARD







USING FIFO5(UNUSED PINS REMOVED



ANALOG DEVICES	SCHEMATIC	
	9642 & 9634 ENGINEERING EVAL. PCB AD9642 Engineering Board	
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	PTD ENGINEER: <PTD_ENGINEER>	SIZE: D — SCALE: NONE — SHEET 6 OF 6