ANALOG DEVICES

Circuit Note
CN-0242

Circuits from the Lab™ Reference Circuits

Circuits from the Lab™ reference circuits are engineered and tested for quick and easy system integration to help solve today's analog, mixed-signal, and RF design challenges. For more information and/or support, visit www.analog.com/CN0242

Devices Connected/Referenced	
AD9643	14-Bit Dual ADC, 250 MSPS Sampling Rate
ADL5202	Wide Dynamic Range, High Speed, Digitally Controlled VGA

High Performance, High IF, 75 MHz Bandwidth, 14-Bit, 250 MSPS Receiver Front End with Band-Pass Antialiasing Filter

EVALUATION AND DESIGN SUPPORT

Design and Integration Files

Schematics, Layout Files, Bill of Materials

CIRCUIT FUNCTION AND BENEFITS

The circuit, shown in Figure 1, is a 75 MHz bandwidth receiver front end based on the ADL5202 wide dynamic range, high speed, digitally controlled variable gain amplifier (VGA) and the 14-bit, 250 MSPS AD9643 dual analog-to-digital converter (ADC).

The fifth-order Butterworth antialiasing filter is optimized based on the performance and interface requirements of the amplifier and the ADC. The total insertion loss due to the filter network and other resistive components is approximately 2.3 dB. The overall circuit with the band-pass filter has a 1 dB bandwidth of 75 MHz (from 145 MHz to 220 MHz) and a 3 dB bandwidth of 110 MHz (from 120 MHz to 230 MHz). The pass-band flatness is 1 dB.

The circuit is optimized to process a 75 MHz bandwidth IF signal centered at 182.5 MHz (second Nyquist zone) with a sampling rate of 245.76 MSPS. The signal-to-noise ratio (SNR) and spurious-free dynamic range (SFDR) measured with a 182.5 MHz analog input across the 75 MHz band are 68.4 dBFS and 80.7 dBc, respectively.

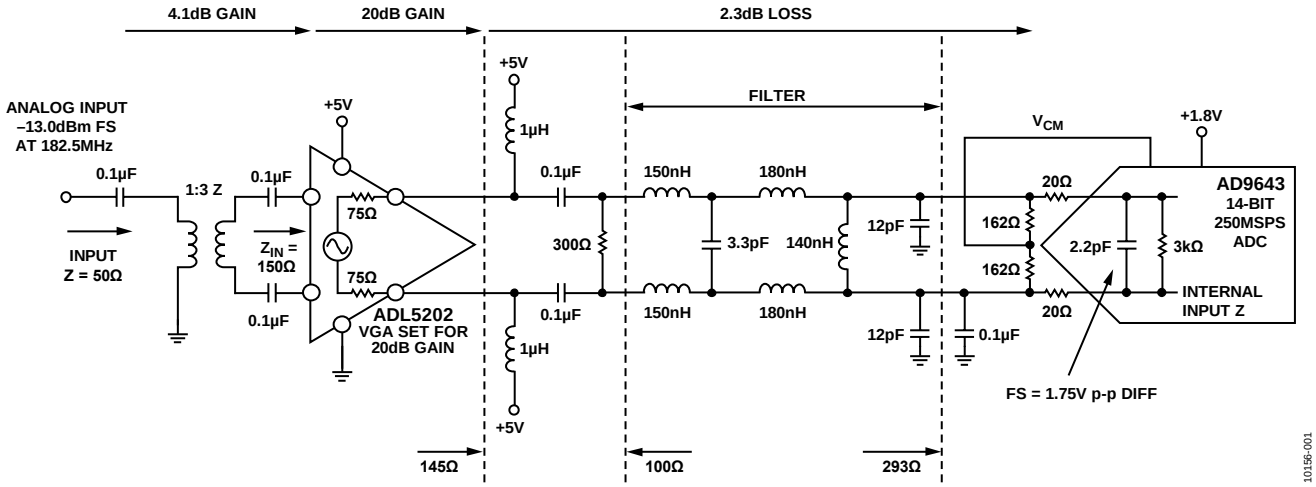

Figure 1. Single Channel of Quad IF Receiver Front End (Simplified Schematic: All Connections and Decoupling Not Shown), Gains, Losses, and Signal Levels Measured Values at 10 MHz

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

CIRCUIT DESCRIPTION

The circuit shown in Figure 1 accepts a single-ended input and converts it to a differential input using a wide bandwidth (5 MHz to 300 MHz) M/A-COM TC3-1T+ 1:3 (Z) transformer. The ADL5202 6.0 GHz differential amplifier has a differential input impedance of 150 Ω and is operated at three different gain settings: 0 dB, 10 dB, and 20 dB.

The ADL5202 is an ideal driver for the AD9643, and the fully differential architecture through the band-pass filter and into the ADC provides good high frequency common-mode rejection, as well as minimizes second-order distortion products. The ADL5202 has a programmable gain range from −11.5 dB up to +20 dB in 0.5 dB steps. In the circuit, three gain settings are used to illustrate the high performance of the ADL5202 and the AD9643.

The insertion loss of the filter network is approximately 2.3 dB, and the gain of the amplifier can be used to compensate for this loss when programming the ADL5202 for positive gain values greater than 2.3 dB. The gain also helps minimize noise impacts from the amplifier.

The antialiasing filter is a fifth-order Butterworth band-pass filter designed with a standard filter design program (in this case, the Advanced Design System [ADS] from Agilent). A Butterworth filter was chosen because of its flat response. Other filter design programs are available from Nuhertz Technologies or Quite Universal Circuit Simulator (Qucs) Simulation.

To achieve best performance, load the ADL5202 with a net differential load of 150 Ω. The 1 µH inductors provide bias for the output stage of the ADL5202, while the series capacitors isolate the filter and the ADC from this bias voltage on the amplifier output. The output of the ADL5202 is loaded with an impedance of approximately 145 Ω from the terminating resistors on the input and output of the filter in combination with the ADC resistance and series damping resistors at the ADC inputs.

The 20 Ω resistors in series with the ADC inputs isolate internal switching transients from the filter and the amplifier. The two 162 Ω resistors in parallel with the ADC serve to reduce the input impedance of the ADC for more predictable performance.

The differential input impedance of the AD9643 is approximately 3 kΩ in parallel with 2.2 pF. The real and imaginary components are a function of input frequency for this type of switched capacitor input ADC; the analysis can be found in Application Note AN-742.

The fifth-order Butterworth filter was designed with a source impedance of 100 Ω, a load impedance of 293 Ω, a 1 dB bandwidth of 75 MHz, and a 3 dB bandwidth of 110 MHz. The final circuit values for the filter are shown in Figure 2. The values chosen for the filter passive components were the closest standard values to those generated by the program. The internal 2.2 pF capacitance of the ADC was used as part of the final shunt capacitance in the filter design. This shunt capacitance at the ADC inputs to help reduce kick back charge currents from the ADC input sampling network and to optimize the filter performance.

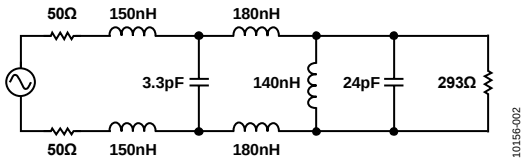

Figure 2. Final Design Values for Fifth-Order Differential Butterworth Filter with Z_S = 100 Ω, Z_L = 293 Ω, f_C = 182.5 MHz

The measured performance of the system is summarized in Table 1, where the 3 dB bandwidth is 110 MHz. The total insertion loss of the network is approximately 2.3 dB.

Table 1. Measured Performance of the Circuit

Performance Specifications at 1.75 V p-p FS	Final Result
Cutoff Frequency f_{LOW} (−1 dB)	145 MHz
Cutoff Frequency f_{HIGH} (−1 dB)	220 MHz
Cutoff Frequency f_{LOW} (−3 dB)	120 MHz
Cutoff Frequency f_{HIGH} (−3 dB)	230 MHz
Pass-Band Flatness (10 MHz to 190 MHz)	1 dB
SNR FS at 140 MHz	68.4 dBFS
SFDR at 140 MHz	80.7 dBc
H2/H3 at 140 MHz	80.7 dBc/ 84.5 dBc
Overall Gain at 182.5 MHz (ADL5202 Gain = 20 dB)	21.8 dB
Input Drive at 182.5 MHz	−13.0 dBm

The bandwidth response of the final filter circuit is shown in Figure 3, and the SNR and SFDR performances are shown in Figure 4 and Figure 5.

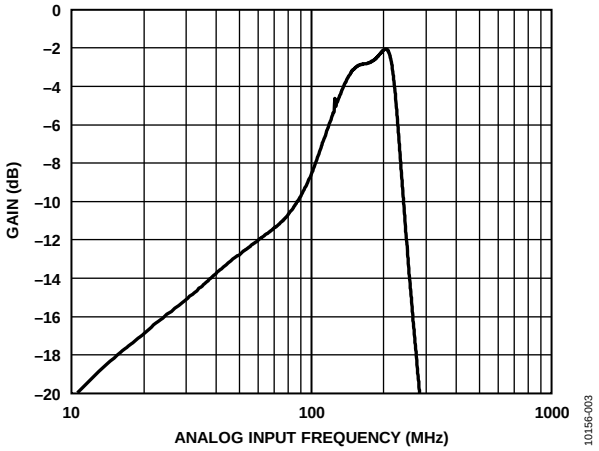

Figure 3. Pass-Band Flatness Performance vs. Analog Input Frequency

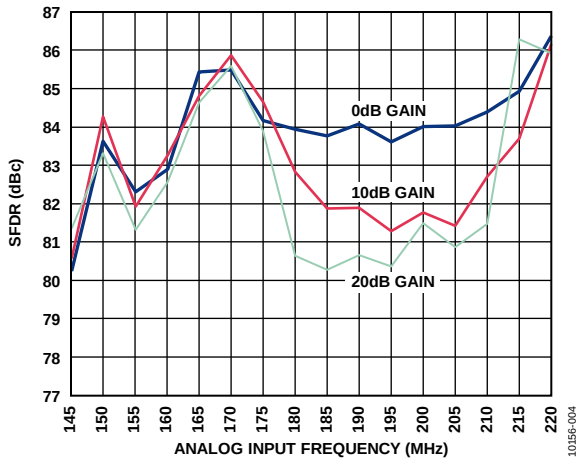

Figure 4. SFDR Performance vs. Analog Input Frequency (0 dB Gain, 10 dB Gain, and 20 dB Gain)

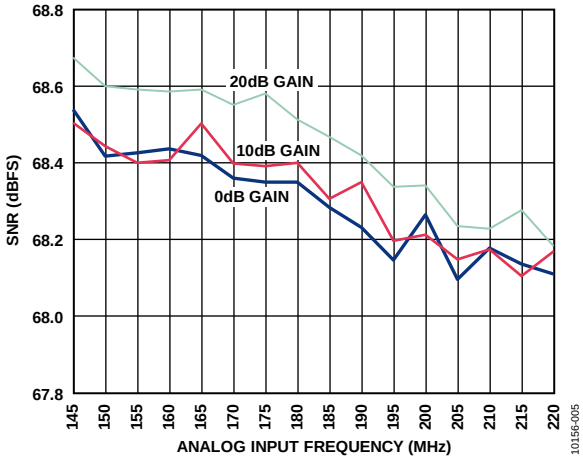

Figure 5. SNR Performance vs. Analog Input Frequency (0 dB Gain, 10 dB Gain, and 20 dB Gain)

Filter and Interface Design Procedure

A general approach to the design of the amplifier/ADC interface with the filter is presented within this section. To achieve optimum performance (bandwidth, SNR, and SFDR), there are certain design constraints placed on the general circuit by the amplifier and the ADC, such as

- The amplifier must see the correct dc load recommended by the data sheet for optimum performance.
- The dc bias inductors must be used between the amplifier and supply to properly bias the amplifier outputs.
- The input impedance of the ADC must be reduced by an external parallel resistor, and the correct series resistance must be used to isolate the ADC from the filter. This series resistor also reduces peaking.

This design approach tends to minimize the insertion loss of the filter by taking advantage of the relatively high input impedance of most high speed ADCs and the relatively low impedance of the driving source.

Details of the design procedure can be found in the CN-0227 Circuit Note, the CN-0238 Circuit Note, and the CN-0279 Circuit Note.

Circuit Optimization Techniques and Trade-Offs

The parameters in this interface circuit are very interactive; therefore, it is almost impossible to optimize the circuit for all key specifications (bandwidth, bandwidth flatness, SNR, SFDR, and gain). However, the peaking, which often occurs in the bandwidth response, can be minimized by varying either the drive amplifier output series resistors (for low impedance outputs) and/or the resistors in series with the ADC inputs (20 Ω for the circuit in Figure 1).

Select the series resistors at the ADC inputs to minimize distortion caused by any residual charge injection from the internal sampling capacitor within the ADC. Increasing this resistor also tends to reduce bandwidth peaking.

However, increasing the ADC input series resistors also increases signal attenuation, and the amplifier must drive a larger signal to fill the ADC input range.

Another method for optimizing the pass-band flatness is to vary the filter shunt capacitors by a small amount.

The ADC input termination resistor (364 Ω for the circuit in Figure 1) should normally be selected to make the net ADC input impedance between 200 Ω and 400 Ω. Making it in this range reduces the effect of the ADC input capacitance and may stabilize the filter design; however, it increases the insertion loss of the circuit. Increasing the value also reduces peaking.

Balancing these trade-offs can be somewhat difficult. In this design, each parameter was given equal weight; therefore, the values chosen are representative of the interface performance for all the design characteristics. In some designs, different values can be chosen to optimize SFDR, SNR, or input drive level, depending on system requirements.

The SFDR performance in this design is determined by two factors: the amplifier and the ADC interface component values, as shown in Figure 1. The final SFDR performance numbers shown in Table 1 and Figure 4 were obtained after optimizing the filter design to account for the board parasitics and nonideal components used in the filter design.

Another trade-off that can be made in this particular design is the ADC full-scale range setting. The full-scale ADC differential input voltage was set for 1.75 V p-p for the data obtained with this design, which optimizes SFDR. Changing the full-scale input range to 2.0 V p-p yields a small improvement in SNR; however, it slightly degrades the SFDR performance. Changing the full-scale input range in the opposite direction to 1.5 V p-p yields a small improvement in SFDR but slightly degrades the SNR performance.

The signal in this design is ac-coupled with 0.1 µF capacitors to block the common-mode voltages between the amplifier, its termination resistors, and the ADC inputs. Refer to the AD9643 data sheet for further details regarding common-mode voltages.

Passive Component and PC Board Parasitic Considerations

The performance of this or any high speed circuit is highly dependent on proper printed circuit board (PCB) layout. This includes, but is not limited to, power supply bypassing, controlled impedance lines (where required), component placement, signal routing, and power and ground planes. See the MT-031 and MT-101 tutorials for more detailed information regarding PCB layout for high speed ADCs and amplifiers.

Use low parasitic surface-mount capacitors, inductors, and resistors for the passive components in the filter. The inductors chosen are from the Coilcraft 0603CS series. The surface-mount capacitors used in the filter are 5%, C0G, 0402 type for stability and accuracy.

See the CN-0242 Design Support Package for complete documentation on the system, including schematics, bill of materials, and PCB layout.

COMMON VARIATIONS

For applications that require less bandwidth and lower power, the ADL5562 differential amplifier can be used. The ADL5562 has a bandwidth of 3.3 GHz. For even lower power and bandwidth, the ADA4950-1 could also be used. This device has a 1 GHz bandwidth and only uses 10 mA of current.

CIRCUIT EVALUATION AND TEST

This circuit uses a modified AD9643-250EBZ circuit board and the HSC-ADC-EVALCZ FPGA-based data capture board. The two boards have mating high speed connectors, allowing for the quick setup and evaluation of the performance of the circuit. The modified AD9643-250EBZ board contains the circuit evaluated as described in this circuit note, and the HSC-ADC-EVALCZ data capture board is used in conjunction with VisualAnalog evaluation software, as well as the SPIController software to properly control the ADC and capture the data. See the UG-293 User Guide for the schematic, BOM, and layout files for the modified AD9643-250EBZ board. The **readme.txt** file in the CN-0242 Design Support Package describes the modifications made to the standard AD9643-250EBZ board. Application Note AN-835 contains complete details on how to set up the hardware and software to run the tests described in this circuit note.

LEARN MORE

CN-0242 Design Support Package: http://www.analog.com/CN0242-DesignSupport

UG-293: Evaluating the AD9643/AD9613/AD6649/AD6643 Analog to Digital Converters

Alex Arrants, Brad Brannon and Rob Reeder, AN-835 Application Note: Understanding High Speed ADC Testing and Evaluation, Analog Devices.

Ardizzoni, John. *A Practical Guide to High-Speed Printed-Circuit-Board Layout*, Analog Dialogue 39-09, September 2005.

MT-031 Tutorial, *Grounding Data Converters and Solving the Mystery of "AGND" and "DGND"*, Analog Devices.

MT-101 Tutorial, *Decoupling Techniques*, Analog Devices.

Agilent Technologies, Advanced Design System.

Reeder, Rob, *Frequency Domain Response of Switched Capacitor ADCs*, AN-742 Application Note, Analog Devices.

Reeder, Rob, *Achieve CM Convergence between Amps and ADCs*, Electronic Design, July 2010.

Reeder, Rob, *Mine These High-Speed ADC Layout Nuggets For Design Gold*, Electronic Design, September 15, 2011.

Rarely Asked Questions: *Considerations of High-Speed Converter PCB Design, Part 1: Power and Ground Planes*, Design News, November 2010.

Rarely Asked Questions: *Considerations of High-Speed Converter PCB Design, Part 2: Using Power and Ground Planes to Your Advantage*, Design News, February 2011

Rarely Asked Questions: *Considerations of High-Speed Converter PCB Design, Part 3: The E-Pad Low Down*, Design News, June 2011

Data Sheets and Evaluation Boards

AD9643 Data Sheet

AD9643 Evaluation Board (AD9643-250EBZ)

Standard Data Capture Platform (HSC-ADC-EVALCZ)

ADL5202 Data Sheet

REVISION HISTORY

9/12—Revision 0: Initial Version