ANALOG DEVICES

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APPLICATION NOTE

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Multicarrier WCDMA Feasibility

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ABSTRACT

The goal of this application note is to determine the feasibility of implementing a multicarrier 3G transceiver and what the major subsystem performances must be.

GENERALIZED BLOCK DIAGRAM

The block diagram in Figure 1 is the general block diagram used in this document. While there are many variations of this design, the key focus is on this architecture. This architecture represents a flexible radio platform that can easily be used to implement a wide variety of air standards including WCDMA, CDMA2000, and TD-SCDMA.

Some of the possible variations to this architecture include high or low IF sampling as well as direct conversion for receive. Although the latter is not feasible for multicarrier today, it is acknowledged as the low cost, high performance solution in the near future. In the transmit path, direct RF modulation is feasible for most applications as long as some amount of IQ balance is provided. This represents the lowest cost transmit path. For applications requiring high performance without an IQ balance network, superheterodyne IF upconversion is another excellent option.

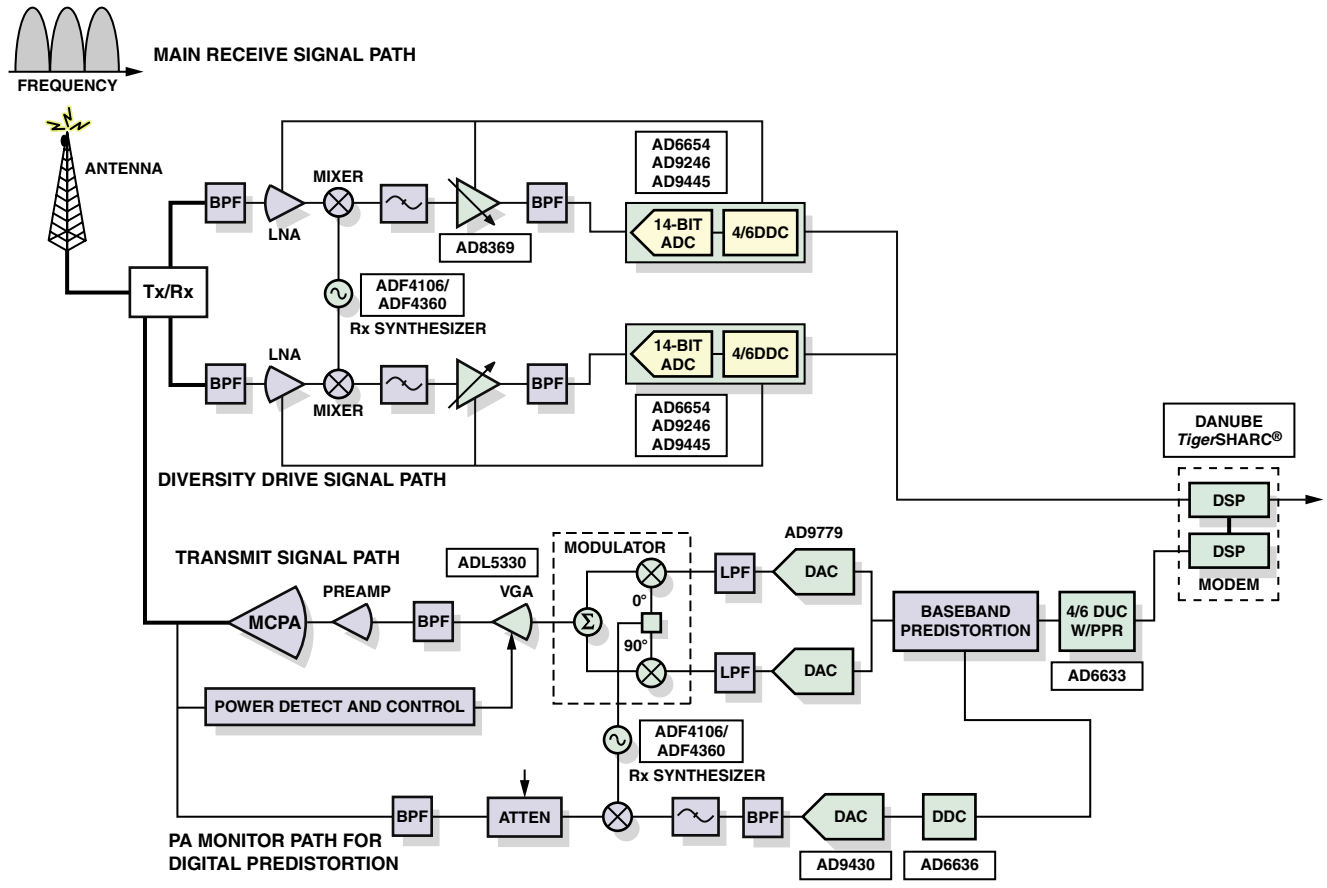

Figure 1. ADI Wideband Multicarrier TRX Common Platform CDMA2000/WCDMA/TD-SCDMA

In addition to variations in the electrical schematic discussed, there are many assembly options that have a wide range of implications. These options include system level partitioning in the form of split Rx and Tx boards as well as split radio and baseband processing. Further options include chip partitioning. One example is the availability of MxFE functions that incorporate both Rx and Tx functions in a single package. This option can facilitate higher integration and lower cost, and offers an excellent alternative for low capacity system options. Other possibilities include combining the ADC and RSP to provide higher integration and lower cost while avoiding import/export restrictions. These and other options are good sources of discussion.

WCDMA

Specifications for this report are taken from the requirements for Wide Area BS as defined by 3GPP TS 25.104 V6.2.0, specifically, section 7. Key specifications from this standard are the reference sensitivities, band of deployment, and blocking requirements. It is assumed that the Node B terminal is not required to meet the sensitivity and blocking requirements of different platforms at the same time. Meeting the sensitivity of a wide area BS while also matching the blocking requirements of the local area BS may be desirable, but is not the goal discussed here. It should be noted that the requirements of Node B terminals for medium and local area BS have similar dynamic range requirements to the wide area version with the exception that the input levels are shifted up. These can be accommodated within the same design by shifting the level plans upward as these systems can also tolerate increased noise.

RECEIVE DISCUSSION

Receiver operating conditions: From the standard, the required minimum sensitivity is –121 dBm within a 3.84 MHz channel bandwidth. On a per Hertz basis, this is a signal density of –186.8 dBm/Hz. Where noted, the WCDMA test conditions specify –115 dBm/3.84 MHz (–180.8 dBm/Hz) also applies.

The second set of conditions is to determine the inband blockers. From the standard, there are two important subconditions for blocking. The first subcondition is intermodulation between two signals at –48 dBm (–47 dBm in operating bands II and III with GMSK blocker). One is a CW tone and the other is a modulated WCDMA carrier (see Figure 4). The second subcondition is the adjacent and the first and second alternate blockers. Of these, the largest is –40 dBm/3.84 MHz. The signal at –40 dBm is assumed to be modulated with a single code and therefore has a peak-to-rms value of about 3.5 dB. From the input conditions above, the largest input power condition is the blocker at –40 dBm/3.84 MHz, giving a peak power of about –36 dBm. It is assumed that out-of-band signals are attenuated and do not enter into the dynamic range considerations of the ADC. Since signals in the adjacent bands are the same as inband, some attenuation may be anticipated by the band filter. However, because they are at the same level or below after filtering as the inband blockers, little additional dynamic range should be required, but this depends on the characteristics of the band filter selected. The key requirement of this wideband filtering is that signal aliasing is prevented. Therefore, any analog filtering must provide sufficient rejection so as to attenuate blockers into the noise floor as they alias back into the useable spectrum of the ADC. This is true for either IF sampling or direct conversion.

Assumptions: Given this information, the front-end design information can now be determined. If the largest peak signal at the antenna is about –36 dBm and the converter full scale is 4 dBm rms/7 dBm peak (2 V p-p into 200 Ω is typical for many ADCs), a conversion gain of up to 43 dB can be used. A gain of 40 causes the ADC to be driven with a peak input of about +4 dBm, leaving 3 dB at the top that can serve as margin for power from other nearby strong signals as well as component margin. Given current receiver trends in LNAs, passive mixers and filter elements, typical downconverter blocks are possible with noise figures below 3 dB (not including the ADC). These numbers are used in the following calculations. If losses from cabling and other hardware are to be considered along with variations in component tolerance, they must be included as well.

The final assumption is that of sample rate for the ADC. With a base data rate of 3.84 MHz, clock rates of 16×, 20×, 24×, and 32× are viable. Since converter data rates are steadily increasing and running, a higher sample rate has slight noise advantages. One of the higher rates, such as 92.16 MHz, should be used. If the lower rates are used for actual implementation, the SNR requirement increases by 1 dB for 76.8 MSPS and 2 dB for 61.44 MSPS. In addition to noise advantage, the higher sample rate allows more transition for band filters, as already discussed. If complex baseband sampling is used, a dual 12-bit or 14-bit converter family, such as the AD9228 and AD9248, are ideal.

ADC SNR requirements: Given the conversion gain and NF above, the ADC SNR can now be calculated. At the antenna, the noise spectral density is assumed to be –174 dBm/Hz. Given the conversion gain and noise figure previously stated, the noise spectral density (NSD) at the ADC input is –131 dBm/Hz (–174 + 40 + 3). This assumes that noise outside the Nyquist band of the ADC is filtered using antialiasing filters to prevent front-end thermal noise from aliasing when sampled by the ADC. If the ADC noise floor is 10 dB below that of the front-end noise, it contributes about 0.1 dB to the overall NF of the receiver. Therefore, a maximum ADC noise floor of –141 dBm/Hz can be expected. Higher ADC noise floors can be used. As the ADC noise begins to contribute to the floor of the receiver, some of the nonlinearities described in the "DNL and Some of its Effects on Converter Performance"

article found in the *Wireless Design & Development Online* June 2001 online issue can adversely impact receiver performance, especially when it comes to signal power estimation. Therefore, the ADC noise floor should be as small as reasonable without over designing.

For IF sampling, the total noise in the Nyquist band of the ADC can be determined by simple integration. Over 46.08 MHz (the Nyquist band of 92.16 MHz), the total noise is found to be –64.4 dBm. If the rms full scale of the ADC is +4 dBm, this is a required minimum full-scale SNR of 68.4 dB. When larger blockers are considered, as in the case of band II and III, higher noise performance is required from the ADC as seen in the following sections.

Although direct downconversion is not quite ready for this market space, it is the preferred architecture for cost and simplicity reasons. It is likely that this approach will be available within the scope of a new multicarrier development and is therefore considered in this application note. The limitations are currently the quadrature demodulator and the data converters. For multicarrier applications the critical aspects are IQ balancing and second-order intermodulation through the demodulators and data converters. Beyond this, the data converters must still meet the same general performance levels as with the IF sampling variations with the advantage of a low frequency input range.

For baseband sampling, two frequency planning options exist for direct conversion. The first option is to balance active FAs on either side of dc. If this is an odd number, one FA is at dc. If this is an even number, no FA exists at dc. If this option is selected, the image rejection on the adjacent sideband must be sufficient to meet the blocking requirements of a signal at –40 dBm in the presence of a –121 (–115) dBm as discussed previously. It is reasonable to assume that an FA falls at dc and, therefore, a concern must exist for dc noise in the form of LO feedthrough, phase noise, and dc offset. This concern is in addition to the second-order intermodulation distortion generated within the demodulator. These are the primary impediments to implementation of a multicarrier direct conversion receiver. Although not unique to multicarrier signal chains, restrictions are not as great on single carrier signal paths that are easier to implement. The second option is to place all of the signals on one side of dc and let the images fall to the other side unabated. This option is wasteful of spectrum, but does allow less focus on the image rejection issues and more on specifications such as intermodulation distortion.

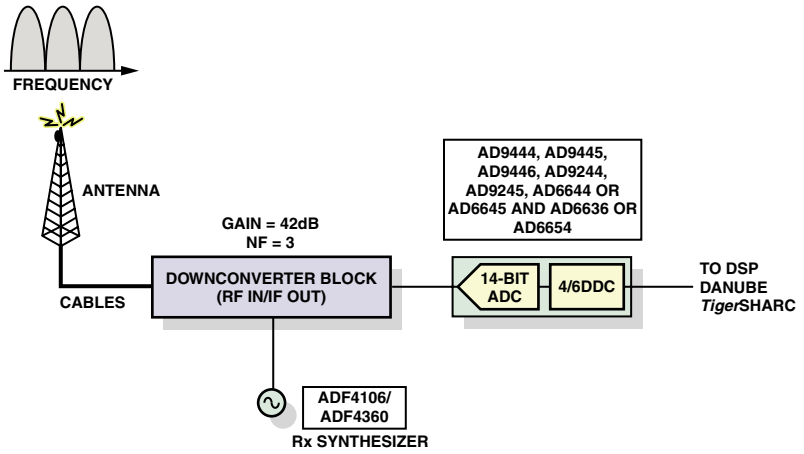

Figure 2.

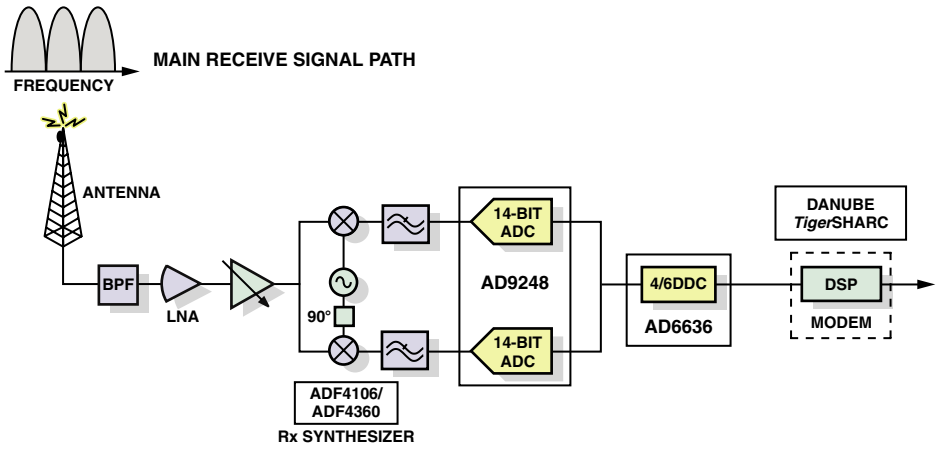

Figure 3.

It is possible to address many of the quadrature balance issues in the digital domain; this is discussed in more detail in a later section. To facilitate this, means for addressing IQ gain mismatch, dc offset, IQ phase correction, and complex baseband tuning are required. In order to combat some of these issues, the AD6636 includes various features used to compensate for them. The AD6636 is equally suitable for IQ signal processing of multicarrier signals as it is for multicarrier IF sampling. It includes IQ gain adjustment, automatic dc offset correction, IQ phase correction, and the ability to perform complex baseband tuning.

For direct conversion, there are several other considerations that must be made. First, a lower sample rate is likely. Since two converters are required, it is likely that a lower sample rate is used to keep digital processing and power as low as possible. A sample rate of 61.44 MSPS is likely, providing a full 61.44 MHz of complex bandwidth. If it is assumed that the ADCs keep the same input range, a 3 dB increase is allowable since the IQ splitter also divides the power between the two ADCs in addition to the losses associated with a typical frequency translation stage. Without this additional gain, 3 dB (approximately) of ADC range will be lost. In the digital processing, these signals are again summed and produce an overall signal 3 dB higher along with a 3 dB higher ADC noise floor from the noncorrelated ADC noise floor of both ADCs. At the same time, however, the effective ADC input range is also 3 dB higher as is the noise floor of the effective ADC contributions. This results in a first-order wash in sensitivity as signal levels and noise each increase by the same amount. If the signal path includes the extra 3 dB gain, the IP3 requirements increase a proportionate amount. First order, each single ADC must also meet the same requirements for IF sampling. Although the sample rate is lower than may have otherwise been used for IF sampling, the noise bandwidth is equal to the full sample rate. The result is that the noise performance is similar to that of an IF sampling solution operating at 122.88 MSPS with two added advantages. First, because the analog signals are at baseband, clock jitter is no longer a problem. Second, because the analog signals are at baseband, they are not subjected to input slew rate limitations of the converter, which is one of the biggest causes of poor harmonic distortion in IF sampling systems.

The primary focus thus far has been to provide a fixed gain solution that meets the dynamic range requirements. This requires a delicate balance between placing the ADC noise sufficiently below the receiver analog thermal noise without overdriving the ADC. As discussed earlier, a converter with a minimum SNR of 68.4 dB makes this possible. However, there may be times when it is desirable to increase the difference between the ADC noise and Rx thermal noise or to increase the signal range on the top end. This can be accomplished by providing an AGC circuit. While this may be useful in single carrier systems to reduce the dynamic range requirements of the ADC, it is not desirable for a multicarrier application, albeit necessary in many cases. In such a system, it may be desirable to trade off gain control range for converter resolution to maintain similar dynamic ranges. Since any individual WCDMA carrier is likely to reside at about –70 dBm most of the time, significant additional gain could be applied in the absence of other blocking signals. However, this is only desirable provided the trade-off between gain and intermodulation is favorable, which is often the case in nonblocking conditions. Signals at this level are significantly above the noise floor and, therefore, this additional gain only provides marginal improvements. This indicates that a fixed lower gain is not only desirable from a performance point of view, it is also desirable from a logistical point of view.

Regardless of any implemented gain control, it is very important that power levels be known. WCDMA's strict power measurement requirements require a means of estimating power levels. While this can easily be accomplished in the DSP, it is often more efficient to implement in the digital hardware. Performing this in hardware can remove some of the processing burden from the DSP as well as minimize the latency of the calculation, which also reduces the chance of front-end overdrive if an analog AGC is required.

Based on the SNR requirements, a good 12-bit ADC could be used to preserve the dynamic range between both the minimum sensitivity and the largest inband blocker. However, this assumes a deployment in the WCDMA band. When deployed in the 850 MHz, 900 MHz, 1800 MHz, or 1900 MHz band, the conversion gain is limited by the presence of narrow-band blockers. These blockers may be 10 dB to 12 dB higher than in the WCDMA band (20+ dB higher in the 900 MHz band) and, therefore, the conversion gain must be reduced, likely reducing the sensitivity. This can be achieved by either reducing the overall fixed conversion gain or by maintaining the higher gain, but also by adding a VGA that reduces the gain during large signal conditions. In this manner, the reference sensitivity can be maintained but sacrificed systematically as total receiver input signal level increases. A proposed solution is to convert 12 dB of the conversion gain to a VGA. This can then be reduced under the appropriate signal conditions to prevent clipping or limiting of the receive signal chain. Digital downconverter products such as the AD6636, can be configured to control the VGA in addition to readjusting the digital data stream such that the absolute digital output data maintains the correct power information.

There are two ways of implementing the VGA. For example, the VGA can be set to adjust signals at the bottom end of the range, reducing gain as soon as signals are large enough to overcome noise limitations. Likewise, the VGA can be set to adjust signals at the top end of the range, reducing the gain just prior to clipping or limiting within the signal chain. Each has advantages and disadvantages with a desirable goal being to implement the receiver without any gain control.

If a VGA is implemented, it should include both voltage and time hysteresis to prevent remodulation of signals. Table 1 shows expected sensitivity as gain is rolled off. It should be remembered that as gain is reduced, the ADC contributes more to the total NF of the receiver and therefore overall receiver impairments. For example, in the high gain state, the noise density of the front end presented to the ADC is –131 dBm/Hz. In the low gain state, the noise has dropped to –137 dBm. If the ADC noise density is –145 dBm, the implication is an increase in the percentage of total noise that comes from the ADC. Given this, as long as sufficient gain can be run, a 14-bit converter is more than adequate for a multicarrier implementation of WCDMA. If conversion gain begins to run low, the noise of the ADC dominates and receiver performance suffers.

The required analog gain control can be implemented by taking advantage of the power measurement within the AD6636 or through other DSP calculations with the loop completed through a VGA implementation. In addition, the AD6636 incorporates an ADC preclip function that allows peak signals that are less than full scale to be detected and sets the gain of a digital gain amplifier or PIN diode attenuator before the converter full scale is reached, thereby preventing converter clipping. The DDC also incorporates digital compensation for the analog changes so that the final digital data is relinearized with respect to the true analog input to the receiver. Similarly, the latency of the analog gain path, including the pipeline delay of the ADC, is accounted for in this process.

SFDR requirements: Spurious performance is a little less obvious from the specifications. However, there are several guidelines in the standard that provide SFDR requirements. These are primarily found in the single and two-tone blocking specifications. In this test, a narrow-band signal (CW) is allowed to intermodulate with either a WCDMA signal or a GMSK signal depending on the band of operation. For WCDMA conditions, both signals are posted at –48 dBm whereas the GMSK (bands II and III) are set to –47 dBm.

Looking first at the band II and III test with GMSK, the intermodulation product falls outside the channel of interest, 2.4 MHz from channel center where the channel 3 dB bandwidth is 1.92 MHz. Digital channel filtering provides adequate filtering of the intermodulation products before the correlator and, therefore, no direct impact is anticipated with the signal of interest. It is assumed that fifth order products are significantly better than anticipated third order products. Even though they fall inband, they should not be an issue. If they do, they must meet the spurious requirements determined below.

For the intermodulation between a CW tone and a WCDMA carrier, the resulting intermodulation product falls directly on the channel of interest. The net effect of this is to increase the noise in the channel as would AWGN. The specification allows for 6 dB of reduced sensitivity for this test. Since receiver performance is limited by thermal noise, setting noise due to intermodulation and spurious equal to the noise floor increases the noise by 3 dB and reduces the sensitivity by the same amount. Since 6 dB is allowed, the remaining 3 dB can be allocated elsewhere (jitter, additional NF, or other). Assuming that conversion gain has not yet been reduced from 40 dB (the AGC point is above the two-tone levels) and that the ADC is providing 74 dB of SNR, the total NF of the receiver is 3.1 dB. Therefore, the noise density (reflected back to the antenna) including the ADC is –171 dBm/Hz. If this is integrated over one channel (3.84 MHz), the total noise is –105 dBm. This is the power of the intermodulation term that isallowed by the intermodulation between the CW and WCDMA signals. This provides detailed information about spurious levels that have to be met. If the intermodulation product is a WCDMA-type product, the energy is already spread and simply appears as AWGN (and spread over 2× by convolution between two different codes—assuming that aliasing does not occur somewhere in the receiver chain). The only exception to this is, of course, if the intermodulating signal is not orthogonal to the signal of interest, but this is assumed not to be the case. Similarly, if the IMD product is a CW tone (not specified in the standard, but is a worst case), it spreads by the PN sequence in the correlation process, again appearing as AWGN. Since all

Table 1.

Gain	AFE NF	0 dB SNR	Effective NF	Effective SNR @ –121 dBm*	ADC Clip Point
40 dB	3 dB	129 dB	3.1 dB	8	–36 dBm
34 dB	6 dB	125.88 dB	6.25 dB	4.88	–30 dBm
28 dB	9 dB	122.64 dB	9.48 dB	1.64	–24 dBm

This table assumes that during the reduction of gain that the AFE NF is increased by one half of the gain reduction.
*This number is –115 dBm for blocking conditions. The numbers in this table do not represent this increase in signal.

of the energy in a CW tone is within a single frequency, this is a more stringent test. Therefore, if the ADC input-referred spurious (the sum of all spurious) must be –65 dBm (–105 dBm plus 40 dB), this sets the absolute worst case spurious that can be tolerated for a cochannel interferer whether generated by single tone, multitone, or intermodulation. Since the ADC full scale is +4 dBm (rms) and the worst case equivalent sum of spur that can be tolerated is –65 dBm, this is equivalent to an SFDR of about 69 dBFS minimum. While conditions that generate the worst case may vary, this represents the worst case cumulative SFDR that can be tolerated.

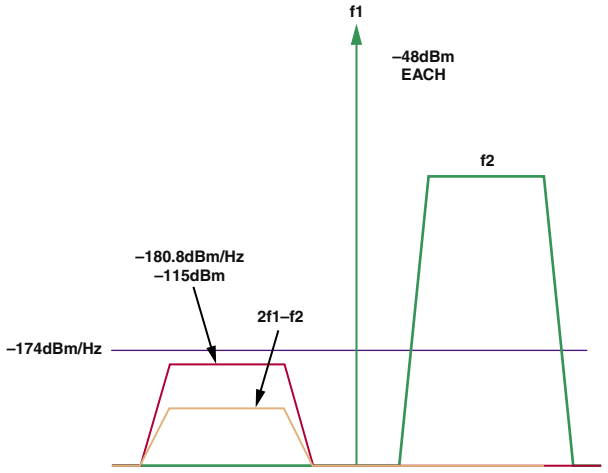

Figure 4.

SFDR split: If it is assumed that the ADC and the downconverter block equally share in the harmonic distortions and are not correlated, each source should be no worse than –72 dBFS (relative to the ADC input) and, more appropriately, –78 dBFS which allows not only for headroom but for the case where the two contributions to SFDR can peak simultaneously. For the case where the gain has been reduced to account for larger blockers (band II and III), the spurious requirements are higher. Although the details are not shown here, the cumulative SFDR is 75 dBFS and allowing for headroom and signal peaking, 81 dBFS minimum.

IP3 requirements: One of the more stringent intermodulation tests are in band II and III under the GMSK test. In this case, two essentially narrow-band tones are placed into the receiver at –47 dBm. This would be the condition as anticipated in a mixed band. For band II and III, the IP3 requirements are easy to predict. For band I, where the intermodulation tones are a CW tone and another WCDMA signal, it is not as direct to compute, and in the end is less critical than the specified band II and III conditions. With two narrow-band tones on the antenna port and the gain not yet reduced, the required intermodulation products must be lower than –105 dBm at the antenna port as previously determined. With the inputs at –47 dBm, the required IP3 referenced to the antenna port is –18 dBm. Reflected to the ADC input, this is +22 dBm assuming a conversion gain of 40 dB. Realistically, there can be other more stringent tests. In the case of a wideband (multicarrier) receiver architecture as proposed here, it is likely that signals as large as –30 dBm are processed by the analog section of the receiver, if only at the band edge. In this case, the numbers would need to be recomputed but would need to take into account the reduction of gain and the increase in system noise. From the ADC perspective, equivalent IP3 performance is in excess of +40 dBm and not a factor; therefore, IP3 is solely contributed from the downconverter block. In the case where higher conversion gain is used, IP3 requirements, as well as noise requirements, scale appropriately. Likewise, design specific margins increase the required performance above the minimums previously shown.

Component selection: Based on the previous discussion, the downconversion block must have a conversion gain of about 40 dB, a noise figure of 3 dB, and an output IP3 of at least +22 dBm. Current receiver technology is capable of this level of performance. Furthermore, room exists to further enhance performance beyond the minimum performance shown here with little effort.

Synthesizer: A number of suitable synthesizers are available for this design. As shown in Figure 1, these include the ADF4106 ultralow noise PLLs and the ADF4360-xfamily of integrated synthesizers and VCOs. The ADF4360 family of synthesizers is well suited for WCDMA Rx and Tx applications as proposed here.

ADC: As discussed in the previous sections, the converter needs an SNR of about 74 dBFS with a –3 dBFS input signal. Analog Devices has a number of converters that meet this requirement as well as new parts in various stages of development. For IF sampling, products such as the AD9446, AD9445, AD9444, and AD9246 are some of the latest announced devices. Existing devices include the AD9244, AD9245, AD9248, and AD6645.

For baseband sampling, the AD9238 and AD9248 dual, 12-bit and 14-bit converters are available. These devices are pin compatible and allow assembly options for platforms that may be common between single and multicarrier applications and where export/import restrictions may exist. In addition to these pin-compatible devices, new quad ADCs are available, including the AD9228 and AD9229. These quad, 12-bit converters are ideal for diversity baseband IQ sampling or for quad, low IF sampling applications such as phased array antennas.

DDC: The AD6636 offers a 4-channel or 6-channel DDC option. Each of these devices has four ADC inputs and, therefore, is easily configured as either diversity, diversity sectored, or phased array. Two ADCs can drive one of these devices to form a diversity two-(4-channel) or three-(6-channel) carrier receiver. One interesting configuration is shown in Figure 5. This application shows a three-sector, four-carrier antenna downconverted and digitized. The digitized signal is then passed to two different DDCs. Each DDC is then used to select and filter two FAs for a total of four FAs per sector. In addition to four diversity FAs per sector, this configuration provides redundancy in the event of a failure. Since each antenna is routed to two DDCs, the failure of a DDC does not take out an entire channel. Likewise, the diversity antenna is routed to two different DDCs providing redundancy there as well. In addition, the diversity signal path is handled by a completely different signal path from the main, providing as much as a four-way redundancy for signal processing. Therefore, in the event of the failure of the main path, the diversity path is totally redundant and not effected by the main path failure. Using this architecture, each sector is 100% covered by redundancy (RF through channelization) in the receive path regardless of the loss. The system is not reliant on any one single component and has a high degree of ability to reallocate channel capacity to other DDCs, in the event of a failure or even increased traffic volume.

In addition to the channelization capabilities, other functions are provided in the DDCs. The first is power estimation. The mean square power, peak power, and the number of times the signal crosses a specified amplitude can be measured for each ADC input. Additionally, when used in complex mode (I and Q), these measurements are done on the complex signals as well. This information can be used in conjunction with attenuation in the front end to prevent overloading in case strong signals are detected. Additionally, each DDC channel has an rms power measurement function with programmable integration for flexibility. This function can be used to set receiver gain, determine loop loss, and generate a digital output AGC function to keep the digital output bits in a narrow dynamic range for use with low bit precision rake receivers.

Other key features include dc offset correction, IQ gain adjustment, IQ phase adjustment, and complex digital tuning. All of these features are required when implementing IQ sampling for multicarrier applications.

Integrated functions: Currently, 14-bit ADCs are under export restriction to key countries. The AD6654 provides integration of the ADC and DDC function by combining the AD6645 and AD6636 cores in a single device. This device is classified as a receiver function and is not subject to export control. In addition to this, combined Rx functions are available that integrate both transmit and receive in a single package. Devices such as the AD9863 include dual, high speed ADCs and DACs suitable for

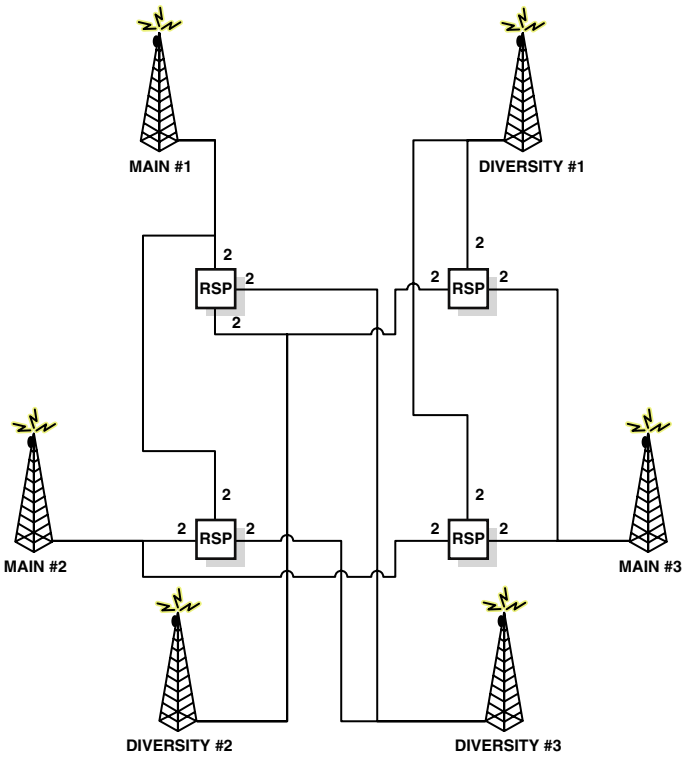

Figure 5.

single carrier applications. This device is an excellent option for low capacity systems. Other devices, which offer a variety of bit precisions and speeds for many options are available in this family (AD986x).

Validation: As seen in the following simulator output, with a minimum sensitivity signal of –121 dBm on the input, this receiver supports an SNR of over 8 dB with a gain of 40 dB, more than enough to meet the requirements for a wide area BS. This sensitivity can be maintained up to a total inband power level of about –36 dBm at the antenna. Beyond this, the input must be attenuated to prevent overdriving the receiver chain. The easiest way to meet the specification is to insert an attenuator to reduce the input signal level at the input of the receiver. While 6 dB would be ideal, additional attenuation can be used as long as the end sensitivity meets the –115 dBm specification. This is the case under the alternate channel blocking test at –40 dBm.

Table 2 below shows the resulting SNR when the conversion gain is changed allowing for modest increases in the NF. As seen, while the SNR changes slightly, it should be remembered that the desired signal level increases by 6 dB, thereby increasing SNR by 6 dB above that shown in the table.

Validation of SFDR sensitivity is a little more difficult. However, clearly for a linear system, CW testing is more stringent than testing with a WCDMA signal. Therefore, if a CW signal at the ADC input is driven to the ADC full scale of +4 dBm (–24 dBm CW at the antenna with 28 dB of conversion gain), worst case spurious should be better than 81 dB lower. WCDMA signals of equivalent peak power produce much lower spurious results due to the much lower spectral density and rms level of the stimulus signal. Typical minimums of 14-bit converters are specified at 85 dB or better depending on frequency. If 83 dB minimum is used (2 dB above the required), this is a CW SFDR power level of –79 dBm. After the rake receiver, this produces a spectral density of –144.8 dBm/Hz at the ADC or at the antenna of –172.8 dBm/Hz, about 8 dB lower than thermal after accounting for front end thermal noise. Therefore, the total noise in the channel of interest is increased by less than 1 dB, reducing overall sensitivity during this condition to better than –118 dBm, leaving a 3 dB margin to meet the specification of –115 dBm. Since a CW signal was used to approximate the effects of the peak signal of a WCDMA waveform, it is expected that the actual rms power of a realistic waveform is to be as much as 12 dB lower, thus achieving significant improvements in the SFDR performance of the receive channel over that expected by a CW tone.

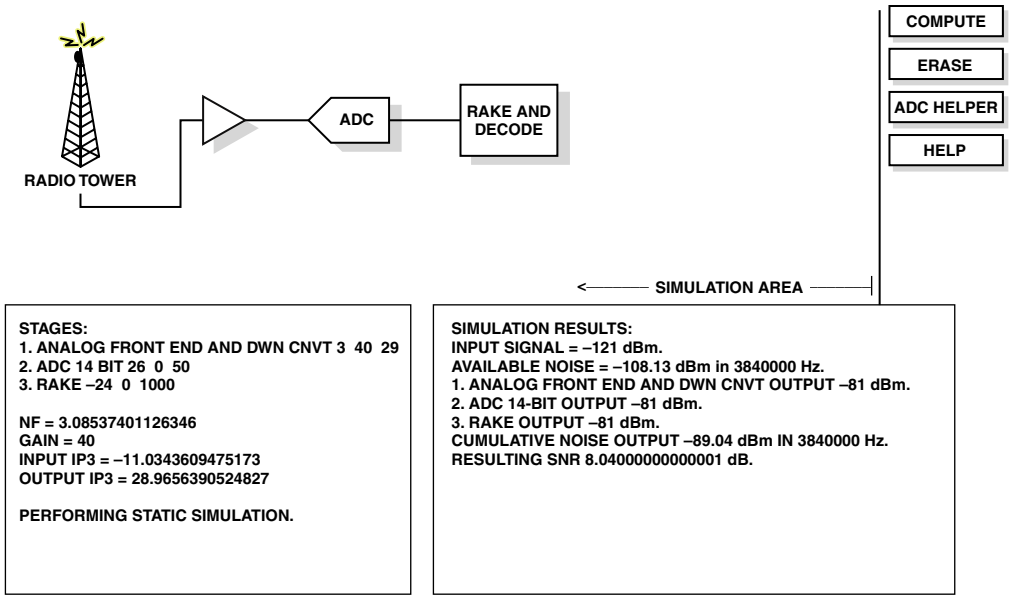

Figure 6.

Table 2.

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40 dB	3 dB	129 dB	3.1 dB	8	–36 dBm
34 dB	6 dB	125.88 dB	6.25 dB	4.88	–30 dBm
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*This number is –115 dBm for blocking conditions. The numbers in this table do not represent this increase in signal.

Noise margin for four carriers: Ideally, the basestation should seek to maintain a relatively low input level for each frequency allocation. Typically, this would be maintained somewhere between –60 dBm and –70 dBm depending on how the controller is programmed. Under these conditions, each carrier should have an SNR of around 60 dB providing excellent BER without the need to engage the gain reduction from the AGC loop. However, to be compliant with the specification, the adjacent and first alternate channels must be considered for the case where they may be outside the control of the base station or where they become large for some unforeseen reason.

For this condition, the desired sensitivity is –115 dBm, indicating that the gain can be reduced by the AGC loop. The impairing signals consist of the alternate signal at +63 dBc (–52 dBm) and the first alternate at +75 dBc (–40 dBm). Since these signals have only one code of modulation, the peak to rms is about 3.5 dB, resulting in a peak power of –36 dBm, which is at the upper limit of the highest gain setting. Given signal chain variations and power from other inband signals, it is assumed that the gain is reduced to the 34 dB setting, increasing the NF to 6.25 dB. In this condition, the desired signal should be processed with an available channel SNR of about 10.88 dB, resulting in a low BER. As discussed earlier, the addition of spurious energy from the large first alternate signal should be near the thermal noise level and have little impact on signals at this increased level.

TRANSMIT DISCUSSION

There are several options for the architecture of the transmit signal path. The factors that impact transmit signal elements are discussed first, followed by a discussion of the different architectures. Figure 7 shows a direct conversion architecture for an initial point of reference only. Section 6 of 3GPP TS 25.104 describes the transmit signal requirements. Throughout all of the architectures to be discussed, there is an assumption that there is a channel filter at the output of the power amplifier that is sharp enough so as not to desensitize the receive path and to ensure spurious emissions, when colocated, are filtered sufficiently.

Frequency error: The specification mandates that the same source is used for RF frequency and data clock generation; this implies that with a 3.84 Mbps data rate, all IF and RF frequency sources should have 3.84 MHz as an integer divisor. As a consequence, converter sample rates of 30.72 MSPS, 61.44 MSPS, 76.8 MSPS, 122.88 MSPS, and 245.76 MSPS, which represent multiplication factors of 8, 16, 20, 32, and 64 are common in WCDMA applications.

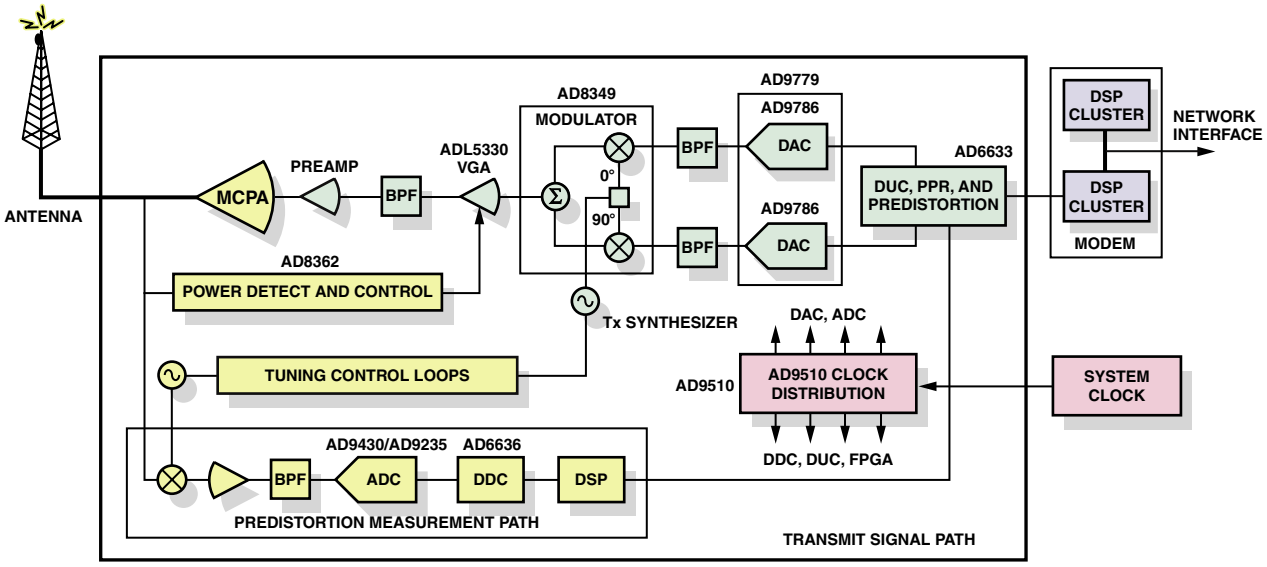


Figure 7.

Power control: The maximum output power is defined as the mean power level per carrier measured at the antenna. For a wide area base station this should be greater than 38 dBm with an integration bandwidth of 3.84 MHz. The specification allows for power control to be applied to each carrier at the antenna output, and on a code channel basis for user quality of service control.

The per carrier power control needs to have a minimum of 18 dB dynamic range. For a system using a single carrier per DAC, the dynamic power control is best placed in a VGA, in order to optimize the dynamic range requirements of the DAC. For a multicarrier system in which there is a common power control setting for all carriers, this should be adjusted in the VGA. It is possible that all but one carrier of a multicarrier system can be 18 dB below the single carrier (see Figure 8); if the spectral performance for a single carrier and for multiple carriers each at maximum dynamic power can be achieved, this scenario would not stress the DAC's dynamic range requirements any further. The dynamic range can be incorporated into the DAC's requirements, however, this would increase the dynamic range requirements of the DAC. (This is a possibility with high dynamic range DACs such as the AD9786 and AD9726, but for the following analysis it is assumed that an analog VGA will be present.)

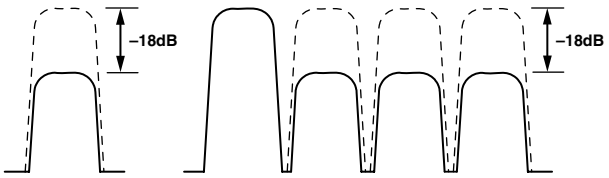


Figure 8.

When closed loop power control is implemented the base station keeps lowering a code channel's power until the user equipment (UE) detects an increase in the error rate. The UE closes the loop with the base station and in such a way maintains a specified quality of service. Inner loop power control is the base station's part of the closed loop code channel power control and the specification mandates a 1 dB step size with a range of ±12 dB in extreme conditions and ±9 dB for normal conditions. This power control is performed at the code channel level, before the composite carrier is formed. If the code channels required for UE synchronization (P-CPICH, P-SCH, S-SCH, PCCPCH) are used, the power level of the code channel has only a small effect on the composite carrier's peak-to-average ratio (PAR), and hence, marginally negligible effect on the dynamic range requirements of the analog downlink blocks.

Peak-to-average ratio (crest factor): The power amplifier that drives the antenna has opposing performance metrics when considering efficiency and linearity. The amplifier is most efficient when driven into saturation, but also has its worst linearity in saturation, conversely an amplifier driven for linearity is highly inefficient. Typically, a compromise is found between linearity and efficiency. This results in amplifiers that are operated in a mode where the average operating point is set such that the signal crests are just less than the maximum saturated output power that the amplifier can deliver. Determining and maintaining the PAR and power amplifier linearity is one of the largest challenges in a WCDMA base station.

Before channel combination, data and control streams (not synchronization channels) are mapped to QPSK symbols and spread with the OVSF spreading code assigned to that data stream channel, this provides the orthogonality/separation between data streams. The complex spread symbols are then multiplied by a base station specific scrambling code, ensuring signal separation between base stations. The primary and secondary synchronization channels (P-SCH, S-SCH) provide radio frame and time slot synchronization and are now combined with the spread data and control streams. This composite waveform is usually pulse shaped in nature to form a band-limited waveform. This waveform, depending upon the number of users and type of information being transferred can cause very high PAR waveforms if the component signals add in phase. Combining a 5 MHz carrier with other 5 MHz carriers further increases the probability of phase alignment, and increases the PAR. The increased PAR lowers the efficiency of the power amplifier if a certain level of linearity is to be maintained. As the PAR is heavily dependent upon the traffic in the channel, a representative test mode has been established for conformance tests, test model 1. This test model can have 64 data streams, or dedicated physical channels (DPCH), at a 30 kSPS data rate with a spreading factor of 128, and is randomly distributed across the code space at random code domain power levels and random timing offsets.

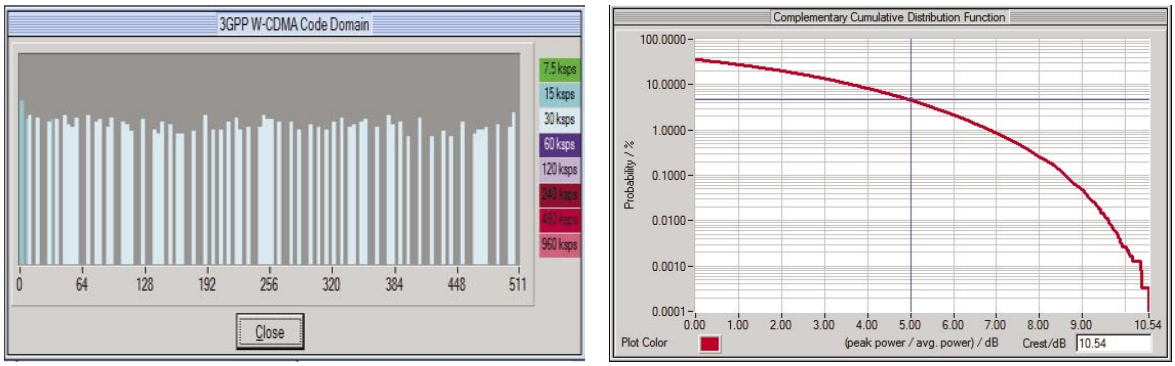


Figure 9.

Figure 9 shows the DPCH distribution within the code domain. To help determine the PAR of this single carrier, the user can look at the complementary cumulative distribution function (CCDF), which shows the probability of a peak happening within this frame. A common metric of acceptability is the 10^{-4}% probability level; peaks with lower probability than 10^{-4}% contribute very little to the actual intermodulation performance of the amplifier and are usually handled by either allowing the amplifier to go into saturation or by clipping within the digital processing. For the single carrier case, using Test Model 1, a peak to average ratio of approximately 10.5 dB results for a 10^{-4}% probability. As previously mentioned, if multiple carriers are combined with little attention to the resulting PAR, the resulting PAR could be very high. To mitigate this, carriers can be encoded with different spreading codes and time offsets, which helps to reduce the phase alignment of the carriers. Figure 10 shows this effect for four carriers, each with Test Model 1 channelization, yielding 4.5 dB of reduction in PAR with appropriate choice of scrambling code and time offset. It should be noted that using different spreading codes and time offset results in a four carrier PAR, which is only 0.6 dB higher than the single carrier PAR.

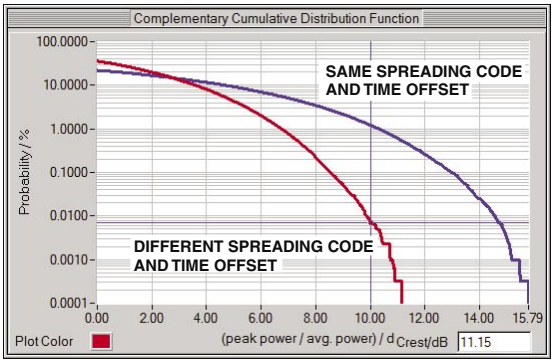


Figure 10.

Peak-to-average power reduction: The more the PAR can be reduced, the higher the average power can be made for the same efficiency. Peak-to-average power reduction techniques (PAPR) can be used that reduce peaking without introducing out-of-band distortion. The typical method of PAPR is clipping followed by filtering. Clipping has the negative impact of significantly reducing the EVM performance and creating new spectral signals that must be filtered. The AD6633 provides PAPR without clipping the baseband or IF signals. It uses a technique that introduces inband distortion selectively to reduce the peaks without causing distortion in adjacent bands. This allows EVM to be directly traded off with compression and without adjacent channel distortion. Additionally, in multichannel applications, the amount of EVM can be allocated differently for each carrier, facilitating quality of service differentiation between carriers. For example, voice carriers can be allocated a higher EVM in favor of high speed data carriers that need lower EVM for the higher data rates. This cannot be accomplished by clip and filter techniques. Figure 11 demonstrates the performance of the AD6633 with four equal power carriers; the uncompressed sum exhibits peaks approximately 6 dB greater than the compressed sum in the displayed time slot. The CCDF shows that for a 10^{-4}% probability, approximately 6 dB improvement is realized. Generally, the more carriers used, the greater the reduction in PAR for a given probability.

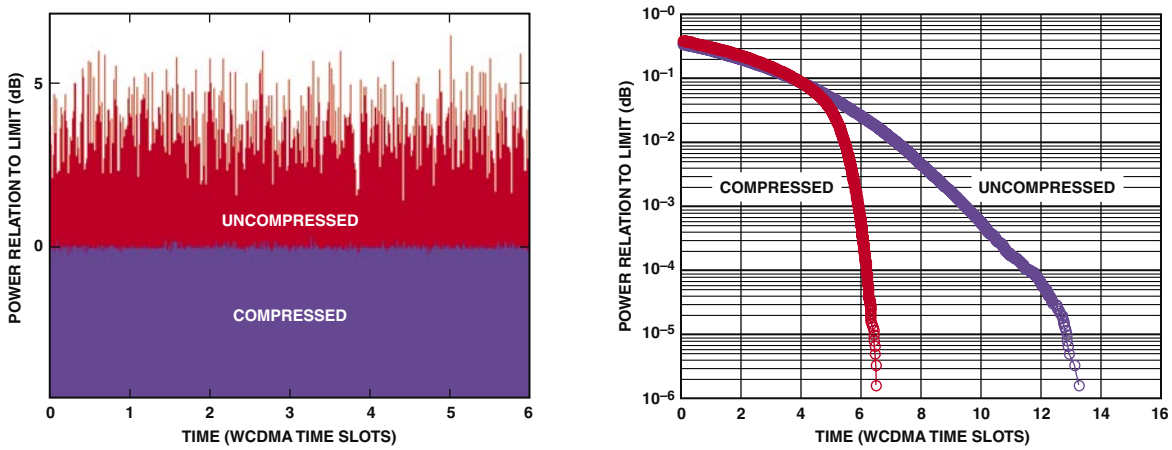


Figure 11.

Power amplifier linearization: Another method for increasing the efficiency of the power amplifier is to allow the amplifier to move closer toward saturation, hence increasing efficiency, but also compensating for the resulting distortion that results. There are two main approaches to PA linearization. Analog feedforward uses linear feedforward compensation amplifiers around the main power amplifier to counter the distortion problems and provide sufficient linearity so that spectral regrowth does not pollute adjacent channels. This approach typically results in efficiencies less than 10% and is a complicated, but tractable, analog problem where the feedforward amplifiers' linearity also need to be considered.

A second approach to PA linearization comes in the form of digital predistortion. This method uses the simple concept that a digital numerical representation is very linear and highly predictable, with no effect from environmental operating conditions. Thereby, if the transfer function of the PA can be determined, summation with an equal and opposite transfer function (see Figure 12) results in a highly linear system response which introduces no noise or distortion. Furthermore, the manufacture of the analog feedforward amplifiers is no longer needed and a cheaper digital process can be used.

The impact on the converters for a system implementing digital predistortion should be considered. The forward path is considered first, see Figure 12. Any signal passed through a power amplifier is disturbed in two ways; firstly, additive noise is introduced to the signal, and secondly, a nonlinear PA transfer function leads to odd-order intermodulation products. For a WCDMA signal these effects lead to spectral regrowth in the adjacent and alternate channels. Third-order intermodulation products cause spreading of the distortion over three times the bandwidth of the carrier; fifth-order intermodulation gives fives times the bandwidth, and seventh-order intermodulation gives seven times the bandwidth. For a single carrier, having a wanted channel bandwidth of 3.84 MHz, third-order distortion occupies a band between 1.92 MHz and 5.76 MHz either side from the center of the wanted channel (see Figure 14). This

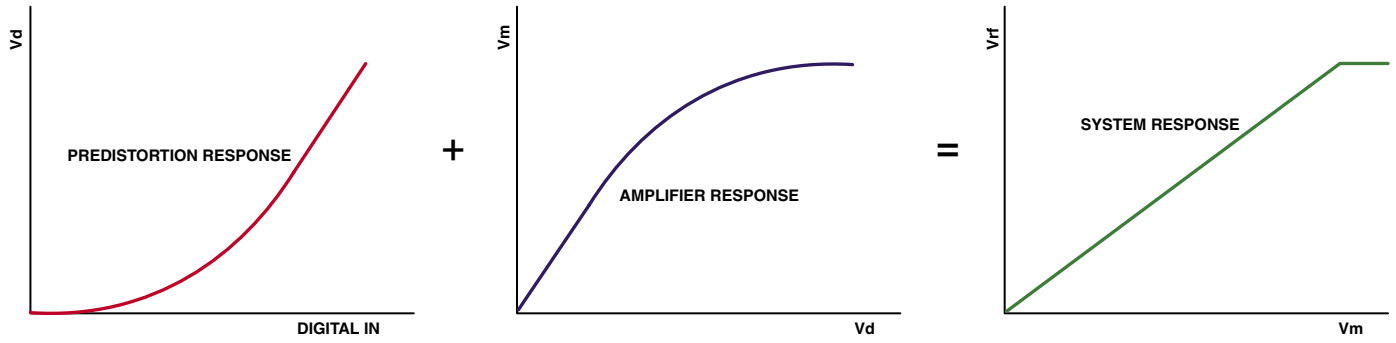


Figure 12.

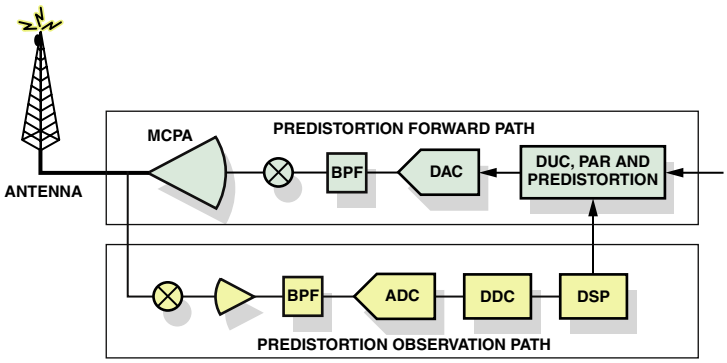


Figure 13.

appears in the adjacent channel together with the additive broadband noise. The first alternate channel is unaffected by third-order intermodulation but is still affected by the broadband noise. Similar consideration of the fifth- and seventh-order intermodulation products shows an additional channel is affected with increasing order of intermodulation. With four carriers, the distorted signal bandwidth is now 18.84 MHz. Consequently, third-order intermodulation now affects a band 9.42 MHz to 28.26 MHz from the center of the signal bandwidth; third-order intermodulation affects significantly more alternate channels. Additionally, for a fixed DAC IMD performance, as more carriers are added there is more energy in the alternate channel, which reduces the ACLR by the factor $10\log_{10}$(#carriers) relative to the single carrier case. Recall that the intent of digital predistortion is to create *antidistortion*, a system employing digital predistortion needs $10\log_{10}$(#carriers) more IMD performance relative to the single carrier case to maintain the same ACLR as the single carrier case. Additionally, control over a bandwidth 3×, 5×, or 7× the signal bandwidth is required to completely null out third-, fifth-, or seventh-order intermodulation products. In the case of four WCDMA carriers (signal bandwidth 18.84 MHz), control over a bandwidth of 131.88 MHz is required if seventh-order IM products are of interest, with an additional 6 dB better IMD performance compared to the single carrier case.

In the observation path, a sample of the RF output signal is mixed down and converted back to digital baseband data where it is compared to the transmitted data. In order to remove fast moving power profiles the downconverted signal is averaged over many hundreds of samples. The algorithms used to create the corrected transfer function can be based on either a polynomial multiplication or on a look-up table. A DSP function can be used to implement the algorithm in which the downconverted and averaged result is compared to the transmitted signal to determine how much distortion was added by the forward path upconversion process. Once determined, the inverse distortion is computed and then used to modify the future look-up table or polynomial coefficients. The coefficient update can take seconds to complete and captures not only distortion due to power profiles of the carriers but also temperature and aging effects.

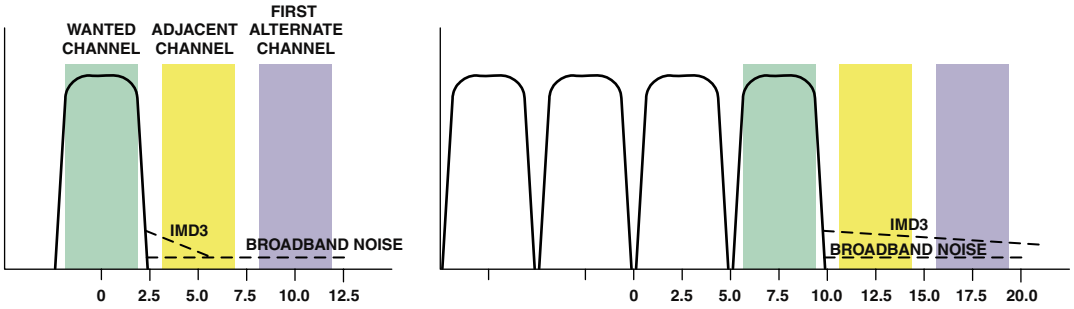


Figure 14.

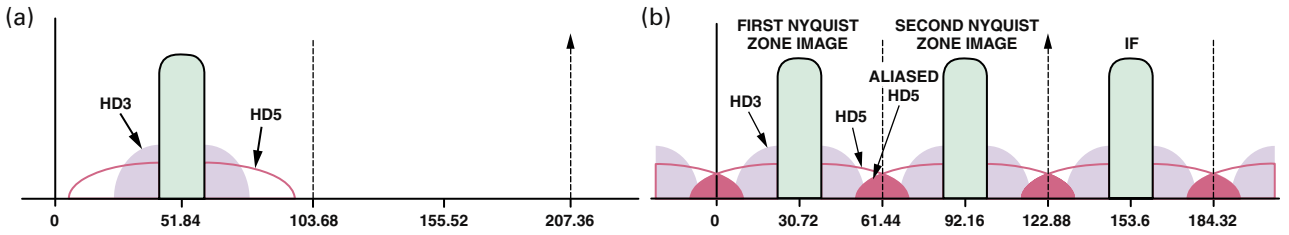


Figure 15.

There are a number of approaches to capture the distortion. One approach mixes the transmitted signal down close to dc and uses a high speed ADC to sample a bandwidth that is equal to the order of distortion times the bandwidth of the RF spectrum. A Nyquist band of 75 MHz and 100 MHz is required for three and four carriers respectively. Common sample rates of between 170 MHz and 210 MHz are used for this function (see Figure 15a).

An alternate approach mixes down to a low intermediate frequency (IF) and undersamples the transmitted signal. With this approach, the ADC samples the signal and the third-order distortion components without aliasing; the fifth- and higher order distortion terms are allowed to alias over the third-order terms and compensated by coefficient control (see Figure 15b). For four carriers at 153.6 MHz, a 122.88 MSPS converter is needed.

The ADC limitation is that it must introduce less distortion than the distortion being measured at the antenna and have a noise spectral density less than the antenna wideband emission requirements. The ADC noise can be averaged over multiple samples, relaxing the noise requirements of the ADC by the oversample ratio to typically 8 ENOB to 10 ENOB. The following discussion reveals a required noise level at 10 MHz offset is –30 dBm/1 MHz or –90 dBm/Hz. This level must be attenuated by typically 50 dB to reduce the maximum PA output to that of the ADC full scale; the directional coupler typically has about 40 dB of attenuation. Therefore, the spectral density at the ADC input is –140 dBm/Hz; across a 100 MHz Nyquist band, this corresponds to an ADC SNR of about 60 dB. The AD9430 provides mid 70s SFDR up to 200 MHz and an SNR of mid 60s, meeting these requirements.

ACLR: The importance of reducing the PAR of the composite signal has been highlighted above. Current literature suggests that a 20 dB ACLR improvement can be realized using PA linearization. The equation below links ACLR, PAR (ξ), and IIP3; it is valid for the first adjacent channel of a single carrier only. As previously mentioned, multiple carrier ACLR can be rationalized back to single carrier requirements by adding $10\log_{10}$(#carriers).

$$ACLR = -20.75 + 1.6\xi + 2(P_{IN} - IIP3) \quad (1)$$

For the DAC, the intercept point is related to the output and Equation 1 reduces to

$$ACLR = -20.75 + 1.6\xi - IMD(dBc) \quad (2)$$

What Equation 2 does not capture is the effect of the noise floor on the ACLR. Figure 16 is a sweep of the channel power for a single WCDMA carrier with Test Model 1 for the AD8349. With channel powers down to about –15 dBm, the ACLR equation holds true with the AD8349 exhibiting an approximate +18 dBm IP3. As the channel power drops, the ACLR begins to become dominated by the noise, and the ACLR degrades.

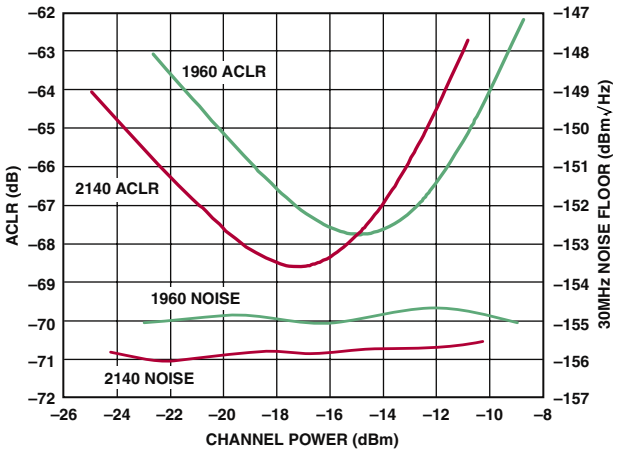


Figure 16.

The case for a wide area base station with 30 W maximum output power, four carrier generic solution is presented next. In Figure 17, a simplified block diagram for the upconversion (mixer + synthesizer), VGA, and PA is used.

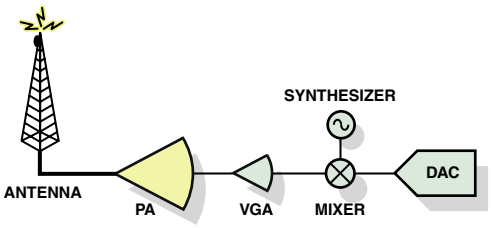


Figure 17.

Out-of-band emissions: Out-of-band emissions are unwanted emissions immediately outside the channel bandwidth resulting from the modulation process and nonlinearity in the transmitter but excluding spurious emissions. Section 6.6.2.1 of the 3GPP specification details an emissions mask.

Consider first the single carrier case. Assume Test Model 1 is being used, having a PAR of 10.5 dB; PAPR is being used and recovers 6 dB of the PAR; a 3 dB overhead is

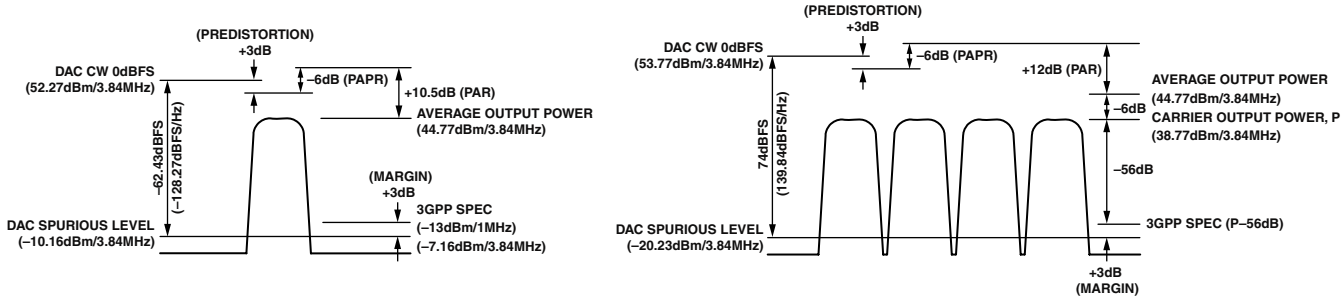


Figure 18.

assumed in the DAC to handle predistortion. This establishes the peak power at the output of the PA and also the full scale of the DAC for dynamic range calculations. The 3GPP specification has spectral emissions requirements based on the output power per carrier. For the single carrier case –13 dBm in an integration bandwidth of 1 MHz is specified. Allowing 3 dB of margin on the specification requires spurious content to be no greater than –910.16 dBm in a 3.84 MHz bandwidth. For this case the DAC needs a dynamic range of 128.27 dBFS/Hz. Furthermore, the frequency offset that this spurious is specified for covers the adjacent channel, hence an ACLR of 55 dB is needed.

Now consider the four carrier case. For the same total average output power, the carrier's output power is 6 dB lower. The PAR is also a little higher than the single carrier case, pushing the peak power up to 53.77 dBm. As the carrier power is lower, there is a different emissions specification: 56 dB below the carrier. With the same 3 dB margin on the emission specification, the DAC spurious level is established at –20.23 dBm. This effectively increases the dynamic range requirement of the DAC to 139.84 dBFS/Hz, but more importantly, the adjacent channel ACLR is now required to be 59 dB.

Spurious emissions: This part of the specification broadly covers how the channel affects other radios, including this base station's receiver. There is frequency separation between this base station's transmitter and receiver; there is also separation between this base station's transmitter and potentially another base station colocated operating in a different frequency band. The amount of frequency separation is greater than 100 MHz, allowing for a duplexer's filter transition band. However, the duplexer does not have a great deal of attenuation 10 MHz away from the band and the specification has requirements for 10 MHz away from the transmit band. If a single carrier is placed at the band edge, illustrated in Figure 19a, there is a requirement for –30 dBm/1 MHz 10 MHz away from the carrier. This would represent the second alternate channel, which is usually dominated by broadband noise for a single carrier. If multiple carriers are used, the –30 dBm/1 MHz requirement is still present (see Figure 19b), but in this case it is possible that third-order distortion could pollute this band.

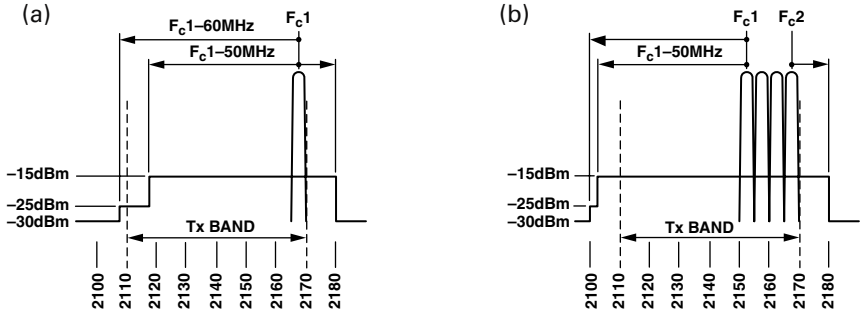


Figure 19.

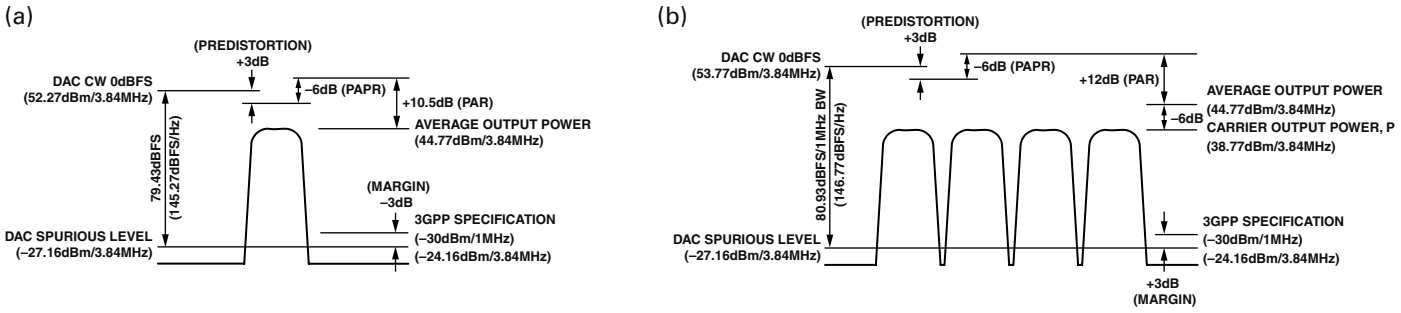


Figure 20.

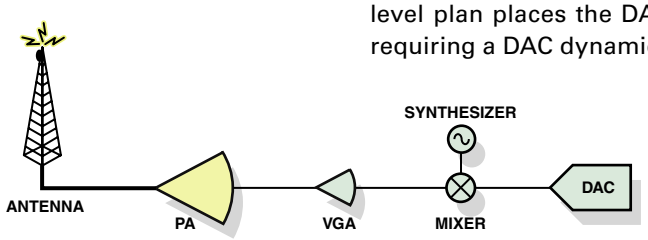
The single carrier case (see Figure 20), has the same peak level as previously discussed; now there is a requirement of –30 dBm/1 MHz, which if the same 3 dB margin is used requires no spurious be greater than –27.16 dBm/3.84 MHz. As this frequency offset is too close to the carrier for any filter transition band to be effective, this requirement sets the minimum broadband noise requirement, and the ACLR requirement of the alternate channels to be almost 72 dB.

For the four carrier case, the peak level is higher than the single carrier case, which when coupled with the low spurious requirement sets the DAC minimum dynamic range requirement of 146.77 dBFS/Hz. This requirement also increases the four carrier alternate ACLR requirement to almost 66 dB.

The minimum adjacent channel ACLR requirements are set by the out-of-band emissions requirements. The four carrier requirement of 59 dB can be referred back to a single carrier requirement by adding 6 dB; allowing 1 dB for the summation of broadband noise within the adjacent channel yields a requirement of 66 dB adjacent channel ACLR for a single carrier. The alternate channel ACLR requirements are derived from the spurious emissions specifications. Here the requirements are set by the single carrier case at 72 dB.

Assume that Test Model 1 has a PAR of 10.5 dB and that PAPR reduces the PAR to around 4 dB. Also assume that PA linearization is being used, giving a 10 dB improvement in OIP3 of the PA. If a mixer/modulator similar to the AD8349 is used, it likes to have an output channel power of around –15 dBm. If the single carrier power control is done in the VGA, this requires a minimum of 18 dB range; allocating 20 dB gain to the VGA requires a gain of 40 dB in the PA to deliver approximately +45 dBm from the output of the DAC. Commercially available PAs and VGAs with these characteristics exhibit a noise figure of around 2 dB. Calculating the cascaded OIP3 at the output of the PA gives +70.92 dBm; if the preceding stages are assumed distortion free, the cascaded OIP3 results in an adjacent channel ACLR, due to intermodulation of 66.18 dB.

To achieve the 72 dB of alternate channel ACLR with the VGA and PA noise and gain, the total noise at the output of the mixer needs to be around –156.8 dBm/Hz. It is possibly easier to get lower noise from the DAC than from the mixer and synthesizer, so the larger burden of low noise is placed on the DAC, the remainder split between the mixer and the synthesizer. The noise contribution in the adjacent channel now needs adding to the odd order distortion in the adjacent channel, which for these levels brings the adjacent channel ACLR to 66.04 dB. The above level plan places the DAC full-scale output at –3 dBm, requiring a DAC dynamic range of –160 dBFS/Hz.



PA			VGA			MIXER			DAC			SYNTHESIZER	
OUTPUT POWER	45		OUTPUT POWER	45		OUTPUT POWER	–15		OUTPUT POWER	–15			
INPUT POWER	5		INPUT POWER	5		INPUT POWER	–15		INPUT POWER	–15			
GAIN	40		GAIN	40		GAIN	0		GAIN	0			
IIP3	34		IIP3	34		IIP3	17		IIP3	29			
OIP3	74		OIP3	74		OIP3	17		OIP3	29			
NF	2		NF	2		NSD	–158		NSD	–163		NSD	–159
									IMD3	70		5MHz OFFSET	
									PAR OVERHEAD	12			
OVERALL OIP3	70.92								0dBFS (dBm)	–3			
ACLR DUE TO IP3	–66.18		OVERALL ACLR (ADJ)		–66.04				NSD (dBFS/Hz)	–160			
ACLR DUE TO NOISE	–71.97		OVERALL ACLR (ALT)		–71.97								

Figure 21.

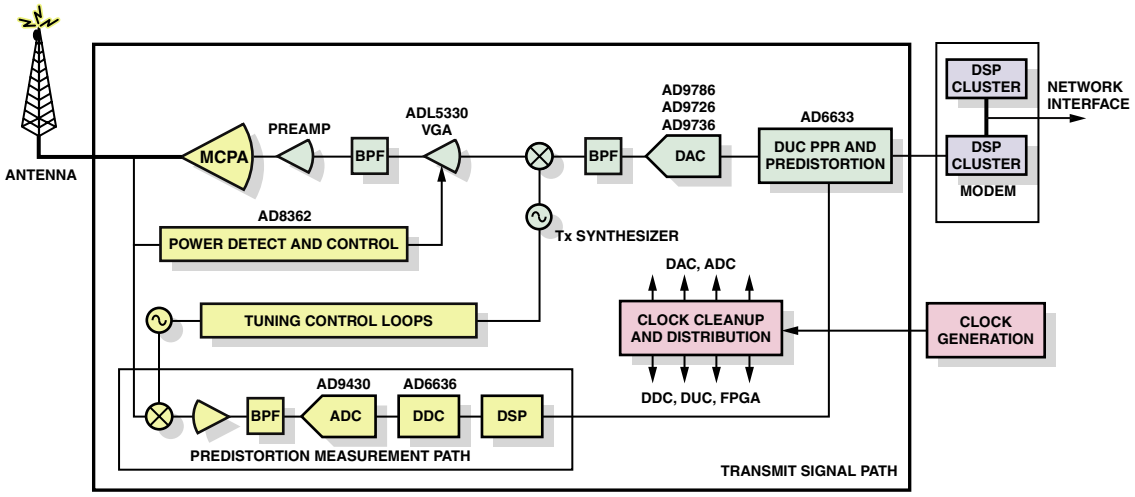


Figure 22.

Transmit modulation: The specification draws out two important metrics for determining the accuracy of the data. The peak code domain error (PCDE) and the error vector magnitude (EVM) are measures of how well the code channels have been spread and retained their orthogonality. The following two equations can be used to link PCDE and EVM back to PAR and ACLR, where SF is the spreading factor.

$$EVM = \frac{1}{\sqrt{PAR}} \times 10^{\frac{ACLR(dB)}{20}} \times 100 \qquad PCDE = 10 \log_{10}\left(\frac{EVM^2}{SF}\right)$$

The specification requires –33 dB for the PCDE, with a spreading factor of 256 and 17.5% EVM if QPSK modulation is being used, or 12.5% with 16 QAM. Normally, if the radio aspects of the specification are met, the code domain aspects are usually also met. For example, in the above radio design, the single carrier ACLR of –66 dB having a PAR of 4 dB would result in an EVM of 2.5% and a PCDE of –56 dB.

Superheterodyne single upconversion: Superheterodyne single upconversion relies on low noise, high performance IF output DAC technology, see Figure 22. If PA linearization is being used with correction for the fifth-order intermodulation products, five times the signal bandwidth is required, for four adjacent carriers this would require approximately 100 MHz. A convenient IF at the DAC output would be a decade away from the final RF frequency, 80 MHz to 200 MHz. There are many options to synthesize carriers at these frequencies; the first (see Figure 23a) uses a high sample rate Nyquist rate converter such as the AD9726 or AD9736. The update rate of the DAC, f_{DAC}, is the same as the input data rate, f_S; for sample rates above 250 MSPS LVDS data inputs should be considered. As the carriers in the first Nyquist zone increase in frequency, the second Nyquist zone images move lower, thus the higher the output carrier frequency for the same sample rate, the more aggressive the analog reconstruction filter needs to be. An alternative to the high speed LVDS inputs is to use lower speed CMOS inputs and interpolate the DAC output (see Figure 23b). This approach uses a digital low-pass filter to suppress the second and third input Nyquist zone image; the interpolation image is further suppressed by the analog reconstruction filter. For the same DAC update rate as the Nyquist rate DAC, the interpolating DAC has slightly less than half the usable bandwidth and produces an image which needs consideration. If an image of the input sample rate is needed, the interpolation filters can be operated in high-pass mode (see Figure 23c). The analog reconstruction filter requirements between the Nyquist and interpolation approaches for the same DAC sample rate are comparable with the interpolation approach suffering from the added interpolation image. For a fixed input sample rate the interpolation approach allows the analog reconstruction filter to be relaxed as the unfiltered image is pushed higher in frequency. The AD9772A is a good fit for 2× interpolation up to 320 MSPS update rate.

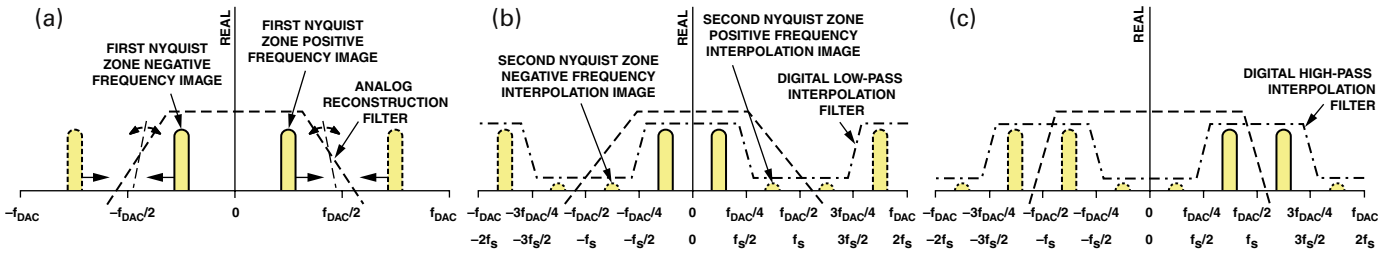


Figure 23.

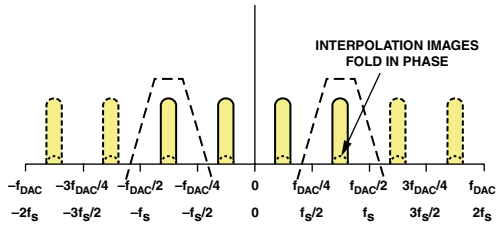


Figure 24.

Another approach to generate an IF signal is to digitally mix a baseband signal to an IF. A single DAC always outputs a real signal, it is mirror symmetrical about 0 Hz and multiples of $f_{DAC}/2$. Consequently, when a real signal is subjected to a real digital mix (see Figure 24) the negative frequencies move into positive frequency and interpolation images fold on top of the desired signal. Fortunately, the interpolation images are in phase with the desired signal and does not cause any distortion. This approach creates a congested spectrum requiring a band-pass filter to select the desired signal.

If a complex baseband is available, a complex interpolation is possible (see Figure 25a); a complex spectrum is now no longer mirror symmetrical around dc, but is still translationally symmetrical about f_S. With a digital complex mix (see Figure 25b) the entire complex spectrum undergoes a frequency shift, with no aliasing. However, the DAC can still only produce a real signal, so if the complex mix's output drives a single DAC, any asymmetric about dc spectrum potentially causes interpolation images to fold on top of the desired signal and be out of phase with the signal, causing distortion (see Figure 25c).

The AD9786 has a single DAC and can accept either a real or complex input, and do a complex mix, with the ability to reject interpolation images folding out of phase. The AD9777 and AD9779 are dual DAC devices with two channels of interpolation filtering and the ability to do either real or complex mixing; a single DAC's output can be used if a real output is needed, or the device can be operated as two single transmit chains for a two antenna diversity system. With the exception of the AD9777 and AD9772A, all mentioned DACs have approximately –160 dBm/Hz noise power spectral density and better than 70 dBc IMD over the desired frequency range; the LVDS input DACs are capable of producing at least a 300 MHz Nyquist band. The AD6633 can still be coupled to the AD9786, AD9777, and AD9779 to provide peak-to-average power reduction and fine frequency tuning. The AD6633 also has the ability to act as a control interface to a DVGA for power control.

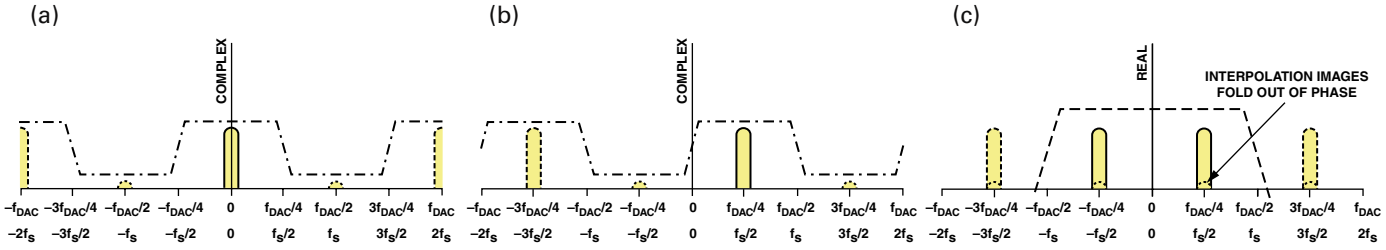


Figure 25.

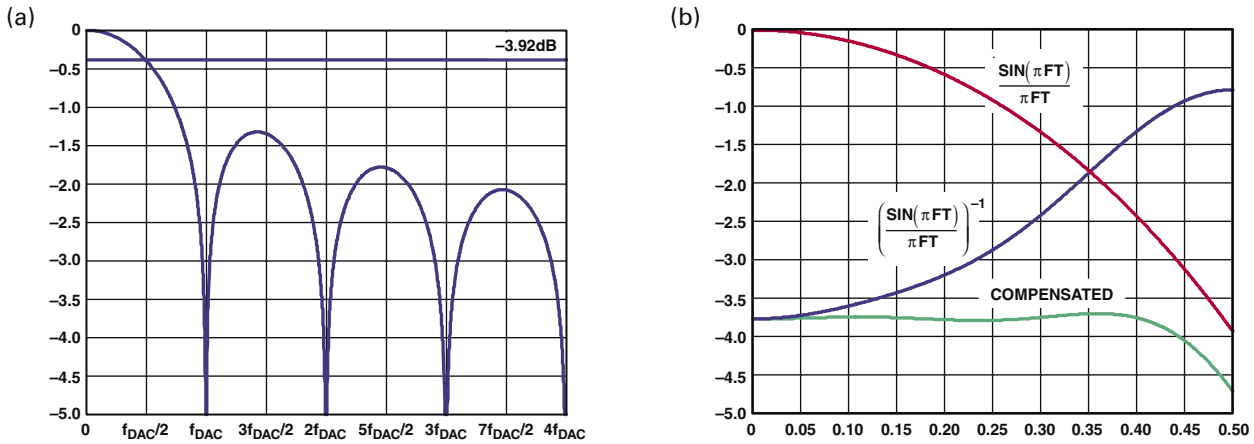


Figure 26.

If the DAC produces a high IF, the DAC's sin(x)/x response needs considering. The DAC has a zero order hold of the data, which produces a frequency domain response with a sin(x)/x characteristic (see Figure 26a). The response has deep nulls at multiples of the DAC sample frequency, f_{DAC}, and by half the DAC sample rate there is a 3.92 dB loss. This is important for multicarrier signals at high frequencies with respect to the DAC sample rate, as it causes inband roll-off that affects the EVM and PCDE; the effect is worst at higher output frequencies. The sin(x)/x response can be digitally compensated (see Figure 26b). An inverse sin(x)/x transfer function can be superimposed on the data such that when synthesized by the DAC the response is essentially flat. The disadvantage of this is that the final output signal is attenuated by approximately 4 dBFS and that the inverse sin(x)/x filter is only bound up to a fraction of the Nyquist rate (0.42 f_{DAC} in Figure 26a). Consequently, using images in higher Nyquist zones is usually not realizable with simple sin(x)/x filters. The sin(x)/x compensation can be implemented at almost any stage of the transmit path and if digital predistortion is being implemented, the overhead to add sin(x)/x compensation is trivial. If it is desired to do the sin(x)/x compensation in the DAC, the AD9779 has an inverse sin(x)/x compensation filter.

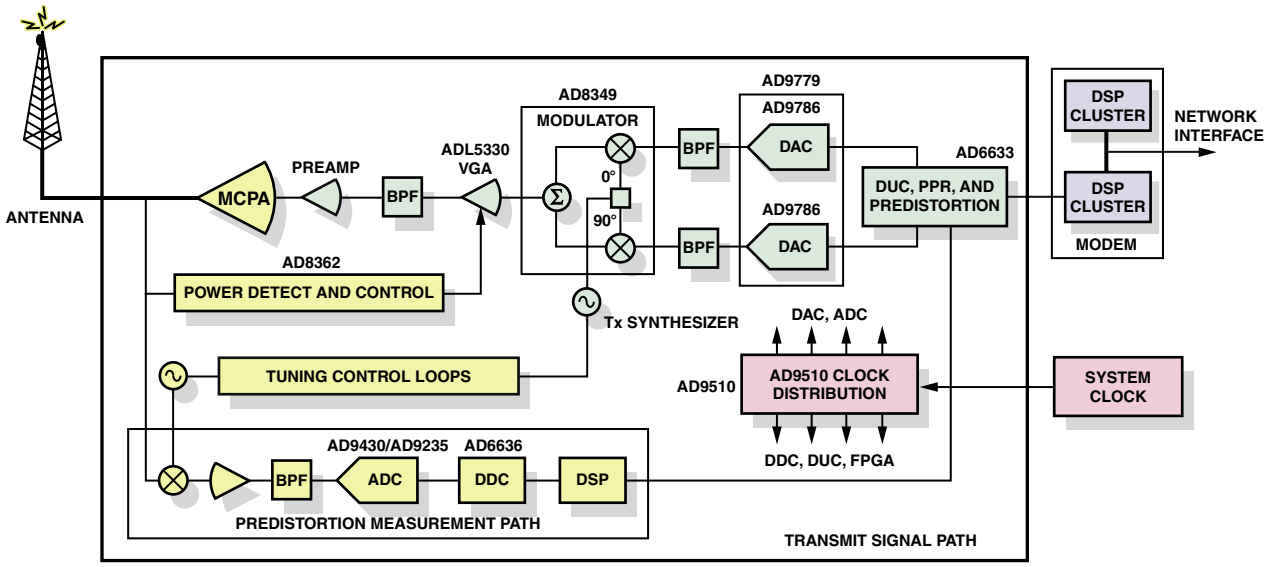


Figure 27.

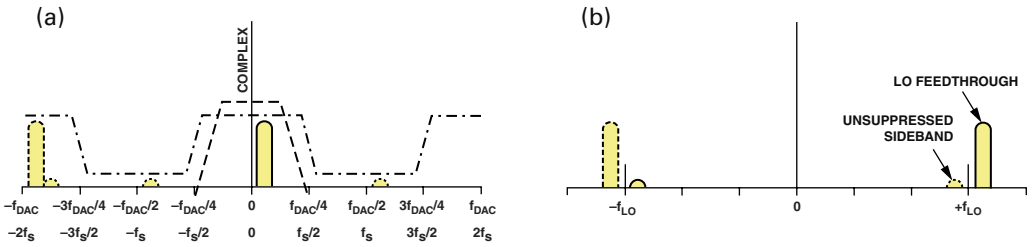


Figure 28.

Direct conversion: This technique is desirable for its simplicity, flexibility, and relative low cost of implementation. The carriers are synthesized by the DACs as a complex pair and then mixed to RF by a quadrature modulator; the action of the quadrature modulator is to do a complex frequency translation but only output the real component of the mix. The baseband carriers, Figure 28a, can either be centered on dc or offset from dc. The DAC outputs are filtered to remove any images before upconversion in the quadrature modulator (see Figure 28b). For an ideal quadrature modulator a perfect single sideband upconversion would result.

Nonidealities in the complex to real translation can lead to LO feedthrough and unsuppressed sidebands at the RF frequency. By using a low IF direct upconversion approach the LO feedthrough and unsuppressed images are moved away from the desired sideband, allowing them to be filtered. For an odd number of permanently on carriers, the carriers can be placed on dc, thereby minimizing the effect of unsuppressed sidebands and LO feedthrough. For an even number of carriers, which are permanently on, the carriers can be placed symmetrically around dc, in which case the LO feedthrough can appear as an adjacent interferer that is subject to emissions limitations. For any number of carriers that can be turned off, the frequency allocation of the turned off carrier can be filled with an unsuppressed sideband, which would also be subject to emissions limitations. The cause of the LO feedthrough and unsuppressed sideband can be compensated for. If a digital predistortion loop is being used, the correction can be part of that loop. Alternatively, the output of the quadrature modulator can be mixed back down to baseband and corrected independently.

There are two main error components that can cause poor sideband rejection. Figure 29a is an example of the effect of a quadrature gain error in the complex path's constellation. As one might expect, the nonideal constellation causes poor EVM and PCDE. To achieve sideband suppression in the 60 dBc to 70 dBc range, the quadrature gain error has to be less than a couple of tenths of a percentage point (see Figure 29b).

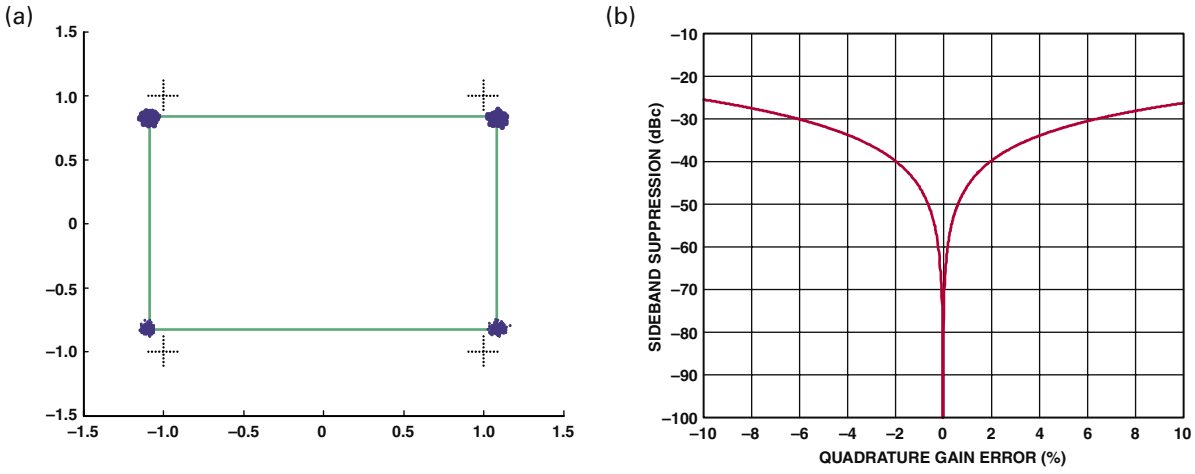


Figure 29.

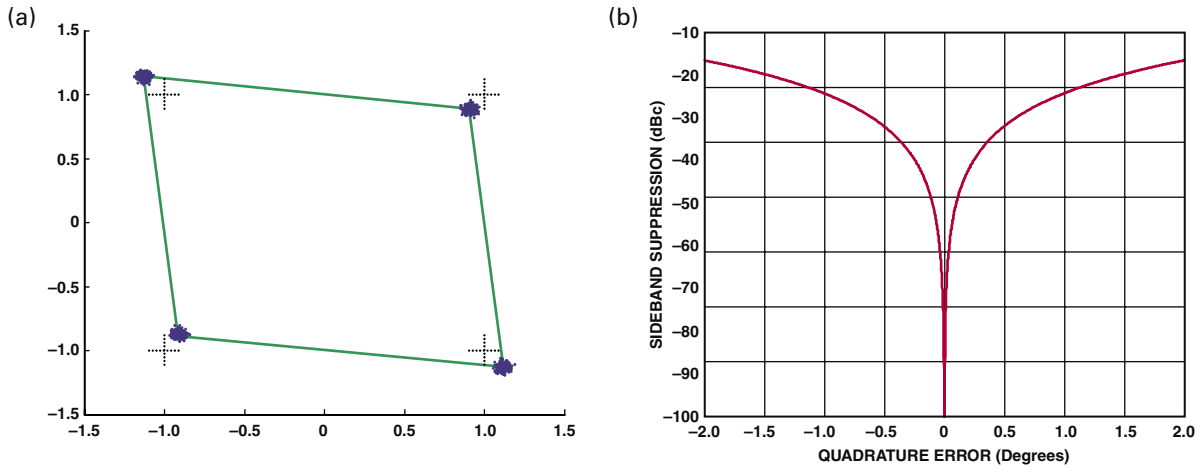


Figure 30.

The second main error component is quadrature phase errors. These errors tend to twist the constellation (see Figure 30a), degrading EVM and PCDE. To achieve sideband suppression in the 60 dBc to 70 dBc range, the quadrature phase error needs to be less than a couple of tenths of a degree, see Figure 30b.

The cause of LO feedthrough is predominantly due to quadrature offsets in the complex path. Offsets shift the origin of the demodulated constellation, see Figure 31a, degrading EVM. As LO feedthrough can also be produced by PCB coupling, Figure 31b, shows the degradation from an ideally matched quadrature path. LO feedthrough is subject to the emissions limitation and typically needs to be 70 dBc to 80 dBc below the total mean output power of the base station.

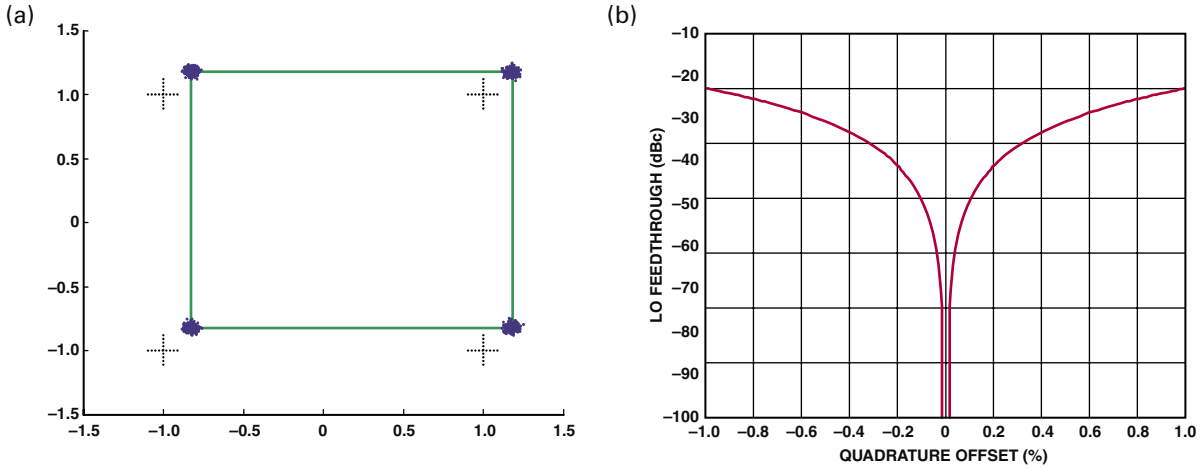


Figure 31.

Since modulators may only be rated to a sideband rejection of –40 dBc and 0.5 degrees of phase accuracy, and DAC outputs may only match to 1%, it is important to have the ability to adjust the IQ balance. This can be accomplished by either adjusting the baseband digital data or by adjusting the gain and offset of the DAC output. If done in the digital baseband, this may be part of the baseband predistortion or through a standalone routine. However, this can consume a peercentage of the total dynamic range of the DAC and modulator. Digital adjustment of the gain, offset, and phase can be done using the AD6633. The most suitable DAC to partner the AD6633 would be a pair of AD9786s, which have sufficient dynamic range that a few percent degradation should not affect system performance. Alternatively, one can select a DAC that includes gain and offset adjustment functions as is found in the AD9777 and AD9779. Using the AD9777 or AD9779 does not reduce the dynamic range of the DAC but requires a dynamic interface between the controller and the DAC control port. Additionally, the AD9779 has the ability to ac couple the DAC outputs to the modulator and still have offset adjustment on the modulator side of the ac coupling.

As proposed so far, the AD9777 or AD9779 and AD8349 are recommended for direct conversion architectures. In addition to the features and functions mentioned, these devices are optimized to work together by providing a smooth interface between devices, including matched common-mode input levels. Following the modulator, an RF VGA is typically used to maintain the PA output level as operating conditions change. The ADL5330 has a gain adjust range of 60 dB and is well suited to this application. In conjunction with the RF VGA, a power detector is required. Devices such as the AD8362 are matched to the power control range of this RF VGA with a detection range of 60 dB.

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