AN-742
APPLICATION NOTE

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Frequency Domain Response of Switched Capacitor ADCs

by Rob Reeder

INTRODUCTION

Knowing the frequency response of unbuffered analog-to-digital converters (ADCs) with a switched capacitor front end is an important first step in understanding how to design an interface to these types of pipeline ADCs. The characteristic input impedance that the ADC exhibits must be determined before designing any high frequency interface, regardless of whether the interface is active, passive, dc-coupled, or ac-coupled.

This application note develops a method, using measurements made with a network analyzer, to provide a better understanding of the input response over high frequency ranges. This method allows users to design a more effective interface to unbuffered converters with switched capacitor inputs. All measurements and model calculations were made using the AD9236 in a 32-lead lead frame chip scale package (LFCSP).

The internal, sample-and-hold amplifier (SHA) circuit within the converter is mainly composed of an input switch, an input sampling capacitor, a sampling switch, and an amplifier. As Figure 1 shows, the input switch interfaces the driver circuit with the input capacitor. When the input switch is on (track mode), the driver circuit drives the input capacitor. The input is sampled (captured) on the input capacitor at the end of this mode. When the input switch is off (hold mode), the driver is isolated from the input capacitor. The track mode period and the hold mode period of the converter are approximately equal.

The interface problem with an unbuffered (switched capacitor) converter is seen as two fold: the frequency domain response, which this application note presents, and time domain response. The first issue is that the input impedance during the track mode of the SHA is different from the input impedance during the hold mode of the SHA. This input impedance change between track and hold mode makes it difficult to accurately impedance match the converter input with the front-end circuit for high intermediate frequencies (IF) designs. Because the converter samples at the input signal only during the track mode, the input impedance must be matched for this mode. The frequency dependence of the input impedance is governed mainly by the sampling capacitor and any parasitic capacitance in the signal path. For accurate impedance matching, it is helpful to have an idea of the frequency dependence of the input impedance. The measurement results obtained from the AD9236 explain the behavior of the input impedance over a wide range of input frequencies. The Example section describes how to interface with the AD9236 while in track mode.

The second issue lies in the time domain where the internal switched capacitor front end introduces kickback into the driver circuit. This problem occurs when the converter switches from one mode to the other, charging the input capacitors from the previous sample to the current sample. Therefore, the current glitch occurring at the input of the converter is dependent on three factors: the difference between the previous and the current samples, the value of the input sampling capacitor, and the sum of all resistances in the signal path. The sum of all resistances comprises the on resistance of the switches in the signal path and any series resistance in the signal path as well.

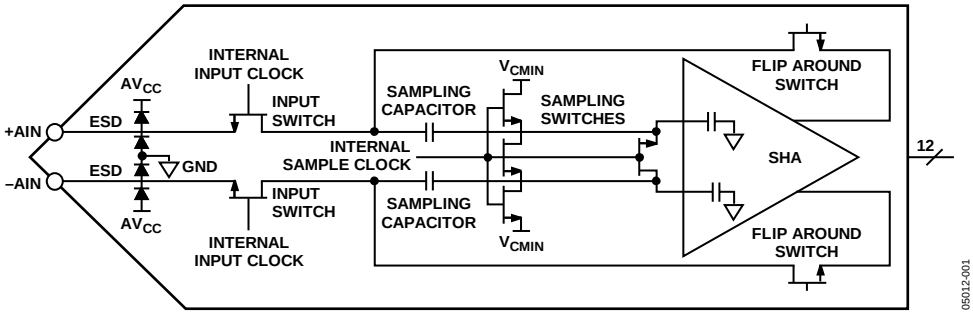

Figure 1. Unbuffered Converter Input Front-End Model

TABLE OF CONTENTS

REVISION HISTORY

6/2018—Rev. B to Rev. C

Changes to Introduction Section 1
Moved Figure 1 1
Added Time Domain Section 3
Changes to Measurements Section and Results Section 5
Changes to Example Section 6
Changes to Converter S Parameters Section and References Section 7

TIME DOMAIN

A time domain example of a current glitch seen at the analog input pin is shown in Figure 2 and Figure 3. Figure 4 shows the frequency domain content of the current glitch of the entire network, in this case, on the primary side of a transformer coupled network.

If the nonlinear portion of the current glitch corrupts the input sample when the driver has a linear response, the resulting sampled signal distorts. Therefore, it is crucial to design an input network (that is, a transformer or amplifier driver) capable of settling the current glitch within a half-clock cycle to preserve converter performance.

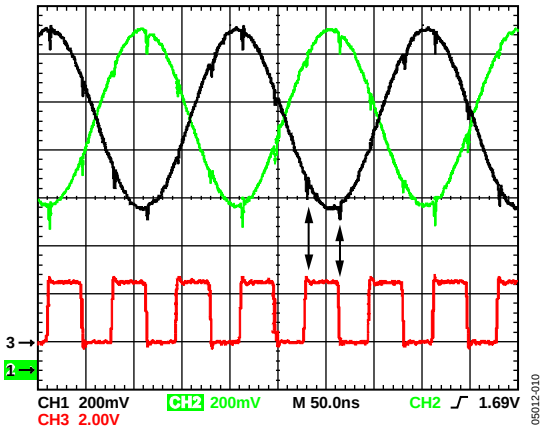

Figure 2. Single-Ended (+AIN or –AIN) Time Domain Measurement at the Analog Input Pins

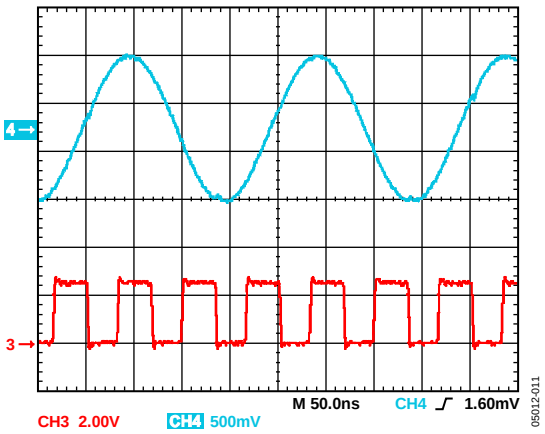

Figure 3. Differential (+AIN or –AIN) Time Domain Measurement at the Analog Input Pins

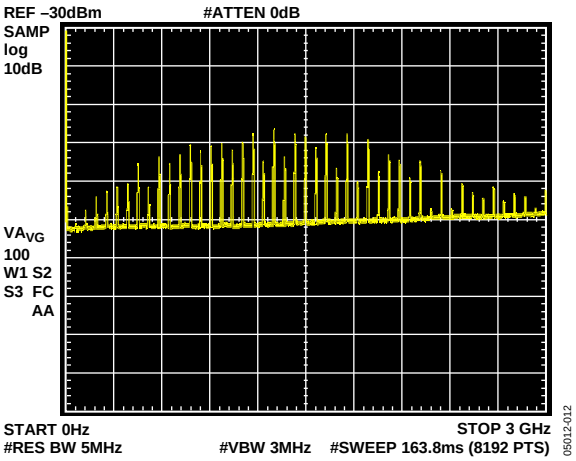

Figure 4. Frequency Domain Measurement of the Entire Network

METHOD

To understand converter frequency response, the internal front end of an AD9236 was measured accurately using a network analyzer. A special AD9236 evaluation board was redesigned to keep the input traces short and to minimize as many board parasitics as possible. The evaluation board was biased at nominal supply voltages and clocked at 1 MSPS.

Figure 5 shows the timing setup used to ensure that the network analyzer sampled during the track mode. The duty cycle of the clock was set to 90% to provide leeway for converter input settling and network analyzer capture delays. The same setup was used to take measurements during the hold mode, except that the clock was inverted, as shown in Figure 6.

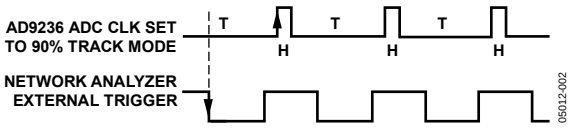

Figure 5. Timing Diagram Setup—Track Mode

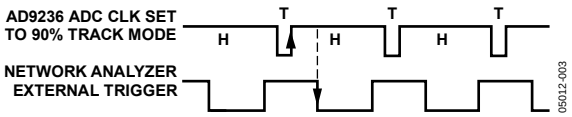

Figure 6. Timing Diagram Setup—Hold Mode

The measurement setup is shown in Figure 7. The network analyzer was configured to capture 1601 points over a 300 kHz to 1 GHz frequency range. A 2-channel pulse generator with matched cables was used to strobe the evaluation board and external trigger of the network analyzer at the same time. Power supplies were applied to properly bias the converter and provide a common-mode voltage of 1.5 V (AVDD/2) to each analog input.

Measurements were made on the evaluation board, and also on an error board, which is a portion of the evaluation board containing the same trace parasitics seen by the ac coupling capacitor, and two common-mode resistor dividers that develop the common-mode voltage on the analog inputs. The error board data is used to deembed the errors caused from these sources, allowing the ADC input structure to be measured independently (see Equation 1).

Evaluation Board (Parasitics + AD9236) – Error Board (Parasitics) = Evaluation Board (AD9236) (1)

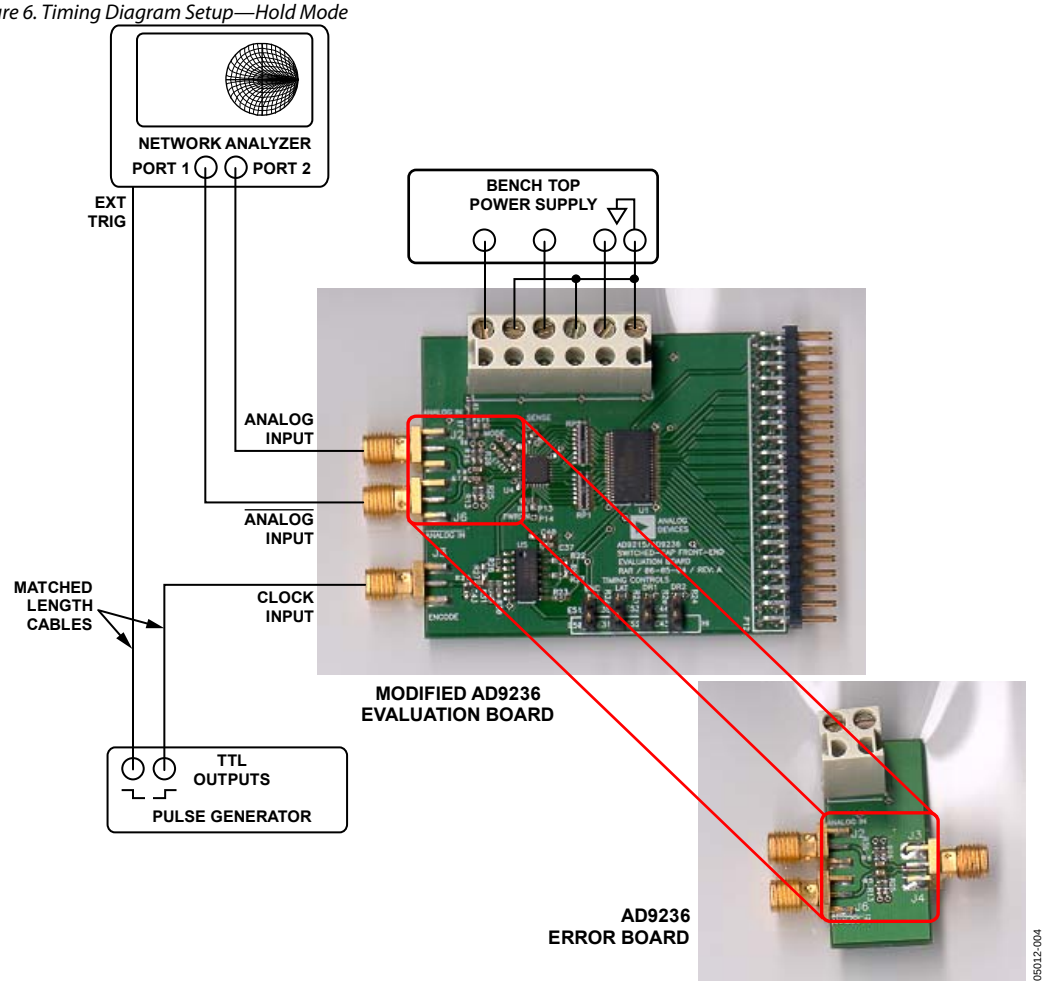

Figure 7. Converter Input Impedance Measurement Setup

MEASUREMENTS

The measurements taken are in single-ended form. Due to the limited capabilities of the network analyzer, a common method of converting these measurements from single-ended to differential was used. The following equation converts a single-ended measurement to differential by using the LogMag scattering parameters (S parameters) S11, S12, S21, and S22 from the network analyzer.

$$T_S = \frac{(2 \times S11 - S21)(1 - S22 - S12) + (1 - S11 - S21)(1 + S22 - 2 \times S12)}{(2 - S21)(1 - S22 - S12) + (1 - S11 - S21)(1 + S22)} \quad (2)$$

A differential impedance is derived by taking Equation 2 a step further, as shown in Equation 3. Equation 3 produces the equivalent parallel real and imaginary impedance (Z_{DIFF}) circuit from the series type measurement.

$$Z_{DIFF} = 50 \times ((1 + \tau) \times (1 - \tau)) = R \pm jX \quad (3)$$

Using the advanced design system (ADS) software simulation package from Agilent Technologies, data was exported from the network analyzer, converted to differential, and the common-mode component error was subtracted out (see Figure 8).

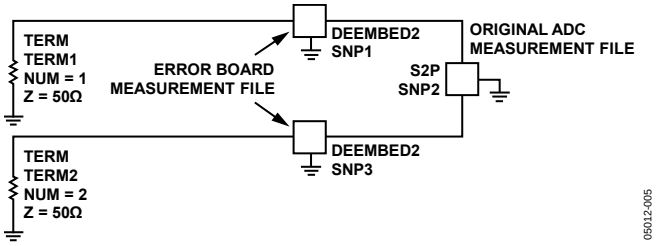

Figure 8. ADS Configuration Setup

RESULTS

The results of these computations show real and imaginary components in both track and hold modes. The values that represent the real impedance of the internal sampling network in ohms are located on the left side of Figure 9. The values that represent the imaginary or capacitive impedance in pF are located on the right side of Figure 9.

In track mode (at low frequencies), the real component of the internal sampling network in ohms appears high impedance, settling to roughly 700 Ω at 200 MHz. Referring to the converter input model of Figure 1, the input impedance is approximately equal to the resistive equivalent of the series parallel combination of transistors in the track mode. The imaginary impedance of the internal sampling network in ohms starts at 4 pF at 200 MHz, rolling off to 1.5 pF at 1 GHz. These values are to be expected because the input stage during the track mode is the sum of the series parallel combination of the parasitic capacitance transistors. In hold mode, the real component of the internal sampling network in ohms of the impedance is much higher, dropping to roughly 570 Ω at 1 GHz. The imaginary impedance of the internal sampling network in ohms, however, quickly falls to 1 pF or less throughout the entire measurement range, as was expected for the ESD and package parasitics. These package parasitics are due to the input structure resembling an open circuit (as shown in Figure 1).

Figure 10 shows an expanded view of Figure 9 that depicts the usable impedance matching range.

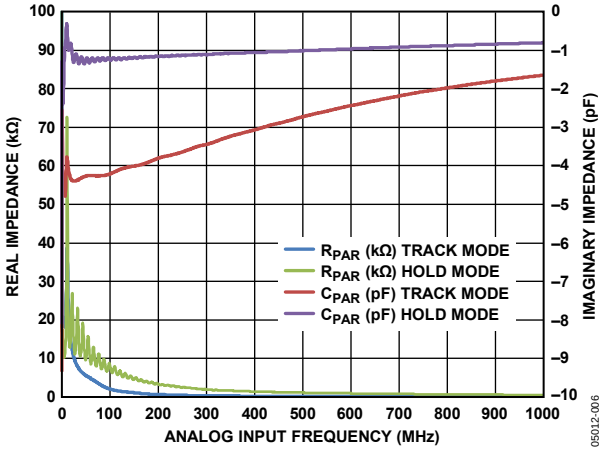

Figure 9. Differential Input Impedance vs. Analog Input Frequency

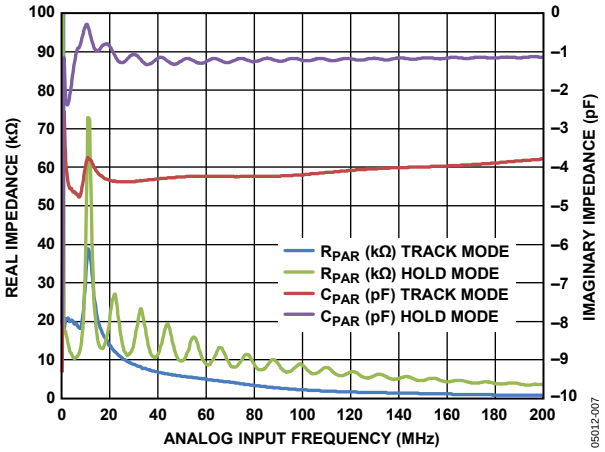

Figure 10. Differential Input Impedance vs. Analog Input Frequency (Expanded)

EXAMPLE

This section provides an example of how to interface with the AD9236 using a transformer coupled input based on the measured results. With an analog input frequency at 120 MHz, the AD9236 resembles a 1.57 kΩ differential resistor and 4.1 pF capacitor during the track mode. If the input impedance is designed to 50 Ω, then one implementation is represented as shown in Figure 11.

Other advantages gained from using this circuit topology when designing interface circuits for switched capacitor ADCs include keeping distortion products low by having a matched differential input termination, as well as high common-mode rejection from switching transients (note the two 33 Ω series resistors). In addition, a capacitor value is determined based on the amount of bandwidth required for a particular application. For this example, a 2 pF was chosen to reduce any wideband aliasing noise seen by the converter.

The key is to make the input look as real as possible when designing at high IFs. Because the input is capacitively dominated, the goal is to find a matching inductive term to cancel the imaginary impedance. The math involved to complete this operation using complex terms is as follows:

$$X = \frac{1}{2p120M4.1p} = -j323\ \Omega,$$

$$X = \frac{1}{2p120M2p} = -j663\ \Omega$$

$$(1.57k - j0) \,||\, (0 - j323\ \Omega) = (64 - j310)\ \Omega$$

$$(64 - j310) \,||\, (0 + j663) = (29.5 - j213.33)\ \Omega$$

where:
X_{CI} is the impedance of 4.1 pF or 1/(2 × π × 120 MHz × 4.1 pF).
p is pico or 10×10^{-12}.
M is mega or 10×10^{6}.
X_{C2} is the impedance of 2.0 pF or 1/(2 × π × 120 MHz × 2 pF).
k is kilo or 10×10^{3}.

Set X_L = 213 Ω and solve for inductance (L) at 120 MHz; this L equals 283 nH.

After solving for L, divide the L value equally and place the inductor in series with the 33 Ω resistors on the secondary of the transformer as shown in Figure 11. Note that the 33 Ω value depends on the converter used for the design. For optimum spurious performance, see the suggested values in the AD9236 data sheet.

Add all of the components together to find the resulting impedance seen at the secondary of the transformer. Remember, the L is added in, canceling out the capacitive term and making the input appear real.

$$(29.5 - j213.33) + (66 + j213.33) = 95.5\ \Omega$$

The transformer has a 1:1 impedance ratio. Therefore, 95 Ω is the impedance seen at the primary of the transformer in parallel with the 105 Ω resistor. These two resistors in parallel further yield the 50 Ω termination, 95 || 105 = 50 Ω.

With the converter internal sampling network S parameters available a better expectation of the preceding filter or load termination of the amplifier is defined as this example shows. These S parameters allow the designer to minimize the load mismatches, which result in gain and roll-off variations in the pass band. Ultimately, it is these types of variations that cause noise and distortion, degrading the expected performance of the converter.

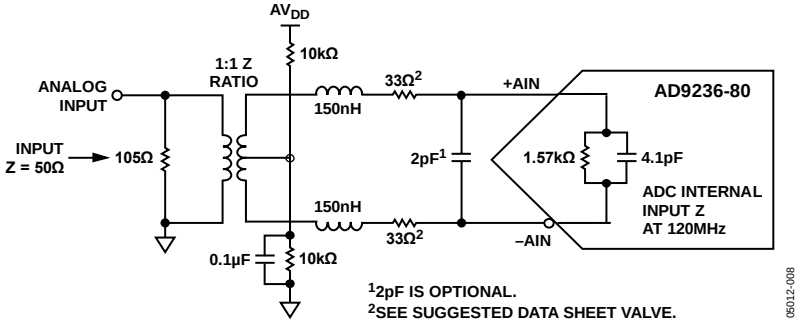

Figure 11. Impedance Matching Example

An exaggerated example of a particular filter response is shown in Figure 12. Note that the frequency response of the filter changes as the load termination changes. The following simple illustration gives the designer an idea of what to expect when designing the front-end interface without further compensation.

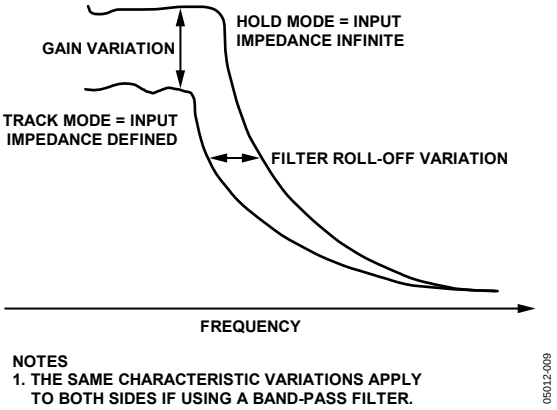

Figure 12. Illustrated Filter Response Due to Load Variation

CONCLUSION

This application note provides some background on internal front ends of unbuffered, switched capacitor, pipeline converters. A method of measuring the varying input imped-ance of the track-and-hold circuit is also shown as well as an example of how to resolve an input interface when using this type of converter at high IF frequencies (>70 MHz). Remember to match the impedance for the front-end design in track mode and design for the center IF frequency band.

When using the converter at 70 MHz and below (baseband), a simple low-pass filter is adequate. Matching the front-end interface is not as critical at lower frequencies to achieve optimal performance when using an unbuffered converter.

The data and example presented here is specific to the AD9236 in a LFCSP package, describing the general behavior of the ADC family of switched capacitors. Other unbuffered, switched capacitor devices also include the AD9204, AD9212, AD9215, AD9219, AD9222, AD9228, AD9233, AD9235, AD9236, AD9237, AD9238, AD9244, AD9245, AD9246, AD9248, AD9251, AD9252, AD9258, AD9268, and AD9287.

CONVERTER S PARAMETERS

S parameter data is available at www.analog.com. Visit a product page, such as the AD9236 product page, to download the spreadsheet that contains both the real and imaginary data values in both series and parallel. These values are in tabular format and plotted against frequency.

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AN05012-0-6/18(C)