Differential Drivers for High Speed ADCs Overview

DIFFERENTIAL DRIVER BASICS

Many high performance ADCs are now being designed with differential inputs. A fully differential ADC design offers the advantages of good common-mode rejection, reduction in second-order distortion products, and simplified dc trim algorithms. Although they can be driven single-ended, a fully differential driver usually optimizes overall performance.

The reduction in second-order distortion products inherent in differential designs can be illustrated as follows. The distortion products are modeled by expressing the transfer functions of the circuit as a power series.

Taking a generic expansion of the outputs and assuming matched amplifiers, we get:

$$V_{OUT+} = k_1(V_{IN}) + k_2(V_{IN})^2 + k_3(V_{IN})^3 + \ldots \quad \text{Eq. 1}$$

$$V_{OUT-} = k_1(-V_{IN}) + k_2(-V_{IN})^2 + k_3(-V_{IN})^3 + \ldots \quad \text{Eq. 2}$$

Taking the differential output:

$$V_{OUT+} - V_{OUT-} = 2k_1(V_{IN}) + 2k_3(V_{IN})^3 + \ldots \quad \text{Eq. 3}$$

where k_1, k_2 and k_3 are constants.

The quadratic terms gives rise to second-order harmonic distortion, the cubic terms gives rise to third-order harmonic distortion, and so on. In a fully-differential amplifier, the odd-order terms retain their polarity, while the even-order terms are always positive. When the differential is taken, the even order terms cancel as shown in Eq. 3. The third-order terms are not affected.

One of the most common ways to drive a differential input ADC is with a transformer. However, there are many applications where the ADCs cannot be driven with transformers because the frequency response must extend to dc. In these cases, differential drivers are required. In cases where significant signal gain is required ahead of the ADCs, differential amplifiers offer a good solution. Although providing "noiseless" voltage gain, transformers with turns ratios greater than two generally suffer from bandwidth and distortion issues, especially at IF frequencies.

A block diagram of the AD813x and ADA493x family of fully differential amplifiers optimized for ADC driving is shown in Figure 1. Figure 1A shows the details of the internal circuit, and Figure 1B shows the equivalent circuit. The gain is set by the external resistors R_F and R_G, and the common-mode voltage is set by the voltage on the V_{OCM} pin. The internal common-mode feedback forces the V_{OUT+} and V_{OUT-} outputs to be balanced, i.e., the signals at the two outputs are always equal in amplitude but 180° out of phase per the equation,

$$V_{OCM} = (V_{OUT+} + V_{OUT-}) / 2. \quad \text{Eq. 4}$$

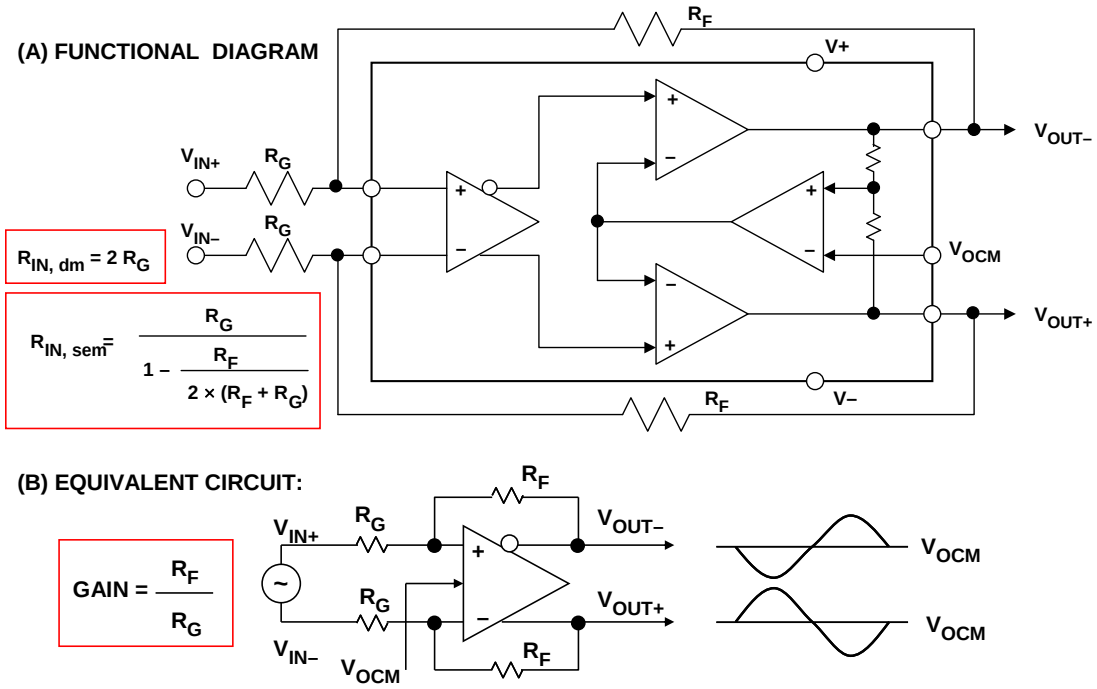
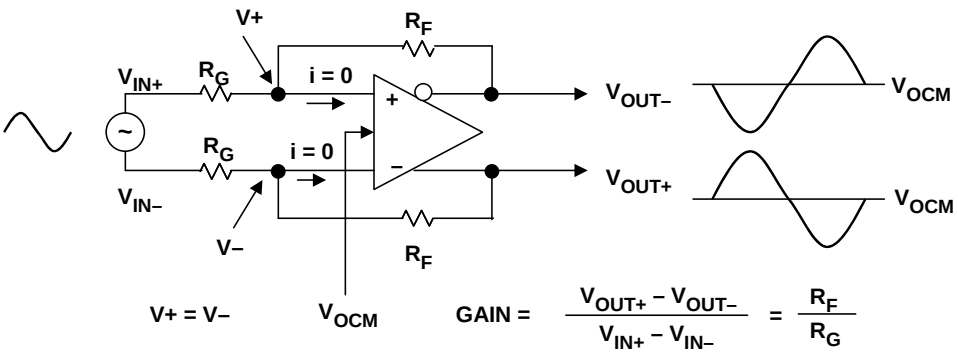


Figure 1: AD813x, AD493x Differential ADC Driver Functional Diagram and Equivalent Circuit

The AD813x and ADA493x uses two feedback loops to separately control the differential and common-mode output voltages. The differential feedback, set with external resistors, controls only the differential output voltage. The common-mode feedback controls only the common-mode output voltage. This architecture makes it easy to arbitrarily set the output common-mode level in level shifting applications. It is forced, by internal common-mode feedback, to be equal to the voltage applied to the V_{OCM} input, without affecting the differential output voltage. The result is nearly perfectly balanced differential outputs of identical amplitude and exactly 180° apart in phase over a wide frequency range. The circuit can be used with either a differential or a single-ended input, and the voltage gain is equal to the ratio of R_F to R_G.

The circuit can be analyzed using the assumptions and procedures summarized in Figure 2. As in the case of op amp circuit dc analysis, one can first make the assumption that the currents into the inverting and non-inverting input are zero (i.e., the input impedances are high relative to the values of the feedback resistors). The second assumption is that feedback forces the non-inverting and inverting input voltages to be equal. The third assumption is that the output voltages are 180° out of phase and symmetrical about V_{OCM}.



- + and – input currents are zero
- + and – input voltages are equal
- Output voltages are 180° out of phase and symmetrical about V_{OCM}
- Gain = R_F/R_G

Figure 2: Analyzing Voltage Levels in Differential Amplifiers

Even if the external feedback networks (R_F/R_G) are mismatched, the internal common-mode feedback loop will still force the outputs to remain balanced. The amplitudes of the signals at each output will remain equal and 180° out of phase. The input-to-output differential-mode gain will vary proportionately to the feedback mismatch, but the output balance will be unaffected. Ratio matching errors in the external resistors will result in a degradation of the circuit's ability to reject input common-mode signals, much the same as for a four-resistor difference amplifier made from a conventional op amp.

Also, if the dc levels of the input and output common-mode voltages are different, matching errors will result in a small differential-mode output offset voltage. For the G = 1 case with a ground-referenced input signal and the output common-mode level set for 2.5 V, an output offset of as much as 25 mV (1% of the difference in common-mode levels) can result if 1% tolerance resistors are used. Resistors of 1% tolerance will result in a worst case input CMR of about 40 dB, worst case differential mode output offset of 25 mV due to 2.5 V level-shift, and no significant degradation in output balance error.

The effective input impedance of a circuit, such as the one in Figure 2, at V_{IN+} and $V_{IN–}$ will depend on whether the amplifier is being driven by a single-ended or differential signal source. For balanced differential input signals, the input impedance ($R_{IN,dm}$) between the inputs (V_{IN+} and $V_{IN–}$) is simply:

$$R_{IN,dm} = 2 \times R_G \qquad \text{Eq. 5}$$

In the case of a single-ended input signal (for example, if V_{IN-} is grounded, and the input signal is applied to V_{IN+}), the input impedance becomes:

$$R_{IN,sem} = \left(\frac{R_G}{1 - \frac{R_F}{2 \times (R_G + R_F)}} \right) \quad \text{Eq. 6}$$

The circuit's single-ended input impedance is effectively higher than it would be for a conventional op amp connected as an inverter, because a fraction of the differential output voltage appears at the inputs as a common-mode signal, partially bootstrapping the voltage across the input resistor R_G.

Figure 3 shows some of the possible configurations for the AD813x differential amplifier. Figure 3A is the standard configuration which utilizes two feedback networks, characterized by feedback factors β1 and β2, respectively. Note that each feedback factor can vary anywhere between 0 and 1.

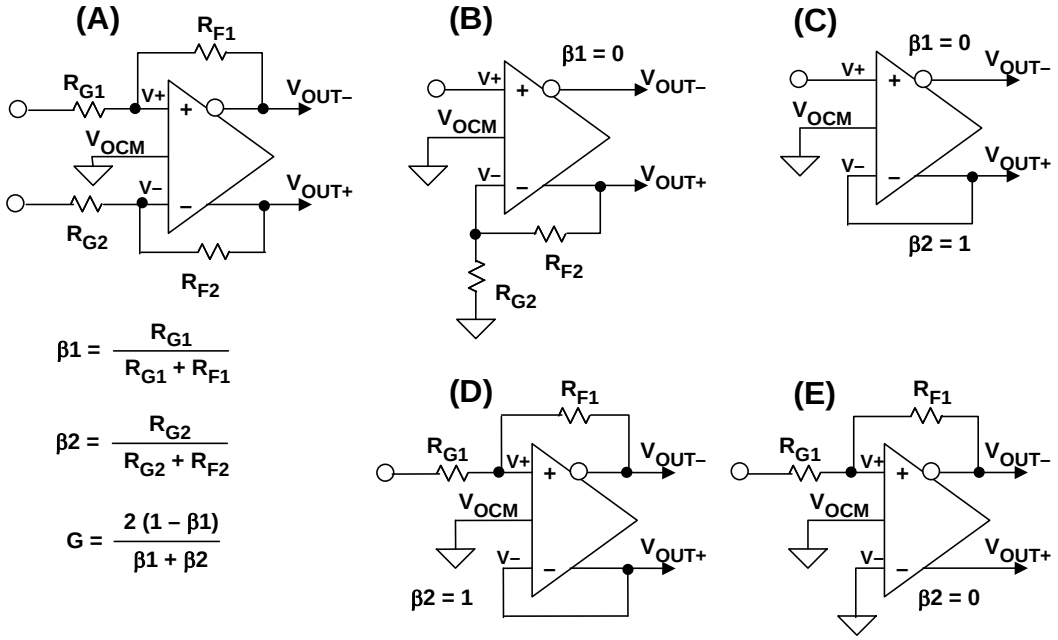


Figure 3: Some Configurations for Differential Amplifiers

Figure 3B shows a configuration where there is no feedback from V_{OUT-} to V+, i.e., β1 = 0. In this case, β2 determines the amount of V_{OUT+} that is fed back to V–, and the circuit is similar to a non-inverting op amp configuration, except for the presence of the additional complementary output. Therefore, the overall gain is twice that of a non-inverting op amp, or $2 \times (1 + R_{F2}/R_{G2})$, or $2 \times (1/\beta 2)$.

Figure 3C shows a circuit where β1 = 0 and β2 = 1. This circuit is essentially provides a resistorless gain of 2.

Figure 3D shows a circuit where β2 = 1, and β1 is determined by R_{F1} and R_{G1}. The gain of this circuit is always less than 2.

Finally, the circuit of Figure 3E has β2 = 0, and is very similar to a conventional inverting op amp, except for the additional complementary output at V_{OUT+}.

DIFFERENTIAL DRIVER/RECEIVER APPLICATIONS

The AD813x/ADA493x-series are also well suited to balanced differential line driving as shown in Figure 4 where the AD8132 drives a 100-Ω twisted pair cable. The AD8132 is configured as a gain of 2 driver to account for the factor of 2 loss due to the source and load terminated cable. In this configuration, the bandwidth of the AD8132 is approximately 160 MHz.

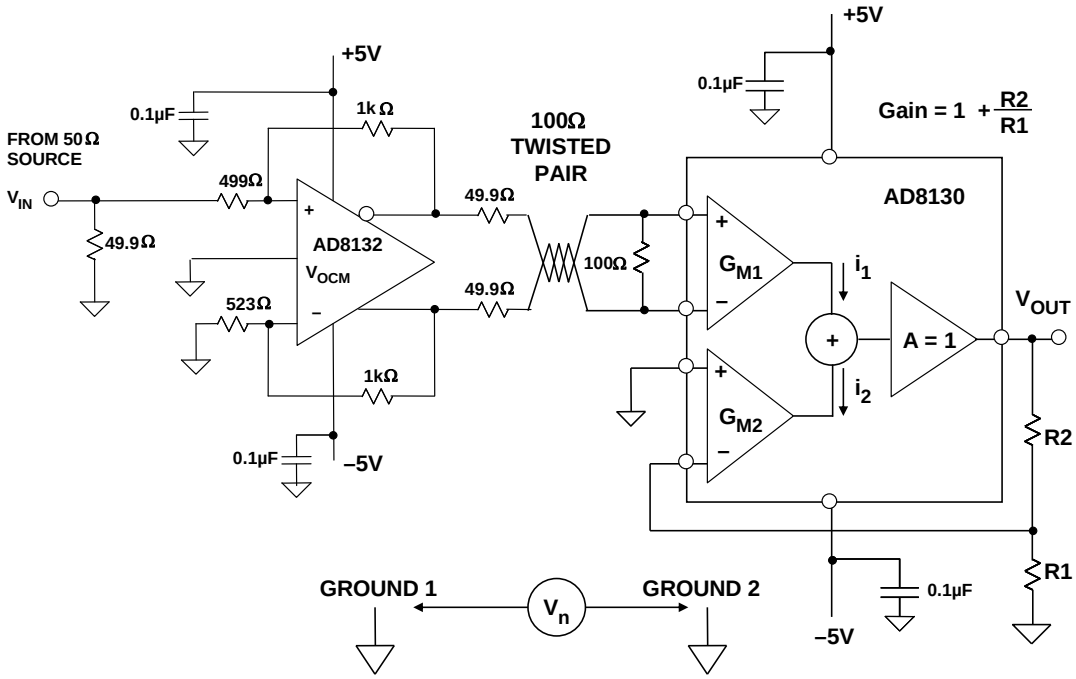


Figure 4: High Speed Differential Line Driver, Line Receiver Applications

The line receiver is an AD8130 differential receiver which has a unique architecture called "active feedback" to achieve approximately 70 dB common-mode rejection at 10 MHz. For a gain of 1, the AD8130 has a 3 dB bandwidth of approximately 270 MHz.

The AD8130 utilizes two identical input transconductance (g_m) stages whose output currents are summed together at a high impedance node and then buffered to the output. The output currents of the two g_m stages must be equal but opposite in sign, therefore, the respective input voltages must also be equal but opposite in sign. The differential input signal is applied to one of the

stages (G_{M1}), and negative feedback is applied to the other (G_{M2}) as in a traditional op amp. The gain is equal to 1 + R2/R1. The G_{M1} stage therefore provides a truly balanced input for the terminated twisted pair for the best common-mode rejection.

A number of triple drivers are available for driving RGB signals over CAT-5 cable such as the AD8133, AD8134, AD8146, AD8147, AD8148.

Corresponding triple receivers are also available, including the AD8143 and AD8145. The AD8123 (Triple) and AD8128 (Single) receivers also include adjustable line equalization.

APPLICATION EXAMPLE: ADA4937-1 DIFFERENTIAL AMPLIFIER DRIVING AD6645 14-bit 80/105MSPS ADC

The AD813x and ADA493x family of differential drivers are suitable for use in dc or ac coupled applications with voltage gains of 1 to 4 (0 dB to 12 dB) and frequencies up to about 100 MHz (depending on the particular member of the family). They are especially useful as low distortion dc-coupled single-ended to differential converters for driving differential input ADCs. The V_{OCM} feature can be used to level shift bipolar signals to match the common-mode input voltage of the ADC. Details of the circuit analysis of dc drivers and selection of resistor values is given in MT-xxx. The ADIsimDiffAmp design tool, is also available to facilitate these designs.

The ADA4937-1 is one of the latest in the series of differential amplifiers and is optimized for operation on a single +5 V supply. Figure 5 shows it is used as a level shifter to drive the AD6645 14-bit 80/105 MSPS ADC. (The ADA4939-1 is a similar part optimized for voltage gains ≥ 2).

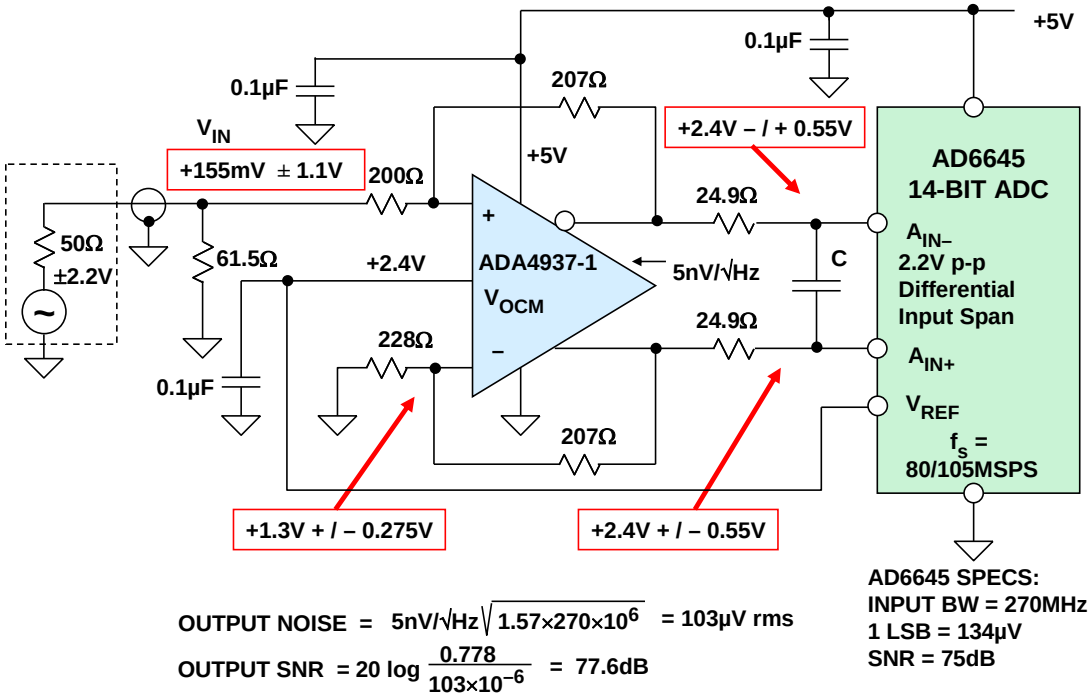


Figure 5: ADA4937-1 Driving AD6645 in +5 V DC-Coupled Application

The circuit shown in Figure 5 will now be carefully analyzed in terms of signal swings and common-mode voltage levels. This is necessary to ensure all voltages fall within the allowable ranges specified by the devices.

The AD6645 operates on a 2.2 V p-p differential signal with a common-mode voltage of +2.4 V. This means that each output of the ADA4937 must swing between 1.85 V and 2.95 V which is within the output drive capability of the ADA4937-1 operating on a single +5 V supply.

The input signals must therefore swing between 1.025 V and 1.575 V which falls within the allowable input range of the ADA4937-1 operating on a single +5 V supply.

The input to the circuit is driven from a 50 Ω source. The "bootstrapped" input impedance in the single-ended configuration is approximately 267 Ω. The 61.5 Ω input termination resistor in parallel with the 267 Ω gain setting resistor makes the overall impedance approximately 50 Ω. Note that a 228 Ω resistor is inserted in series with the inverting input. This is to match the net impedance seen by the noninverting input (200 Ω + 61.5 Ω||50 Ω = 200 Ω + 28 Ω = 228 Ω). Without this extra 28 Ω matching resistor in series with the original 200 Ω gain setting resistor, the unbalanced source impedances cause an unwanted differential offset voltage to appear at the output.

The increase in the bottom gain setting resistor from 200 Ω to 228 Ω requires that the feedback resistors be increased to 207 Ω in order to maintain a gain of one. In practice, the nearest standard 1% resistors would be substituted for the calculated values. The ADIsimDiffAmp design tool is available to facilitate these designs and calculate the required resistor values for a specified gain and source impedance. The tool also checks for violations of the input and output common-mode range limits of the differential amplifier.

The output noise voltage spectral density of the ADA4937-1 is only 5 nV/√Hz. This value includes the contributions of the feedback and gain resistors and is for G = 1. Integrated over the input bandwidth of the AD6645 (270 MHz), this yields an output noise of 103 μV rms. This corresponds to an SNR of 77.6 dB due to the amplifier. Note that the integration must be over the full input bandwidth of the ADC since there is no external noise filter.

The SNR of the AD6645 is 75 dB which corresponds to an input noise of 138 μV rms. The combined noise due to the op amp (103 μV) and the ADC (138 μV) is 172 μV, yielding an overall SNR of 73 dB.

If the full bandwidth of the AD6645 is not required, a single-pole noise reduction filter can be added by selecting an appropriate value for C.

WIDEBAND AC COUPLED ADC DRIVERS FOR IF APPLICATIONS

In the example shown in Figure 6, we are digitizing a wideband signal with the AD9445 14-bit, 125 MSPS ADC and desire to preserve as much of the ADC input bandwidth as possible. Therefore there is no interstage noise filter.

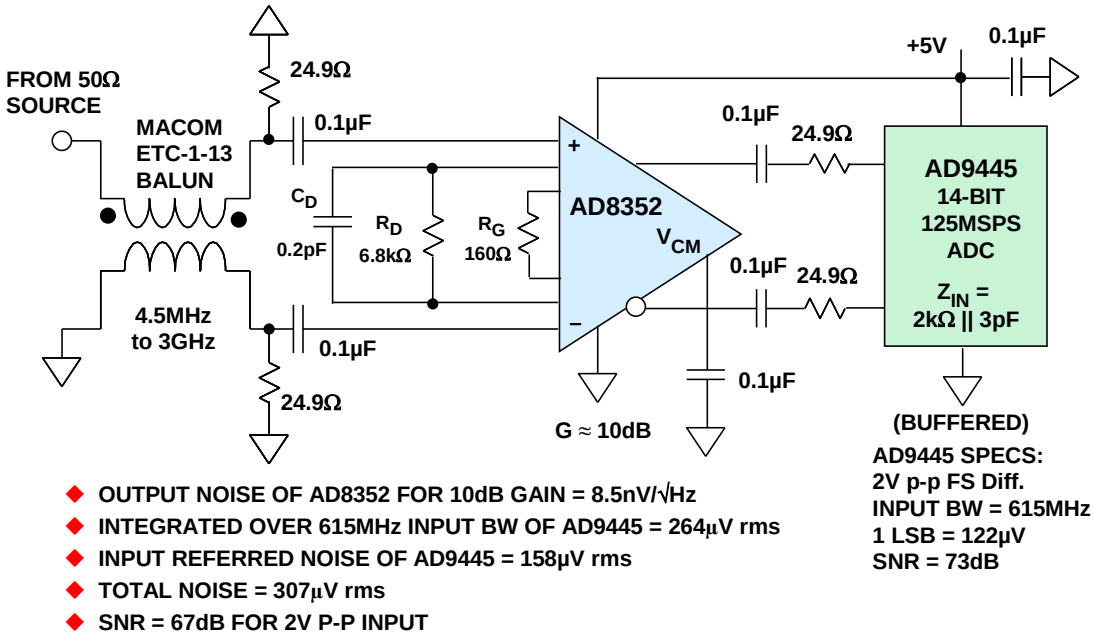


Figure 6: AD8352 2GHz Differential Amplifier Driving AD9445 14-Bit, 125MSPS ADC

The AD9445 has 615 MHz input bandwidth and an SFDR of 95 dBc for a 100 MHz input. For the driver, we have chosen the AD8352 2 GHz bandwidth differential amplifier because it has a resistor programmable gain range of 3 db to 21 dB. The amplifier also has low noise (2.7 nV/√Hz referred to the input for a gain setting of 10 dB) and low distortion (82 dBc HD3 at 100 MHz). The lower end of the bandwidth requirement is approximately 10 MHz.

Figure 6 shows the optimum circuit configuration for driving the AD9445 with the 2 GHz AD8352 in a wideband application. The balun converts the single-ended input to differential to drive the AD8352. Although it is possible to configure the AD8352 to accept a single-ended input (see AD8352 data sheet), optimum distortion performance is obtained if it is driven differentially as shown. The C_D/R_D network is chosen to optimize the third-order intermodulation performance of the AD8352. The values are selected based on the desired gain and are given in the data sheet.

The circuit yields an SFDR of 83 dBc for a 98.9 MHz input signal sampled at 105 MSPS.
The output noise spectral density of the AD8352 for G = 10 is 8.5 nV/√Hz. Since there is no input filter, this must be integrated over the entire 615 MHz input bandwidth of the AD9445. SNR of the combined amplifier and ADC is 67 dB.

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