ANALOG DEVICES

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APPLICATION NOTE

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Provisioning Data Rates Using the AD9951 DDS as an Agile Reference Clock for the ADN2812 Continuous-Rate CDR

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INTRODUCTION

This application note describes how to use the AD9951 direct digital synthesizer (DDS) as an agile reference clock generator for the ADN2812 continuous-rate clock and data recovery (CDR) device.

In a typical application, the ADN2812 will automatically lock to any incoming serial NRZ data stream between 10 Mb/s and 2.7 Gb/s without needing a reference clock as an acquisition aid or any programming for a specific data rate or range of data rates. This is ideal for protocol agnostic line cards that have multiple channels receiving different protocols at different data rates (Figure 1).

However, the ADN2812 has an optional mode where a reference clock can be supplied in order to limit the ADN2812 to lock to a specific data rate. For example, in a DWDM system there can be 16 different channels carrying 16 different protocols. The provider may want to limit the rate on any particular channel for billing purposes by setting up the ADN2812 to lock to only the data rate being billed to the customer on that particular channel.

The AD9951 DDS with the ADN2812 CDR provides a simple, space-saving solution for a frequency agile receiver that needs to lock to a wide range of specific data rates on protocol agnostic line cards.

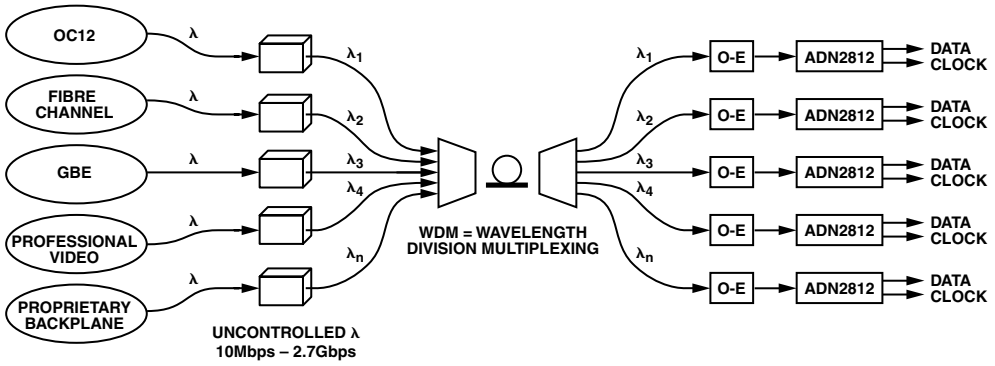

Figure 1. WDM Transponder Block Diagram

ADN2812 Continuous-Rate CDR

The ADN2812 (Figure 2) provides the receiver functions of quantization, signal level detect and clock, and data recovery for continuous data rates from 10 Mbps to 2.7 Gbps. The patented PLL/DLL architecture exceeds all SONET jitter requirements, including jitter transfer, jitter generation, and jitter tolerance. Together with a PIN diode and a TIA preamplifier, this device can implement a highly integrated, low cost, low power fiber optic receiver.

The default mode of the ADN2812 is to automatically lock to any data rate from 10 Mbps to 2.7 Gbps without the need of a reference clock or a microcontroller.

There are, however, optional I²C® accessible modes that allow the user to

- lock to a specific data rate with the use of a reference clock (the subject of this application note).
- read back the data rate that the ADN2812 has locked onto (both coarse and fine readback modes).
- access several other modes of operation and optional features.

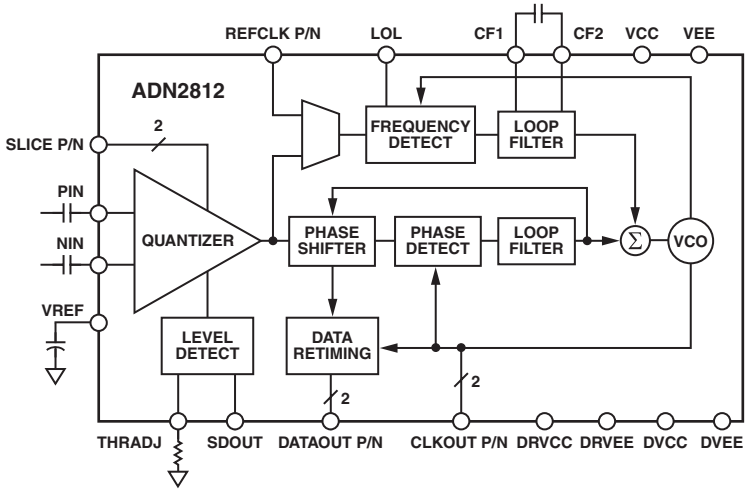

Figure 2. ADN2812 Block Diagram

AD9951 Direct-Digital Synthesizer

The AD9951 (Figure 3) is a direct digital synthesizer (DDS) featuring a 14-bit DAC operating up to 400 MSPS. The AD9951 uses advanced DDS technology, coupled with an internal high speed, high performance D/A converter to form a digitally programmable, complete high frequency synthesizer capable of generating a frequency-agile analog output sinusoidal waveform at up to 200 MHz. The AD9951 is designed to provide fast frequency hopping and fine tuning resolution (32-bit frequency tuning word). The frequency tuning and control words are loaded into the AD9951 via a serial I/O port.

As is true of all DDS architectures, the output DAC (and, therefore, the phase accumulator and look-up tables that feed it) must have a sample rate more than twice the maximum desired output frequency. The AD9951 and other family members make it easy to fulfill this requirement with almost any available clock due to the built-in PLL clock multiplier circuit, which can multiply the clock by any integer between 4 and 20. For example, a 10 MHz clock supplied to the AD9951 could be multiplied by 20, which would allow output frequencies of up to 80 MHz (Nyquist limit plus an allowance for the low-pass reconstruction filter).

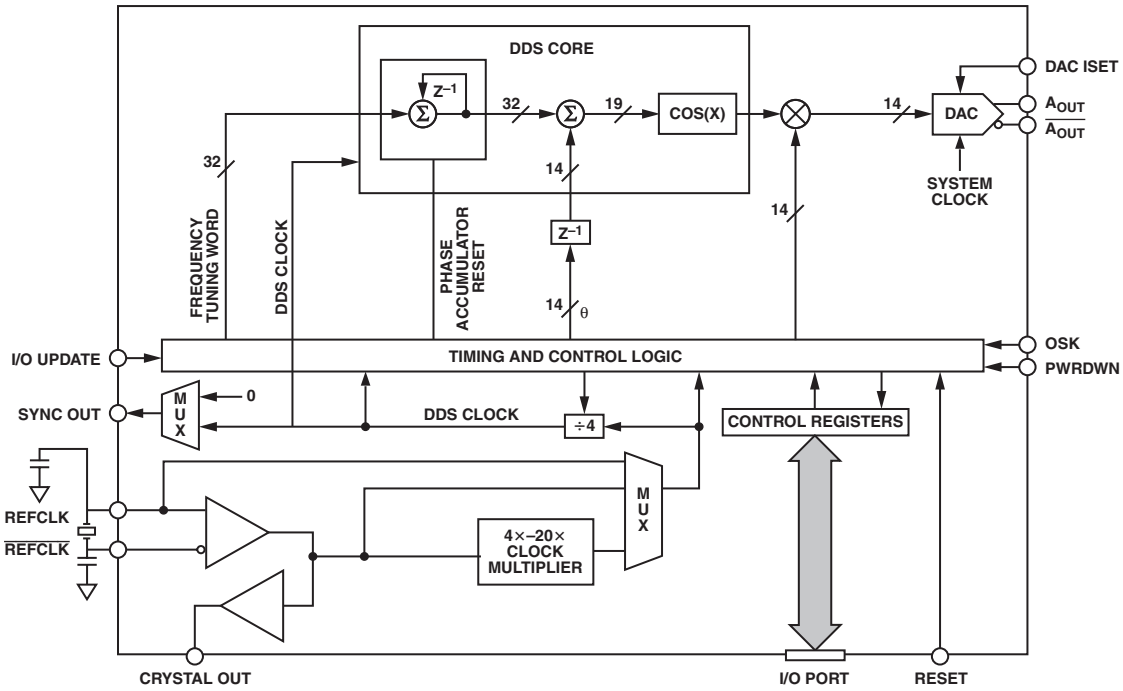

Figure 3. AD9951 Block Diagram

Application Circuit

The complete circuit is shown in Figure 4. The clock input to the AD9951 DDS is 19.44 MHz, which is a frequency commonly found in SONET systems. This single-ended signal is ac-coupled to the REFCLK input, and the $\overline{\text{REFCLK}}$ input is decoupled to AV_{DD} with a 0.1 μF capacitor (C1). Because of the very fine tuning capability of the DDS, the frequency used is not critical, and just about any available frequency can be used, provided that the PLL multiplier is set correctly and that appropriate values are selected in the tuning word. Alternatively, a crystal can be connected directly to the REFCLK and $\overline{\text{REFCLK}}$ inputs.

When using the on-board PLL multiplier, the DDS clock duty cycle is not critical, but if a high speed clock is provided directly and the multiplier is turned off, any jitter or duty cycle errors will affect the quality of the DDS output.

R1 and C2 form part of the PLL multiplier loop filter. While the data sheet shows 1 kΩ and 0.1 μF as general-purpose values, higher multiplication factors and output frequencies work better with the 250 Ω/0.01 μF values shown here. The output of the DDS is from a 14-bit current DAC, whose reference current is set by R2. The value of 3.85 kΩ shown results in a full-scale output current of 10 mA. The compliance range of the IOUT and IOUTN outputs is approximately 250 mV above and below V_{DD}, so these are connected to V_{DD} through R3 and R4 (22 Ω), which results in a full-scale output voltage of 440 mV p-p.

The ADN2812 specifies a reference clock with a minimum of 100 mV p-p differential level. R5/C4 and R6/C5 form a pair of simple low-pass filters to smooth the DAC outputs and remove images. These filtered differential signals are then dc-coupled to the CDR REFCLK inputs. The REFCLKP and REFCLKN pins are the inputs to a differential clock buffer with 100 kΩ resistors internally terminated to $V_{CC}/2$. The input stage can handle rail-to-rail input levels, so ac coupling is not required when driving the inputs differentially.

The remaining pins of the ADN2812 are connected according to the applications circuit in the ADN2812 data sheet; the signal inputs are normally ac-coupled from the PIN/TIA or ROSA. The CML outputs CLKOUTP, CLKOUTN, DATAP, and DATAN are terminated with 100 Ω to V_{CC} and then through 50 Ω transmission lines, and ac coupled to the next device in the receive chain.

ADN2812 Register Settings

When using the reference clock in the lock to reference clock mode, it is necessary to program the CTRLA register of the ADN2812 for the desired data rate. The ADN2812 registers are written to via a standard I^2C interface. The appropriate reference clock frequencies and CTRLA register values for some standard data rates are shown in Table I.

For example, to have the ADN2812 lock only to OC-48 (2.48832 Gb/s):

1. Set up the AD9951 to provide a 19.44 MHz reference clock to the ADN2812.
2. Set CTRLA = 00011101:
   a. CTRLA[7..6] = 00 (reference frequency is between 10 MHz and 20 MHz)
   b. CTRLA[5..2] = 0111 (where $2.48832 \times 10^9 / 19.44 \times 10^6 = 128 = 2^{CTRLA[5..2]}$)
   c. CTRLA[1..0] = 01 (lock to reference clock)

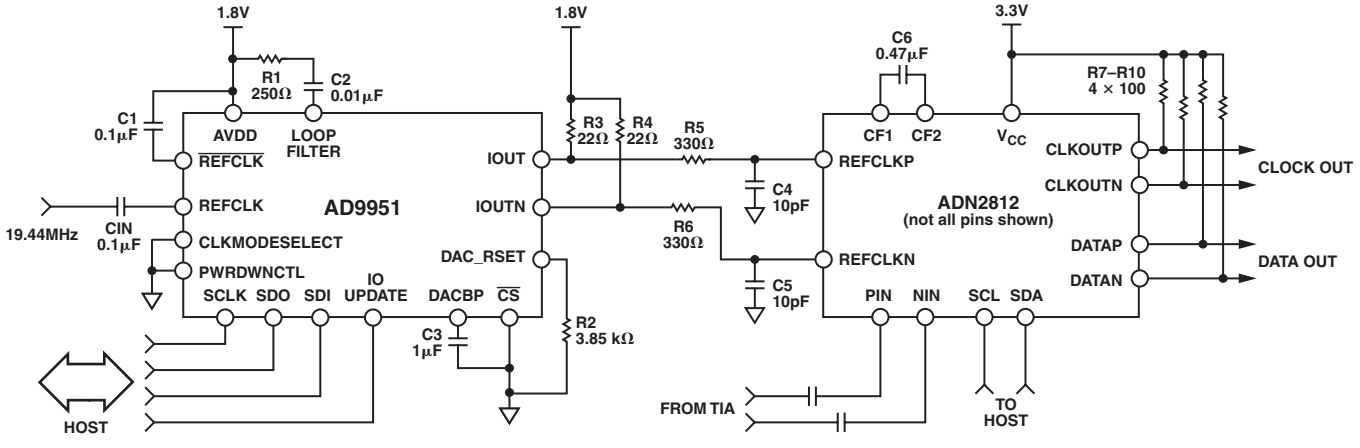

Figure 4. Application Diagram

Following any change in the input data rate or reference clock frequency, it is necessary to write a 0 to 1 transition into CTRLA[0] to initiate a new acquisition with respect to the new data rate or reference frequency.

For information on other registers in the ADN2812, consult the ADN2812 Data Sheet.

Table I. ADN2812 I²C Register Settings for Lock to REFCLK Mode

Data Rate	REFCLK Frequency (MHz)	CTRLA Setting
OC-48 (2.48832 Gb/s)	19.44	00011101
OC-12 (622.08 Mb/s)	19.44	00010101
OC-3 (155.52 Gb/s)	19.44	00001101
GbE (1.25 Gb/s)	39.0625	01010101
Fibre Channel (1.0625 Gb/s)	16.602	00011001
2 × FC (2.125 Gb/s)	16.602	00011101
HDTV (1.485 Gb/s)	23.203	01011001

AD9951 Register Settings

The AD9951 connects to the host microcontroller through a high speed serial port, which can be either 2-wire receive-only (SCLK and SDI) or 3-wire, if register readback is required (SCLK, SDI, and SDO). When data is sent to the device, it is stored in holding registers until the IO_UPDATE pin is toggled from low to high, at which time the data is transferred from the holding registers to the internal working registers. This feature facilitates the synchronization of multiple DDS devices.

On power-up, the default values that are loaded into the AD9951 register are suitable for this application. The only ones that need to be written are those applicable to the PLL multiplier circuit (CFR2) and to the frequency tuning word (FTW0).

For this example, with a clock input to the DDS of 19.44 MHz, optimum results are obtained by setting up the PLL multiplier to multiply by a factor of 20. When generating a DDS system clock greater than 220 MHz with the PLL multiplier, it is recommended to set the VCO gain bit (CFR2<2>) high. Therefore, a value of 0A4 (hex) should be written to Bits <7:0> of the CFR2 register.

Next, the FTW0 (frequency tuning word) register needs to be loaded with a 32-bit value to generate the correct output frequency. Table II lists the hex values to be loaded for the various data rates presented in Table II. If the serial port is operated at maximum speed (25 MHz), a frequency change can be accomplished in approximately 2 μs, which is normally much faster than required, or indeed orders of magnitude faster than the CDR can lock to incoming data.

Table II. Frequency Tuning Word Values for Common Data Rates

Data Rate	REFCLK Frequency (MHz)	FTW0 Setting (Hex)
OC-48 (2.48832 Gb/s)	19.44	0C CC CC CD
OC-12 (622.08 Mb/s)	19.44	0C CC CC CD
OC-3 (155.52 Gb/s)	19.44	0C CC CC CD
GbE (1.25 Gb/s)	39.0625	19 B8 5C B5
Fibre Channel (1.0625 Gb/s)	16.602	0A EE 6D 7B
2 × FC (2.125 Gb/s)	16.602	0A EE 6D 7B
HDTV (1.485 Gb/s)	23.203	0F 47 17 0D

Conclusion

The combination of the AD9951 DDS and the ADN2812 Continuous-Rate CDR provides an ideal low power, low board space solution for clock and data recovery where data rate provisioning is needed, using practically any available system clock frequency. Any data rate from 10 Mbps to 2.7 Gbps can be recovered meeting all applicable specifications.

References

AD9951 Preliminary Data Sheet Rev PrB, 3/03, Analog Devices, Inc.

ADN2812 Preliminary Data Sheet Rev PrE, 12/02, Analog Devices, Inc.

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