ANALOG DEVICES

AN-847
APPLICATION NOTE

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Measuring a Grounded Impedance Profile Using the AD5933
by Sean Brennan

INTRODUCTION

This application note describes the circuit architecture and details required to measure the impedance profile of a grounded sensor using the AD5933 impedance-to-digital converter. The AD5933 is a high precision impedance converter system (see Figure 1) that combines an on-board frequency generator with a 12-bit, 1 MSPS, analog-to-digital converter (ADC). The frequency generator allows an external complex impedance to be excited with a known frequency. The response signal from the impedance is sampled by the on-board ADC, and a discrete Fourier transform (DFT) is processed by an on-board DSP engine. The DFT algorithm returns a real (R) and imaginary (I) data-word at each output frequency. The magnitude of the impedance and relative phase of the impedance at each frequency point along the sweep are easily calculated using Equation 1 and Equation 2.

$$Magnitude = \sqrt{R^2 + I^2} \qquad (1)$$

$$Phase = Tan^{-1} (I/R) \qquad (2)$$

The AD5933 requires a calibration process before any valid measurement can take place. The calibration process simply requires that a measured impedance (for example, a precision resistor) is connected between VIN and VOUT and a scaling factor (gain factor) is calculated for subsequent measurements, as described in the AD5933 data sheet. As shown in Figure 1, the output pin (VOUT) of the transmit side is an ac excitation voltage signal with an appropriate dc bias. The input pin (VIN)

to the receive side transimpedance amplifier presents a virtual earth voltage of VDD/2 to the output excitation voltage at VOUT. Ohm's law dictates that a signal current flows through unknown impedance and into the feedback pin because of the potential difference from VOUT to VIN. The current is transformed into a voltage on the output of the transimpedance amplifier. The signal processing that follows on the output voltage of the transimpedance amplifier allows the impedance to be accurately calculated (see the AD5933 data sheet for further details). The AD5933 can measure an impedance value between 100 Ω and 10 MΩ to a system accuracy of 0.5% for excitation frequencies between 1 kHz and 100 kHz.

A fundamental problem exists for certain applications where the impedance to be analyzed must be connected between the output (VOUT) and ground. In applications where the unknown impedance/sensor being measured has one connection to ground, with no signal return path, the AD5933 as shown in Figure 1 cannot be used to analyze the impedance or sensor. This document describes a circuit architecture using the AD5933 and external components that allows the system designer to measure the impedance profile of a grounded load. This application note also describes the performance of such a system in measuring a load that varies from 20 kΩ to 60 kΩ between 99.9 kHz and 100.1 kHz, running from a single supply of 5.0 V.
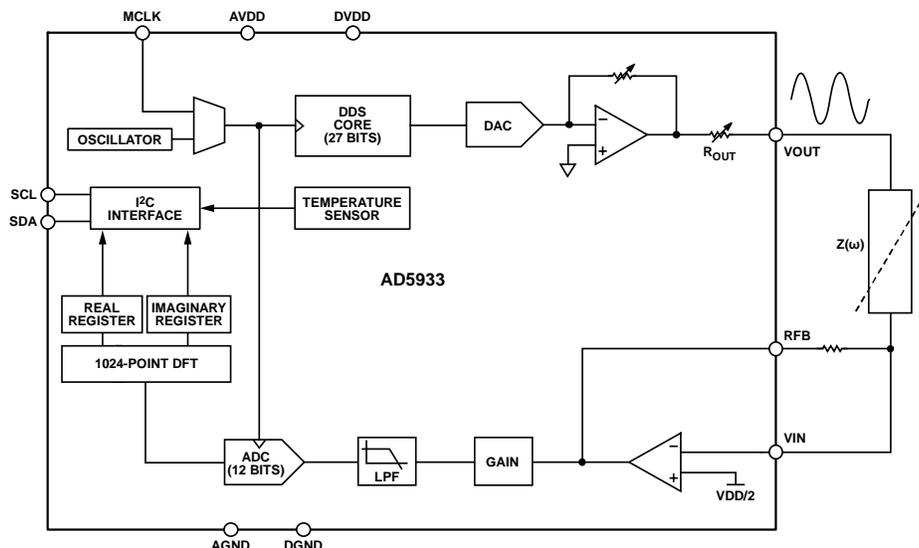

Figure 1. AD5933

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REVISION HISTORY

8/12—Rev. 0 to Rev. A

6/06—Revision 0: Initial Version

OVERVIEW

Figure 2 shows the circuit block diagram used to measure the impedance profile of a grounded load. The circuit consists of three major blocks.

The first block is a modified high-side current sense using a precision single supply, rail-to-rail output, JFET instrumentation amplifier (AD8220) to measure the current flowing through a ense resistor connected in series with the grounded impedance.

The second block is the bias circuitry and a reference buffer to ensure that the input sense signal and output signal do not saturate the internal amplifiers of the AD8220 amplifier and the receive side transimpedance amplifier of the AD5933.

Last there is the AD5933 impedance-to-digital converter.

The following sections detail the external circuitry surrounding the AD5933, as shown in Figure 2, as well as the gain factor required for the new system to successfully measure the grounded impedance. Finally, this application note describes the overall performance of the circuit shown in Figure 2 in measuring a grounded impedance. The grounded complex impedance measures between 20 kΩ and 60 kΩ over a frequency range of 99.9 kHz to 100.1 kHz. The required steps to perform a frequency sweep are detailed in the AD5933 data sheet.
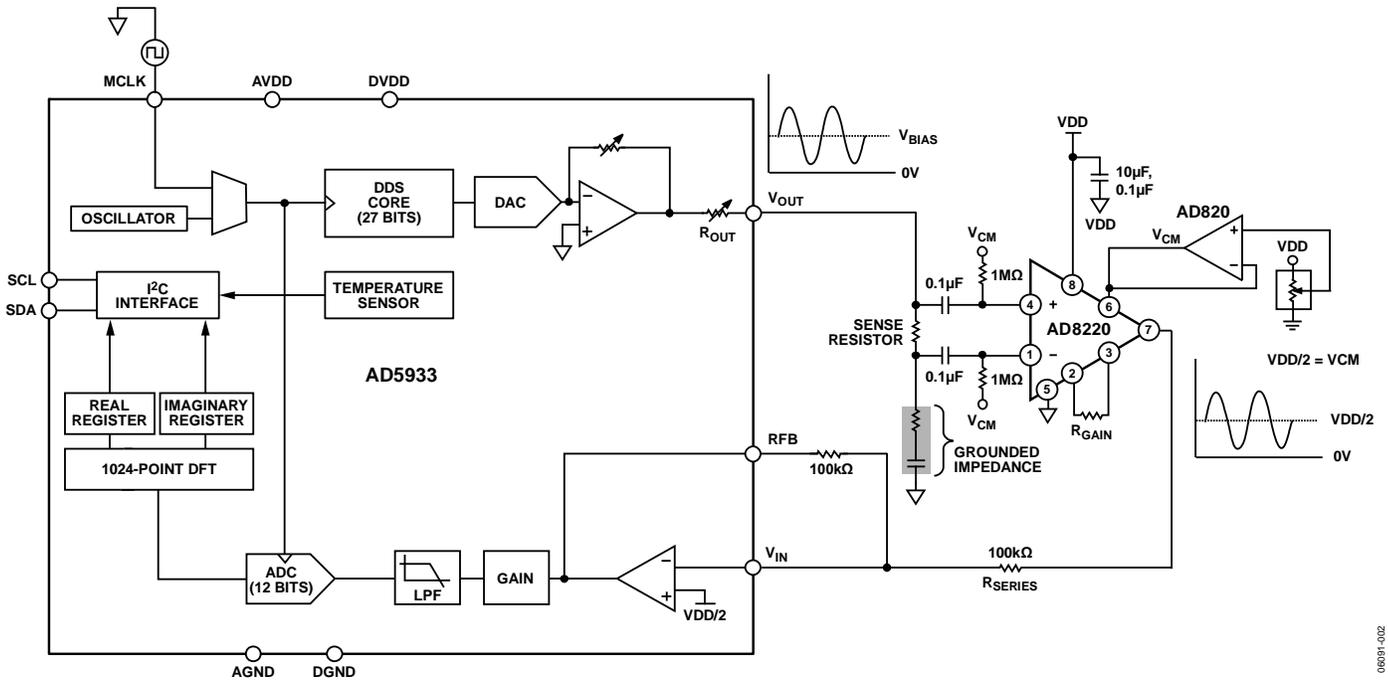

Figure 2. Grounded Impedance Measurement Circuit

CIRCUIT OPERATION EXPLAINED

Figure 3 shows a close-up of the modified high-side, current sense used in the circuit. The AD5933 output excitation voltage is developed across the sense resistor, which is in series with the grounded load. The resulting current through the grounded load is monitored by the AD8220 high precision in-amp, which measures the difference voltage across R_{SENSE}. The AD8220 sine wave output signal is symmetric about a set bias value of VDD/2 and connected back into the AD5933 for digital signal processing (DSP).
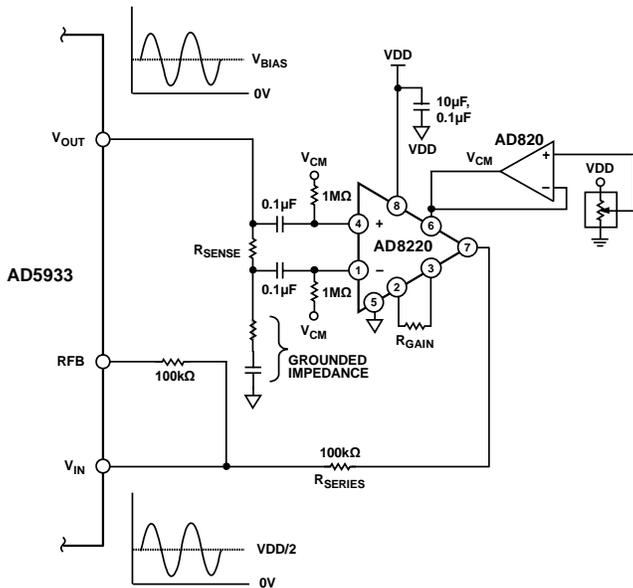

Figure 3. Modified High-Side Current Sense Using an AD8220 Instrumentation Amplifier

Referring to Figure 3, with a system supply value (VDD) of 3.2 V, the user can program the AD5933 output ac excitation voltage of the AD5933 to be one of four values (2 V p-p, 1 V p-p, 400 mV p-p, or 200 mV p-p) by setting Bit D10 and Bit D9 in the AD5933 control register (see the AD5933 data sheet for more details). The dc bias of the output excitation in each case is set according to the excitation voltage chosen. Both the output ac excitation voltage and the corresponding dc bias scales with the AD5933 supply voltage (VDD).

Therefore, the system designer can choose any one of the four output voltages to act as the stimulus voltage signal to the grounded load. The choice of excitation voltage depends upon the value of the sense resistor and the span of the grounded impedance and the common-mode input range of the AD8220.

The AD8220 instrumentation amplifier shown in Figure 3 measures the current through a sense resistor (R_{SENSE}) which is connected between the output pin of the AD5933 and the remaining terminal of the grounded impedance. The current flowing through the grounded load results in a voltage drop across this sense resistor. This voltage is measured and amplified by the AD8220 to provide a single-ended (with respect to the AD8220 reference voltage, Pin 6 (REF) sine

wave output voltage signal. The AD8220 output voltage is then connected to a series resistor, which in conjunction with an equal value feedback resistor, RFB, results in an inverted unity gain voltage being generated at the output of the receive side current-to-voltage (I-to-V) amplifier within the AD5933.

The output voltage of the I-to-V amplifier is then low-pass filtered and finally sampled by the 1 MSPS ADC. The ADC output samples are windowed and presented to the internal DSP, which performs a synchronized single-point DFT at the same frequency as the AD5933 output excitation waveform. The DFT output is a complex answer and is stored internally in the form of a 16-bit, twos complement real and imaginary value at each frequency of the sweep.

The magnitude of the real and complex component given by Equation 3 is a measure of the peak signal sampled by the internal ADC at each frequency. To convert the peak signal to a impedance figure, the magnitude of the real and imaginary component is multiplied by a number called a gain factor and subsequently inverted in a nearby processor to give the resulting impedance value at each frequency.

$$Magnitude = \sqrt{R^2 + I^2} \tag{3}$$

As described in the AD5933 data sheet, the gain factor for the AD5933 circuit (as shown in Figure 1) is a number determined once at system calibration. The gain factor simply involves placing a known impedance between the VIN and VOUT pins and calculating the magnitude of the resulting code at a midsweep frequency programmed by the user. The AD5933 system gain settings must be carefully considered so that the optimum signal is presented to the ADC input without saturation of the ADC over the unknown impedance range being measured. Therefore, the user must have prior knowledge of the impedance span under test in order to calibrate the AD5933 correctly. Mathematically the gain factor is given by Equation 4.

$$Gain\ Factor = \left(\frac{Admittance}{Code} \right) = \frac{\left(\frac{1}{Impedance} \right)}{Magnitude} \tag{4}$$

Consider the following example of a gain factor calculation with these assumptions:

Output excitation voltage = 2 V p-p
Calibration impedance value, $Z_{CALIBRATION}$, = 200 kΩ
PGA gain = ×1
Current to voltage amplifier gain resistor = 200 kΩ
Calibration frequency = 30 kHz

The typical contents of the real and imaginary register after a frequency point conversion would be:
Real register: = F064 hex = −3996 decimal
Imaginary register: = 227E hex = 8830 decimal

$$Magnitude = \sqrt{(-3996^2 + (8830)^2} = 9692.106$$

$$Gain\ Factor = \left(\frac{\dfrac{1}{200\ k\Omega}}{9692.106} \right) = 515.819E-12$$

Because the circuit shown in Figure 2 is different from the circuit shown in Figure 1, a new gain factor must used to transform the AD5933 output codes into an impedance figure. The new gain factor accounts for the fact that the circuit shown in Figure 2 has a sense resistor that remains constant for the rest of the measurement and the fact that the impedance under test is no longer directly connected to the AD5933 input terminal (VIN). The new gain factor is clearly described in the System Gain Factor section.

Once the system designer accounts for the new gain factor, the same calibration procedure remains: the system is calibrated at a specific frequency, using a measured grounded load and sense resistor the gain factor is calculated, and so any change in the grounded load can be measured by the AD5933 output code. The impedance profile can be determined in a nearby processor either at a single frequency or over a range of frequencies.

POWERING THE CIRCUIT

The circuit in Figure 2 operates on a single supply of 5.0 V. The AD5933 and AD8220 have a high PSRR specification. However, for optimum performance, a stable dc voltage should be used to power both chips because noise on the supply lines can adversely affect circuit performance. The power supply to both parts is decoupled using standard surface-mount, 0.1 μF ceramic chip capacitors and 10 μF electrolytic tantalum capacitors. The separate analog and digital grounds of the circuit are connected at one point only. It is recommended to tie all three supply pins of the AD5933 together and run from the single supply (VDD = 5.0 V in this system). Similarly, it is recommended to connect the three ground pins of the AD5933 together, as shown in Figure 2. The AD5933 and the AD8220 run from the same positive and negative supply, as shown in Figure 4, so the system remains ratio-metric.

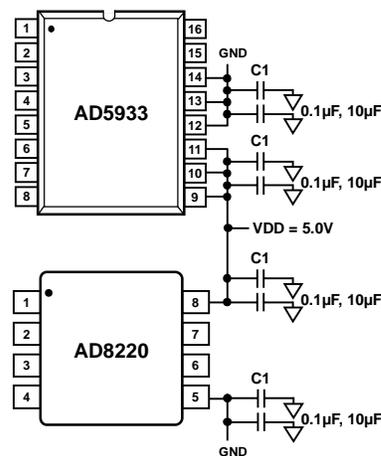The AN-202 and AN-581 Application Notes provide more information on grounding and decoupling single supply amplifiers.

Figure 4. AD5933/AD8220 Single Supply Configuration

CHOOSING THE OUTPUT EXCITATION RANGE

The transmit side of the AD5933 generates a sinusoidal output voltage at VOUT. The AD5933 performs a linear frequency sweep. The frequency sweep is defined by the contents of three registers (start frequency, frequency increment, and number of increments) preprogrammed by the user (see the AD5933 data sheet). The user has the added flexibility to select one of four possible output excitation peak-to-peak ranges by setting Bit D8 and Bit D9 in the control register. At a supply voltage of 3.2 V, the AD5933 was designed to provide the four selectable excitation ranges outlined in Table 1. The corresponding dc bias of each excitation range is also outlined.

Table 1. AD5933 Output Excitation Ranges at VOUT (VDD = 3.2 V)

Output Excitation Voltage Amplitude	Output DC Bias Level
Range 1: 2 V p-p	1. 6 V (VDD/2)
Range 2: 1 V p-p	0. 8 V (VDD/4)
Range 3: 400 mV p-p	0.320 V (VDD/10)
Range 4: 200 mV p-p	0.160 V (VDD/20)

The receive side pin (VIN) of the AD5933 is an ac virtual earth to the output excitation voltage at VOUT. Therefore, the input (VIN) presents a constant hard-biased voltage of VDD/2 to any of the chosen excitation signals given in Table 1. The reference to the ADC is also approximately the supply range (0 V to VDD), making the AD5933 a truly ratio-metric system. As the supply voltage varies between 2.7 V and 5.5 V, the peak-to-peak of the ac output excitation signal and the corresponding dc bias increases/decreases in conjunction with the ADC reference, so the output code is not affected by any supply variations. This provides added immunity to any power supply drift over time.

The peak-to-peak value (of Range 2) of the ac output excitation voltage is scaled with the supply voltage (VDD) according to Equation 5:

$$Output\ Excitation\ Voltage\ (p-p) \equiv \frac{1.0}{3.2} \times VDD \qquad (5)$$

Correspondingly, the dc bias value of the output excitation voltage is also scaled with the supply voltage (VDD) according to Equation 6:

$$Output\ Excitation\ Voltage\ (p-p) \equiv \frac{800\ mV}{3.2} \times VDD \qquad (6)$$

The circuit shown in Figure 2 was designed to operate from a supply of 5.0 V. Therefore, the peak-to-peak voltage of Range 1 at VDD = 5.0 V is given by Equation 7:

$$Output\ Excitation\ Voltage\ (p-p) \equiv \left(\frac{1.0}{3.2} \times 5.0\right) = 1.5625\ V\ p-p \quad (7)$$

In addition, the bias voltage is given by Equation 8:

$$Output\ Excitation\ Voltage\ (p-p) \equiv \frac{800\ mV}{3.2} \times 5.0\ V = 1.25\ V \quad (8)$$

SELECTING THE SENSE RESISTOR

Once the AD5933 output excitation range for the circuit is selected, choose a suitable sense resistor (R_SENSE) that allows the AD8220 to accurately measure the range of grounded impedance (20 kΩ to 60 kΩ). The voltage developed across the sense resistor is multiplied by the internal voltage gain of the AD8220 (set by the resistor value seen between Pin 2 and Pin 3 of the AD8220) to set the peak-to-peak ac output voltage. The AD8220 voltage gain helps the system designer choose an appropriate R_SENSE value.

The first requirement at this stage is to select a AD8220 gain resistor (which determines the system bandwidth). The second requirement is to select a sense resistor (R_SENSE) that provides a suitable AD8220 output voltage which is linear and symmetric (about a bias point of VDD/2) over the entire unknown impedance range, while preventing saturation of the internal circuitry of the AD8220. Once these requirements are achieved, the AD8220 output signal can be further amplified by selecting a suitable combination of RFB/R_SERIES and PGA setting such that the dynamic range of the AD5933 internal ADC is used.

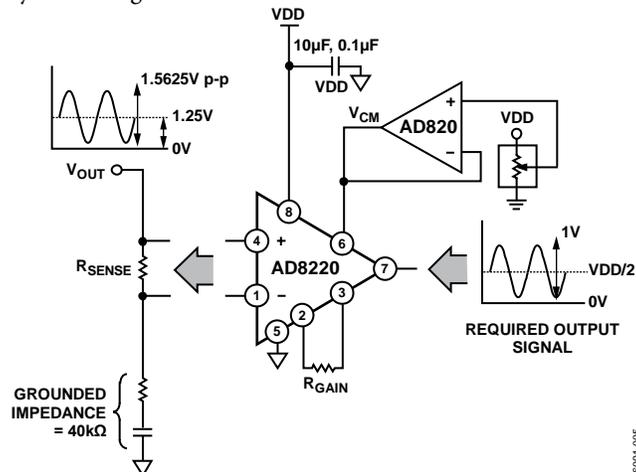Figure 5. Choosing the Correct Sense Resistor (R_SENSE) for the Calibration Grounded Impedance

Figure 5 shows how to choose a suitable sense resistor (R_SENSE) to measure the grounded complex impedance. Having selected Range 1 as the excitation range (a 1 V p-p sine wave biased at VDD/4) and knowing that the grounded impedance range is between 20 kΩ and 60 kΩ, the gain resistor of the AD8220 is selected to set the required bandwidth and common-mode rejection ratio (see the section on Instrumentation Amplifier Considerations). The AD8220 voltage gain was set to 11 by connecting a 4.67 kΩ resistor between Pin 2 and Pin 3, which corresponds to a 3 dB point of 400 kHz. Therefore, when the AD5933 output excitation frequency is sweeping between 99.9 kHz and 100.1 kHz, the AD8220 operates in the flat mid-band gain region with a good common-mode rejection of almost 80 dB.

The circuit in Figure 5 is calibrated at the midpoint of the impedance range (≈40 kΩ), to ensure that the peak-to-peak AD8220 output voltage is linear and symmetric about this impedance point. With this knowledge, the goal is to choose the sense resistor to generate a 1 V p-p AD8220 output voltage for a calibration grounded impedance of 40 kΩ and AD8220 gain of 11, as shown in Figure 5. Working through the circuit analysis, this requires that the voltage (ΔV) developed across the sense resistor R_SENSE and measured by the AD8220 be given by

$$\Delta V = \frac{1\ V\ p-p}{11} = 90\ mV\ p-p \qquad (9)$$

Knowing the value of the calibration grounded impedance (40 kΩ, measured 39.9 kΩ), a simple resistor divider analysis shows that an R_SENSE value of 2.67 kΩ satisfies the requirement to generate a 90 mV p-p signal across R_SENSE, resulting in a 1 V p-p signal. The common-mode input of the AD8220 contains both an ac and dc signal due to the dc bias (1.17 V) of the AD5933 ac excitation signal (1.46 V) and is given in by the restive divider law shown in Equation 10 and Equation 11.

$$DC = \frac{39.9\ k\Omega}{39.9\ k\Omega + 2.67\ k\Omega} \times 1.25\ V \equiv 1.1715\ V \qquad (10)$$

$$AC = \frac{39.9\ k\Omega}{39.9\ k\Omega + 2.67\ k\Omega} \times 1.5625\ V\ p-p \equiv 1.4644\ V \qquad (11)$$

Thus, the total common-mode input voltage seen by the AD8220 input is a 1.46 V p-p sine wave biased on a 1.17 V dc level.

The voltage developed on the AD8220 output is therefore (1.56 V − 1.46 V) × 11 ≈ 1.1 V p-p, which is close to the required 1 V p-p output. The output ac signal is biased on a dc voltage of (1.25 V − 1.1715 V) × 11 = 863 mV.

The output dc bias of 863 mV must be level shifted to VDD/2 by applying a buffered voltage at Pin 5 (V_REF) of the AD8220 to prevent internal saturation of the AD5933 impedance (see the Instrumentation Amplifier Considerations section).

SYSTEM GAIN FACTOR

As explained in the Circuit Operation Explained section, the gain factor for the proposed circuit in Figure 2 is different from the AD5933 standalone configuration shown in Figure 1 (as shown in the data sheet). The new gain factor can be determined by examining the output code of the AD5933 in Figure 2. The AD5933 output code is proportional to voltage presented to the input of the internal ADC (that is, the voltage gain through the system), and is given by Equation 12:

$$Output\ Code \propto \left\{ I \times \Delta V \times In\text{-}Amp\ Gain \times \frac{RFB}{R_{SERIES}} \times PGA \right\} \quad (12)$$

where:
I is the current flowing from the AD5933 output pin (VOUT) through the grounded load.
ΔV is the differential voltage seen by the AD8220 across R_{SENSE}.
PGA is the gain setting of the internal AD5933 programmable gain amplifier.
RFB/R_{SERIES} is the ratio of the AD5933 feedback resistor to AD8220 output load resistor.

The AD5933 output code can now be written as follows:

$$Output\ Code \propto \left\{ VOUT \times \frac{1}{(Z + R_{SENSE})} \times (V^+ - V^-) \times 11 \times \frac{100\ k\Omega}{100\ k\Omega} \times 1 \right\}$$

$$(13)$$

The ratio RFB/R_{SERIES}, PGA setting, and AD8220 gain settings all remain constant once the system shown in Figure 2 has been calibrated for the unknown impedance range under test.

The gain factor used in the circuit is given by the Equation 14:

$$Gain\ Factor = \left(\frac{\dfrac{1}{Z + R_{SENSE}}}{\sqrt{R^2 + I^2}} \right) \quad (14)$$

where:
R and I are the real and imaginary components returned by the AD5933 at the calibration frequency.

Finally, the measured impedance of this new architecture must account for the sense resistor, which is in series with the grounded load (R_{SENSE} remains constant throughout the measurement) and needs to be subtracted in order to measure the true grounded impedance at each frequency. This is given by Equation 15:

$$Z(f) = \left(\frac{1}{Gain\ Factor \times Code} \right) - R_{SENSE} \quad (15)$$

where:
$Code$ is the magnitude of the real and imaginary component stored given by Equation 1 at each subsequent sweep frequency.
R_{SENSE} is the chosen sense resistor for the unknown impedance range under test.

INSTRUMENTATION AMPLIFIER CONSIDERATIONS

The AD8220 voltage gain is determined by placing a resistor across the R_{GAIN} terminals, or more precisely, by whatever impedance appears between Pin 1 and Pin 8. The AD8220 offers accurate gains using 0.1% to 1% tolerance resistors. Table 2 shows required values of R_{GAIN} for various gains. Note that for G = 1, the R_{GAIN} terminals are unconnected (R_{GAIN} = ∞). For any arbitrary gain, R_{GAIN} can be calculated by using Equation 15:

$$R_{GAIN} = 49.4\ k\Omega/(G-1) \quad (15)$$

Table 2. AD8220 Gain Setting Resistor Values

1% Standard Value of R_{GAIN}	Calculated Gain
49.9 kΩ	1.990
12.4 kΩ	4.984
4.7 kΩ[1]	10.51
2.61 kΩ	19.93
1.0 kΩ	50.40
499 Ω	100.0
249 Ω	199.4
100 Ω	495.0
49.9 Ω	991.0

[1]Chosen resistor for circuit shown in Figure 2.

The AD8220 defaults to a gain of G = 1 when no gain resistor is used (R_{GAIN} = ∞). Gain accuracy of the AD8220 is determined by the absolute tolerance of R_{GAIN}. The temperature coefficient of the external gain resistor increases the gain drift of the AD8220 output.
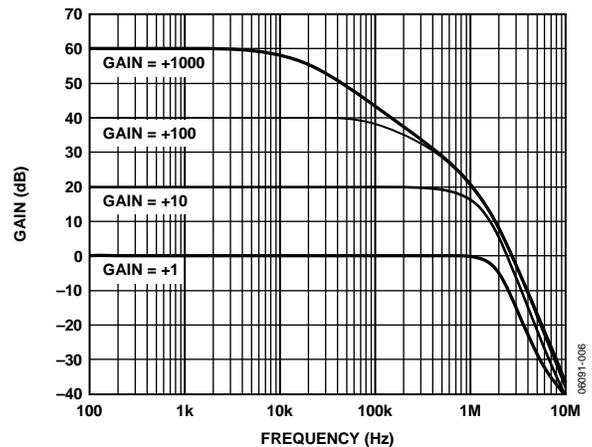
Figure 6. AD8220 Gain vs. Frequency

The requirement of this experiment is to measure the grounded complex impedance between 99.9 kHz and 100.1 kHz. The gain of the AD8220 determines the bandwidth of the output signal, as shown in Figure 6. The AD8220 gain was set to ≈ ×11(that is, ≈ 20 dB) using a R_{GAIN} value of 4.7 kΩ in order to operate within the correct frequency range of the AD8220. Figure 7 shows that the CMRR of the AD8220 is ≈75 dB in this region.
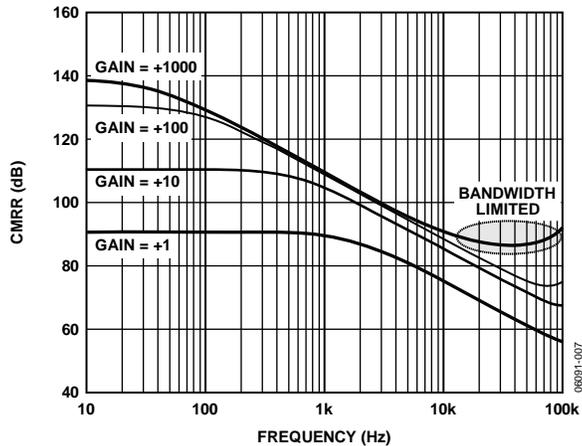
Figure 7. AD8220 CMRR vs. Frequency

As with all instrumentation amplifiers, when the AD8220 is used with a low single supply voltage, high amplifier gains can render the in-amp circuit inoperative. Figure 8 shows this point. It most commonly occurs when in-amps are operating at high gains, such as 1000. Under these circumstances, a 10 mV p-p input times a gain of 1000 creates a 10 V p-p signal between the outputs of A1 and A2. When using dual ±15 V supplies, this situation can occur. However, the circuit shown in Figure 2 is restricted to using a 5 V single supply, so the circuit becomes dysfunctional. Because users of monolithic ICs do not have access to the buffer outputs of the AD8220, A1 and A2, they only see what is happening at the final output—the output of A3.
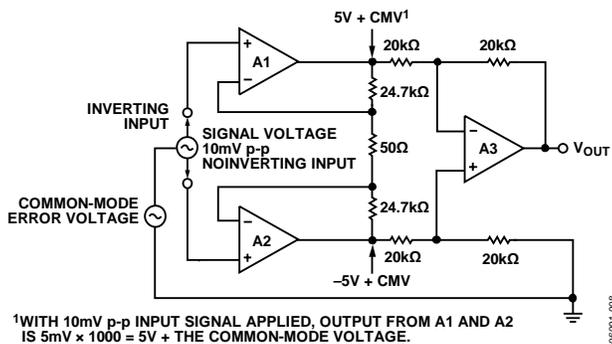
[1]WITH 10mV p-p INPUT SIGNAL APPLIED, OUTPUT FROM A1 AND A2 IS 5mV × 1000 = 5V + THE COMMON-MODE VOLTAGE.

Figure 8. Simplified AD8220 Internal Block Diagram

Another common application problem stems from operating standard, non-rail-to-rail devices, from low single-supply voltages. A high quality rail-to-rail in-amp, such as the AD8220, with a gain of 1 can swing its output to only within 0.15 V of the positive supply line and down to 0.2 V above ground. Its input-voltage range can only swing to within 2 V of the positive supply. With higher gains, the amplifier's output swing does not reach the supply voltage. Therefore, when using a 5 V single supply, the amplifier has approximately a 3 V output swing. Unfortunately, some system designers forget about amplifier headroom and use standard, non-rail-to-rail products in these applications. Even a good dual-supply in-amp has an output swing within only about 2 V of either rail.

DRIVING THE AD8220 REFERENCE TERMINAL

The reference terminal potential of the AD8220 defines the zero output voltage and is especially useful when the load does not share a precise ground with the rest of the system. It provides a direct means of injecting a precise offset to the output. The reference terminal is also useful when bipolar signals are being amplified, as it can be used to provide a virtual ground voltage. The voltage on the reference terminal can be varied from ground to $+V_S$. A common application problem that must be avoided in this experiment is when system designers try to drive the reference pin of an AD8220 in-amp with a high impedance source. Typical values for the impedance of the reference input in many popular in-amps are 20 kΩ to 125 kΩ. If a low impedance source, such as an op amp, is directly driving the reference, there is no problem, but often, an unwary designer tries to use a resistive voltage divider as a low cost, ratio-metric reference and ends up introducing serious errors.
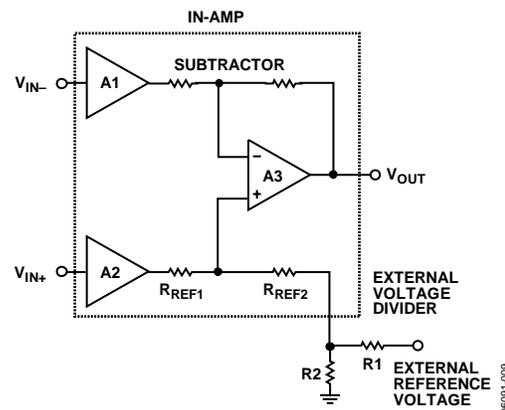
Figure 9. Using a Buffer or a Reference ADR42x

The reference input in the AD8220 is part of the output-subtracter circuit in a typical three-op-amp instrumentation amplifier. As such, it has a finite input resistance, approximately equal to R_{REF1} plus R_{REF2}, typically. Adding external resistor R2, between the reference terminal and common ground, as shown in Figure 9, unbalances the output (A_3) subtracter circuit, introducing a common-mode error. An obvious way to minimize this problem is to reduce the value of R2 to approximately 0.1% of R_{REF1} plus R_{REF2} (for 72 −dB CMR). However, with 20 kΩ values of R_{REF1} and R_{REF2} (40,000 total input Z), R2 must be 40 Ω. This value, in turn, unnecessarily burns large amounts of supply current in the voltage-divider network. There is also the issue of R_{REF1} and R_{REF2} shunting R2 and causing a reference-voltage error. The solution is to use a simple buffer like the AD820 and drive it with a potentiometer run from the 5.0 V supply, as shown in Figure 10.

Figure 10. Buffer the Reference Input

SETTING AD8220 COMMON-MODE INPUT RANGE

Limits on AD8220 common-mode range, coupled with the fact that in this application the common-mode input signal to the AD8220 changes depending on the value of the grounded impedance, forces the user to ac-couple the inputs of the in-amp circuit in this application. In this experiment, the AD8220 is powered by a single 5 V supply, so ac coupling is more complicated and requires applying a dc common-mode voltage, V_{CM}, to both inputs (Figure 12). This step is necessary because the in amp output cannot swing below the negative supply—in this case, ground—as shown in Figure 11. Here, if the in-amp output voltage tries to swing more than a few millivolts negative, the signal is clipped.

Figure 11. AD8220 Required Output Voltage vs. Common-Mode Input Voltage

A common, incorrect procedure is to connect a capacitor in series with each in-amp input terminal. Again, because a monolithic in-amp is a complete package, system designers often fail to realize what is inside the IC. In-amps like the AD8220 connected with these floating inputs do not have a dc reference. The input bias currents charge up the ac coupling capacitors until they exceed the input common-mode voltage. In other words, the capacitors charge up to the supply line or down to ground, depending on the direction of the in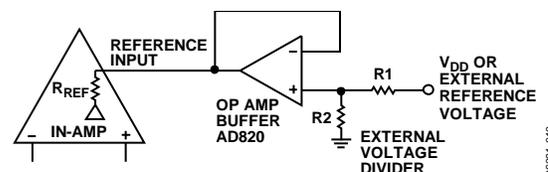put bias currents. With a FET input device and high value capacitors, it could take several minutes before the in-amp becomes inoperative. Therefore, a casual lab test might not detect this problem, thus it is important to avoid it altogether.

Figure 12. AC Coupling the AD8220 Inputs

Choosing appropriate voltages for V_{CM} and V_{REF} is the next important design consideration, especially in low supply voltage applications. In general, set V_{CM} to the middle of the expected input dynamic range and center V_{REF} on the expected output dynamic range. Output centering is similar: estimate the amount and direction of the in-amp output swing—in most cases, $\Delta V \times$ AD8220 gain $+V_{CM}$—and then apply a reference voltage at V_{REF} that is in the center of that range. Look at the voltage swing at the impedance range limits. The reference applied to Pin 5 of the AD8220 is 2.5 V for a supply voltage of 5 V. The choice of dc-return-resistor value for ac-coupled circuits is a trade-off between offset errors and the physical and electrical size of the input coupling capacitors. The larger the value of the input resistor, the smaller the required input coupling capacitor. This approach saves both money and PCB space. However, the trade-off is that high value input resistors increase the offset voltage error due to input offset currents. Offset voltage drift and resistor noise also increase. With lower resistor values, higher value input capacitors for C1 and C2 are necessary to provide the same −3 dB corner frequency, as shown in Equation 16.

$$F - 3 \text{ dB} = (1/(2\pi R1C1)) \tag{16}$$

where R1 = R2 and C1 = C2.

GROUNDED IMPEDANCE MEASUREMENT

The circuit shown in Figure 2 was developed and used in the measurement of grounded complex impedance. The transmit side of the AD5933, used as a voltage excitation signal, drives the sense resistor and the grounded impedance. As explained in the Introduction, the AD5933 integrated circuit impedance converter combines an internal DDS frequency generator and ADC to form a self-contained impedance measurement system. A frequency sweep is performed by the AD5933 to typically gather magnitude and phase data at frequencies defined by the user. In Figure 2, the impedance to be analyzed is placed between the sense resistor and ground. The AD8220 is used to measure the current in the sense resistor. The AD8220 output signal is then passed through a programmable gain amplifier (PGA), filtered and then delivered to the 12-bit ADC. After the receive signal is digitized by the ADC, a DFT is performed on the data.

A nearby microcontroller communicates to the AD5933 via the I²C interface, allowing the user to program the AD5933 sweep parameters (start frequency, frequency step size, and number of points) configure the control register, adjust the excitation amplitude and PGA setting, as well as read back the measured data from the AD5933 for the final impedance calculation. Once the AD5933 is correctly programmed, only a single bit in the status register at each point in the user defined sweep must be polled to see if valid data is available to read from the AD5933 (see the AD5933 data sheet for more details).

SYSTEM CALIBRATION

However, prior to a valid impedance measurement, the AD5933 system shown in Figure 2 must undergo a calibration process. The calibration process requires that a known precision imped-ance be substituted for the subsequent unknown impedance to be measured and a scaling factor (gain factor) is calculated for subsequent measurements. As described in the System Gain Factor section, the gain factor for this circuit is given in Equation 17:

$$Gain\ Factor = \left(\frac{\frac{1}{Z_{CALIBRATION} + R_{SENSE}}}{\sqrt{R^2 + I^2}} \right) \quad (17)$$

where:
R and I are the contents of the real and imaginary register (94h to 97h) at the chosen calibration frequency point.
$Z_{CALIBRATION}$ is the known calibration impedance.
R_{SENSE} is the chosen sense resistor.

The gain factor is calculated by dividing the sum of a known precision impedance and sense resistor by the magnitude of the real and imaginary data returned at a suitable midpoint frequency in the sweep. Both the real and imaginary com-ponent are stored in two, 16-bit registers which must be read after each ADC conversion, and before the next frequency point in the sweep, where the contents of these two registers are refreshed with new data.

The grounded complex impedance ranges between 20 kΩ and 60 kΩ. Therefore, the calibration impedance was chosen to have a value of ≈40 kΩ and the sense resistor was 2.67 kΩ.

GROUNDED IMPEDANCE CALCULATION

Once the calibration process is finished, the unknown complex impedance replaces the calibration impedance. After the user issues a start frequency sweep command to the control register, the AD5933 automatically sequences through the user-defined frequency sweep. The frequency sweep is calculated by contents of the three registers (start frequency, frequency step, and number of increments register). Finally, the microprocessor communicating to the AD5933 calculates the grounded impedance at each frequency point by multiplying the gain factor by the magnitude of the complex code returned at each frequency by the AD5933 and inverting the answer. The sense resistor is subtracted in the final calculation. The impedance at each frequency point is given by Equation 18.

$$Z\ Complex\ Impedance = \frac{1}{Gain\ Factor \times \sqrt{\left(R^2 + I^2 \right)}} - R_{SENSE} \quad (18)$$

Where R and I are the contents of the real and imaginary registers (94h to 97h) at each frequency sweep point.

SYSTEM CLOCK SETTINGS

The frequency of the clock applied to MCLK (Pin 8) is set to 16 MHz using a stable, low jitter, quartz crystal oscillator. This allows the AD5933 to analyze excitation frequencies from 99.9 kHz to 100.1 kHz. Table 3 lists the programmed sweep parameters (start frequency, frequency increment, and number of increments) used in the test to cover the 99.9 kHz to 100.1 kHz bandwidth. The frequency step size was set to 1 Hz and the number of sweep points was set to 200. The number of settling time cycles register was set at 15 output cycles throughout the experiment. The circuit in Figure 2 was calibrated at a frequency of 100 kHz.

As described in the AD5933 data sheet register map, the start frequency is a 24-bit word that is programmed to the on-board RAM at Address 82h, Address 83h, and Address 84h. The required code loaded to the start frequency register is the result of the formula in Equation 19, based on the master clock frequency and the required start frequency output from the DDS.

$$Start\ Frequency\ Code = \left(\frac{Required\ Output\ Start\ Frequency}{\left(\frac{MCLK}{4}\right)}\right) \times 2^{27}$$

(19)

For example, refer to the first column of Table 3. If the user requires the sweep to begin at 99.9 kHz and has a 16 MHz clock signal connected to MCLK, the code that must be programmed is given by Equation 20:

$$Start\ Frequency\ Code = \left(\frac{99.9\,\text{kHz}}{\left(\frac{16\,\text{MHz}}{4}\right)}\right) \times 2^{27} \equiv 332617\ \text{hexadecimal}$$

(20)

The user programs 33 hex to Register 82 h, 26 hex to Register 83 h, and 17 hex to Register 84 h.

Similarly, the frequency increment register is a 24-bit word that is programmed to the on-board RAM at Address 85 h, Address 86 h, and Address 87 h (see the AD5933 data sheet register map). The required code loaded to the frequency increment register is also the result of the formula shown in Equation 21, based on the master clock frequency and the required increment frequency output from the DDS.

$$Frequency\ Increment\ Code = \left(\frac{Required\ Frequency\ Increment}{\left(\frac{MCLK}{4}\right)}\right) \times 2^{27}$$

(21)

For example, if the user requires the sweep to have a resolution of 1 Hz and has a 16 MHz clock signal connected to MCLK, the code that needs to be programmed is given Equation 22:

$$Frequency\ Increment\ Code = \left(\frac{1\,\text{Hz}}{\left(\frac{16\,\text{MHz}}{4}\right)}\right) \equiv 000021\ \text{hexadecimal}$$

(22)

The user programs 00 hex to Register 85 h, 00 hex to Register 86 h, and 21 hex to Register 87 h.

The third parameter to define the frequency sweep is the number of increments register. This is a 9-bit word that represents the number of frequency points in the sweep. The number is programmed to the on-board RAM at Address 88 h and Address 89 h. The maximum number of points that can be programmed is 511. For example, if the sweep needs 200 points, the user programs 00 hex to Register 88 h and C8 hex to Register 89 h. Table 3 shows a summary of the required sweep codes for a 16 MHz clock frequency. The settling time cycles register was set to a value of 15 by programming 0F hex to Register 8B hex.

Table 3. AD5933 Required Sweep Codes for Frequency Range 99.9 kHz to 100.1 kHz

Programmed Start Frequency	Required Start Frequency Code	Programmed Frequency Increment	Required Frequency Increment Code	Programmed No. of Increments	Required No. of Increments Code	Clock Frequency Applied to MCLK Pin
99.9 kHz	332617 hex	1 Hz	000021 hex	200	00C8 hex	16 MHz

RESULTS

The system in Figure 2 was calibrated with a 35 kΩ impedance and a sense resistor of 2.67 kΩ (midpoint between 20 kΩ and 60 kΩ), and the gain factor was calculated at a calibration frequency of 100 kHz (the midpoint in the sweep) using the sweep dial up codes outlined in Table 3. The calculated calibration gain factor was stored in memory in a nearby microcontroller. The calibration impedance was replaced by a range of complex grounded impedances which varied between 20 kΩ to 60 kΩ. A frequency sweep was carried by the AD5933, and the measured impedance was calculated at each frequency point by multiplying the stored gain factor by code at each frequency and inverting the answer, as shown in Equation 23 and Equation 24.

$$Gain\ Factor = \left(\frac{1}{\frac{Z_{CALIBRATION} + R_{SENSE}}{\sqrt{R^2 + I^2}}} \right) \tag{23}$$

$$Z\ Complex\ Impedance = \frac{1}{Gain\ Factor \times \sqrt{(R^2 + I^2)}} - R_{SENSE} \tag{24}$$

A plot of percentage impedance error vs. frequency for the grounded impedance at the calibration frequency of 100 kHz is shown in Figure 13.
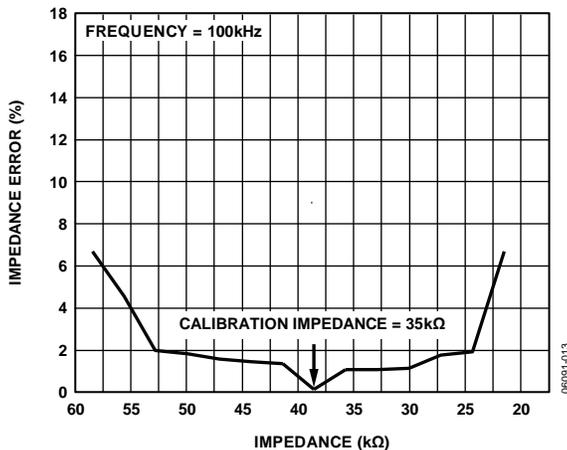

Figure 13. Grounded Impedance Measurement Results by AD5933 at 100 kHz

Figure 13 shows that at the calibration frequency of 100 kHz, the percentage impedance error is zero at the calibration impedance of 35 kΩ and increases from this point. The results of the measurement in Figure 13 show that there is less than 7% impedance error over the entire 60 kΩ range as a result of the single-point calibration. A reduction in error can be achieved by calibrating over a reduced impedance range.

CONCLUSION

The AD5933 provides an accurate low cost solution to grounded impedance measurement compared to the traditional and expensive multichip-based solutions. Along with the AD5933, only a few external support components are required to incorporate the simple test circuitry to a nearby grounded sensor with minimum board space. The impedance profile of the grounded sensor can be evaluated upon system power-up with minimal effort, providing a simple means of characterizing the sensor impedance profile, examining the effects of aging and damage, and identifying changes.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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