

AD9929: HD/CLI Timing Relationship in Slave Mode

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INTRODUCTION

When operating the AD9929 in slave mode, the relationship between HD and CLI is critical to insure proper resetting of the internal counters. The HD signal is used to reset several internal counters. Under certain timing conditions, it is possible for the counter reset location to vary by ± 1 pixel at hot or cold temperatures.

HD AND CLI PHASE RELATIONSHIP

The external HD signal is latched by an internal clock that is generated by a combination of the master clock, CLI, and the value programmed to the SHDLOC register (Register 0x02, Bits[21:16]). As shown in Figure 1, t_{HDCLI} is defined as the time from the falling edge of HD to the rising edge of CLI. This definition is used when describing the invalid HD to CLI relationship for a given SHDLOC value.

For operation at 36 MHz and SHDLOC = 0x0, the invalid values for t_{HDCLI} are from 18.8 ns to 24.8 ns. The invalid region shifts with SHDLOC and is governed by the following equations:

$$\text{Minimum } t_{HDCLI} = 18.8 \text{ ns} - (27.8 \text{ ns}/48) \times SHDLOC(\text{decimal})$$

$$\text{Maximum } t_{HDCLI} = 24.8 \text{ ns} - (27.8 \text{ ns}/48) \times SHDLOC(\text{decimal})$$

where 27.8 ns is the period of CLI (t_{CONV}) at 36 MHz. For example, for 36 MHz operation and SHDLOC = tap 4, the inhibit region for t_{HDCLI} would be derived in the following way:

$$\text{Minimum } t_{HDCLI} = 18.8 \text{ ns} - (27.8 \text{ ns}/48) \times 4 = 16.5 \text{ ns}$$

$$\text{Maximum } t_{HDCLI} = 24.8 \text{ ns} - (27.8 \text{ ns}/48) \times 4 = 22.5 \text{ ns}$$

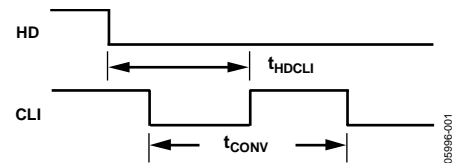


Figure 1. HD-to-CLI Phase Relationship

HD-TO-CLI TIMING SPECIFICATIONS

AVDD = TCVDVDD = DVDD = 2.7 V to 3.6 V, -25°C to $+85^{\circ}\text{C}$, H1BLKRETIME = 1, SHDLOC = 0.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit
Invalid HD-to-CLI Timing Relationship	t_{HDCLI}	18.8	21.8	24.8	ns

AN-842

NOTES