Data Sheet

ADA4099-1/ADA4099-2

50 V, 8 MHz, 1.5 mA per Channel, Robust, Over-The-Top, Precision Op Amps

FEATURES

- Ultrawide common-mode range: $-V_S - 0.1$ V to $-V_S + 70$ V
- Wide power supply voltage range: (V_{SY}): +3.15 V to +50 V (±25 V for PSRR)
- Low supply current: 1.5 mA per channel (typical)
- Low input offset voltage: ±40 µV maximum
- Low input offset voltage drift: ±0.4 µV/°C maximum
- Low voltage noise:
  - 1/f noise corner: 6 Hz typical
  - 150 nV p-p typical at 0.1 Hz to 10 Hz
  - 7 nV/√Hz typical at 100 Hz (e_n)
- High speed
  - GBP: 8 MHz typical
  - Slew rate: 5.5 V/µs typical at ΔV_{OUT} = 25 V
- Low power shutdown: 20 µA maximum
- Low input bias current: ±10 nA maximum
- Large signal voltage gain: 120 dB minimum
- CMRR: 118 dB, minimum
- PSRR: 123 dB, minimum
- Input overdrive tolerant with no phase reversal
- ±2 kV HBM and ±1.25 kV FICDM
- Wide temperature range: −55°C to +150°C (H grade)

APPLICATIONS

- Industrial sensor conditioning
- Supply current sensing
- Battery and power supply monitoring
- Front-end amplifiers in abusive environments
- 4 mA to 20 mA transmitters

GENERAL DESCRIPTION

The ADA4099-1 and ADA4099-2 are single/dual robust, precision, rail-to-rail input/output operational amplifiers (op amps) with inputs that operate from $-V_S$ to $+V_S$ and beyond, which is referred to in this data sheet as Over-The-Top™. The devices feature offset voltages of <40 µV, input bias currents (I_B) of <10 nA, and can operate on single or split supplies that range from 3.15 V to 50 V. The ADA4099-1 and ADA4099-2 draws 1.5 mA of quiescent current per channel.

The ADA4099-1 and ADA4099-2 Over-The-Top input stages have robust input protection features for abusive environments. The inputs can tolerate up to 80 V of differential voltage without damage or degradation to dc accuracy. The operating input common-mode range extends from rail-to-rail and beyond, up to 70 V > $-V_S$, independent of the $+V_S$ supply.

The ADA4099-1 and ADA4099-2 are unity-gain stable and can drive loads requiring up to 20 mA per channel. The device can also drive capacitive loads as large as 100 pF. The amplifiers are available with low power shutdown.

The ADA4099-1 is available in a standard, 6-lead, thin small outline transistor (TSOT) package. The ADA4099-2 is available in an 8-lead, standard small outline package (SOIC_N), 8-lead, mini small outline package (MSOP), and a 10-lead, lead frame chip scale package (LFCSP).

TYPICAL APPLICATION CIRCUIT

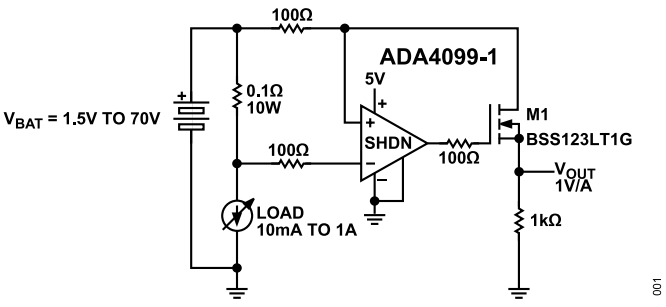

Figure 1. 1 V/A Over-The-Top Current Sense Application (ADA4099-1 6-lead TSOT)

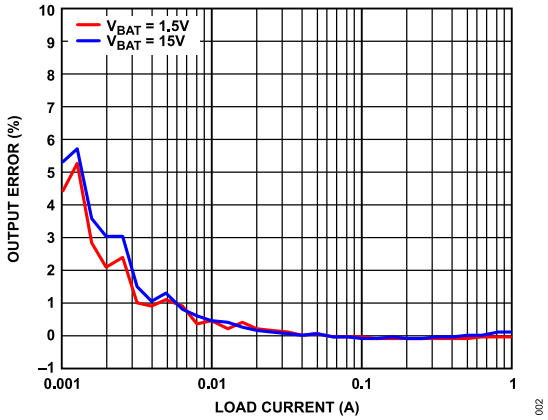

Figure 2. Output Error vs. Load Current

Rev. A

DOCUMENT FEEDBACK

TECHNICAL SUPPORT

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1/2021—Revision 0: Initial Version

SPECIFICATIONS

5 V SUPPLY

Common-mode voltage (V_{CM}) = 2.5 V, SHDN pin (ADA4099-1) and SHDNx pins (ADA4099-2 10-lead LFCSP) are open, load resistance (R_L) = 499 kΩ to midsupply, ambient temperature (T_A) = 25°C, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	B Grade			H Grade			Unit
		Min	Typ	Max	Min	Typ	Max	
DC PERFORMANCE								
Input Offset Voltage (V_{OS})[1]	0.25 V < V_{CM} < 3.25 V		±10	±40		±10	±40	µV
	Minimum temperature (T_{MIN}) < T_A < maximum temperature (T_{MAX})			±90			±90	µV
	0.25 V < V_{CM} < 70 V		±25	±65		±25	±65	µV
	T_{MIN} < T_A < T_{MAX}			±125			±140	µV
	−0.1 V < V_{CM} < +70 V		±25	±70		±25	±70	µV
	T_{MIN} < T_A < T_{MAX}			±125			±200	µV
Input Offset Voltage Drift[2]	T_{MIN} < T_A < T_{MAX}		±0.1	±0.4		±0.1	±0.8	µV/°C
Input Bias Current (I_B)			±4	±10		±4	±10	nA
	T_{MIN} < T_A < T_{MAX}			±15			±30	nA
	V_{CM} = 70 V, Over-The-Top	70	82.5	98	70	82.5	98	µA
	T_{MIN} < T_A < T_{MAX}	40		125	40		125	µA
	0 V < V_{CM} < 70 V, V_{SY} = 0 V		0.001	10		0.001	10	µA
	T_{MIN} < T_A < T_{MAX}			25			25	µA
Input Offset Current (I_{OS})			±2	±4		±2	±4	nA
	T_{MIN} < T_A < T_{MAX}			±10			±20	nA
	V_{CM} = 70 V, Over-The-Top[3]		±0.5	±2		±0.5	±2	µA
	T_{MIN} < T_A < T_{MAX}			±5			±5	µA
Common-Mode Rejection Ratio (CMRR)	V_{CM} = −0.1 V to +70 V	118	136		118	136		dB
	T_{MIN} < T_A < T_{MAX}	110			108			dB
	V_{CM} = 0.25 V to 3.25 V	114	132		114	132		dB
	T_{MIN} < T_A < T_{MAX}	108			108			dB
Common-Mode Input Range	Guaranteed by CMRR tests	$-V_S$ − 0.1		$-V_S$ + 70	$-V_S$ − 0.1		$-V_S$ + 70	V
Large Signal Voltage Gain (A_{OL})	ΔV_{OUT} = 4 V	126	140		126	140		dB
	T_{MIN} < T_A < T_{MAX}	116			110			dB
	ΔV_{OUT} = 4 V, R_L = 10 kΩ	120	130		120	130		dB
	T_{MIN} < T_A < T_{MAX}	110			102			dB
NOISE PERFORMANCE								
Input Voltage Noise	Frequency (f) = 0.1 Hz to 10 Hz		150			150		nV p-p
	1/f noise corner		6			6		Hz
	f = 100 Hz		7			7		nV/√Hz
Over-The-Top	f = 100 Hz, V_{CM} > 5 V		8			8		nV/√Hz
Input Current Noise	f = 100 Hz		0.5			0.5		pA/√Hz
Over-The-Top	f = 100 Hz, V_{CM} > 5 V		5			5		pA/√Hz
DYNAMIC PERFORMANCE								
Slew Rate	ΔV_{OUT} = 2 V	2.7	4		2.7	4		V/µs
	T_{MIN} < T_A < T_{MAX}	1.75			1.75			V/µs
Gain Bandwidth Product (GBP)	Test frequency (f_{TEST}) = 25 kHz	7.5	8		7.5	8		MHz
	T_{MIN} < T_A < T_{MAX}	6.75			6.5			MHz
Phase Margin			47			47		Degrees
1% Settling Time	ΔV_{OUT} = ±2 V		1.15			1.15		µs

SPECIFICATIONS

Table 1.

Parameter	Test Conditions/Comments	B Grade			H Grade			Unit
		Min	Typ	Max	Min	Typ	Max	
0.1% Settling Time	ΔV_{OUT} = ±2 V		1.5			1.5		µs
Total Harmonic Distortion Plus Noise (THD + N)	f = 10 kHz, V_{OUT} = 2 V p-p, R_L = 10 kΩ, bandwidth = 80 kHz		0.001			0.001		%
Channel Separation	f = 1 kHz, R_L = 2 kΩ		115			115		dB
INPUT CHARACTERISTICS								
Input Resistance	Differential mode		100			100		kΩ
	Common mode		>1			>1		GΩ
Over-The-Top	Differential mode, V_{CM} > 5 V		600			600		Ω
	Common mode, V_{CM} > 5 V		>100			>100		MΩ
Input Capacitance	Differential mode		9			9		pF
	Common mode		3			3		pF
SHDN AND SHDNx PINS								
Input Logic Low	Amplifier active, SHDN and SHDNx voltage (V_{SHDN}) < $-V_S$ + 0.5 V, T_{MIN} < T_A < T_{MAX}			$-V_S$ + 0.5			$-V_S$ + 0.5	V
Input Logic High	Amplifier shutdown, V_{SHDN} > $-V_S$ + 1.5 V, T_{MIN} < T_A < T_{MAX}	$-V_S$ + 1.5			$-V_S$ + 1.5			V
Response Time	Amplifier active to shutdown		2.5			2.5		µs
	Amplifier shutdown to active		10			10		µs
Pull-Down Current	V_{SHDN} = $-V_S$ + 0.5 V, T_{MIN} < T_A < T_{MAX}		0.6	3		0.6	3	µA
	V_{SHDN} = $-V_S$ + 1.5 V, T_{MIN} < T_A < T_{MAX}		0.3	2.5		0.3	2.5	µA
OUTPUT CHARACTERISTICS								
Output Voltage Swing Low	Overdrive voltage (V_{OD}[4]) = 30 mV, no load		45	60		45	60	mV
	T_{MIN} < T_A < T_{MAX}			105			120	mV
	V_{OD} = 30 mV, sink current, (I_{SINK}) = 10 mA		260	325		260	325	mV
	T_{MIN} < T_A < T_{MAX}			435			450	mV
Output Voltage Swing High	V_{OD} = 30 mV, no load		45	55		45	55	mV
	T_{MIN} < T_A < T_{MAX}			110			140	mV
	V_{OD} = 30 mV, source current, (I_{SOURCE}) = 10 mA		900	1100		900	1100	mV
	T_{MIN} < T_A < T_{MAX}			1500			1650	mV
Short-Circuit Current	I_{SOURCE}	20	30		20	30		mA
	T_{MIN}< T_A < T_{MAX}	15			15			mA
	I_{SINK}	40	50		40	50		mA
	T_{MIN} < T_A < T_{MAX}	20			20			mA
Output Pin Leakage During Shutdown	V_{SHDN} = $-V_S$ + 1.5 V		±0.01	±100		±0.01	±100	nA
	T_{MIN} < T_A < T_{MAX}			±10			±10	µA
POWER SUPPLY								
Maximum Operating Voltage[5]				50			50	V
Voltage Range	Guaranteed by power supply rejection ratio (PSRR)	3.15		50	3.15		50	V
Supply Current/Channel	Amplifier active		1.5	1.6		1.5	1.6	mA
	T_{MIN} < T_A < T_{MAX}			2.2			2.35	mA
	Amplifier shutdown V_{SHDN} = $-V_S$ + 1.5 V		12	20		12	20	µA
	T_{MIN} < T_A < T_{MAX}			22.5			22.5	µA

SPECIFICATIONS

Table 1.

Parameter	Test Conditions/Comments	B Grade			H Grade			Unit
		Min	Typ	Max	Min	Typ	Max	
PSRR	V_{SY} = 3.15 V to ±25 V	123	136		123	136		dB
	$T_{MIN} < T_A < T_{MAX}$	119			120			dB
THERMAL SHUTDOWN[6]								
Temperature	Junction temperature (T_J)		175			175		°C
Hysteresis			20			20		°C
Operating Temperature	Ambient temperature (T_A)	−40		+125	−55		+150	°C

[1] Thermoelectric voltages present in the high speed production test limit the measurement accuracy of this parameter. The limits shown in Table 1 are determined by test capability and are not necessarily indicative of actual device performance.

[2] Offset voltage drift is guaranteed through lab characterization and is not production tested.

[3] Test accuracy is limited by high speed production test equipment repeatability. Bench measurements indicate that the input offset current in Over-The-Top configuration is typically controlled to under 250 nA at +25°C and 1000 nA over the −55°C < T_A < +150°C temperature range.

[4] V_{OD} is +30 mV for V_{OUT} high and −30 mV for V_{OUT} low.

[5] Maximum operating voltage is limited by the time-dependent dielectric breakdown (TDDB) of on-chip capacitor oxides. The amplifier tolerates temporary transient overshoot up to the specified absolute maximum rating, but the dc supply voltage must be limited to the maximum operating voltage.

[6] Thermal shutdown is lab characterized only and is not tested in production.

±15 V SUPPLY

V_{CM} = 0 V, SHDN pin (ADA4099-1) and SHDNx pins (ADA4099-2 10-lead LFCSP) are open, R_L = 499 kΩ to ground, and T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	B Grade			H Grade			Unit
		Min	Typ	Max	Min	Typ	Max	
DC PERFORMANCE								
Input Offset Voltage (V_{OS})[1]			±12	±40		±12	±40	µV
	$T_{MIN} < T_A < T_{MAX}$			±95			±90	µV
	V_{SY} = ±25 V		±15	±40		±15	±40	µV
	$T_{MIN} < T_A < T_{MAX}$			±105			±90	µV
Input Offset Voltage Drift[2]	$T_{MIN} < T_A < T_{MAX}$		±0.1	±0.4		±0.1	±0.9	µV/°C
Input Bias Current			±4	±10		±4	±10	nA
	$T_{MIN} < T_A < T_{MAX}$			±25			±60	nA
	V_{SY} = ±25 V		±4	±10		±4	±10	nA
	$T_{MIN} < T_A < T_{MAX}$			±35			±100	nA
Input Offset Current			±2	±5		±2	±5	nA
	$T_{MIN} < T_A < T_{MAX}$			±15			±30	nA
	V_{SY} = ±25 V		±4	±5		±4	±5	nA
	$T_{MIN} < T_A < T_{MAX}$			±20			±35	nA
CMRR	V_{CM} = −14.75 V to +13.25 V	118	130		118	130		dB
	$T_{MIN} < T_A < T_{MAX}$	112			114			dB
	V_{CM} = −15.1 V to +13.25 V	115	126		115	126		dB
	$T_{MIN} < T_A < T_{MAX}$	105			101			dB
	V_{CM} = −15.1 V to +55 V	117	126		117	126		dB
	$T_{MIN} < T_A < T_{MAX}$	110			107			dB
Common-Mode Input Range	Guaranteed by CMRR tests	−15.1		+55	−15.1		+55	V

SPECIFICATIONS

Table 2.

Parameter	Test Conditions/Comments	B Grade			H Grade			Unit
		Min	Typ	Max	Min	Typ	Max	
A_{OL}	ΔV_{OUT} = 25 V	134	154		134	154		dB
	$T_{MIN} < T_A < T_{MAX}$	120			116			dB
	ΔV_{OUT} = 25 V, R_L =10 kΩ	120	134		120	134		dB
	$T_{MIN} < T_A < T_{MAX}$	114			110			dB
NOISE PERFORMANCE								
Input Voltage Noise	f = 0.1 Hz to 10 Hz		150			150		nV p-p
	1/f noise corner		6			6		Hz
	f = 100 Hz		7			7		nV/√Hz
Over-The-Top	f = 100 Hz, $V_{CM} > +V_S$		8			8		nV/√Hz
Input Current Noise	f = 100 Hz		0.5			0.5		pA/√Hz
Over-The-Top	f = 100 Hz, $V_{CM} > +V_S$		5			5		pA/√Hz
DYNAMIC PERFORMANCE								
Slew Rate	ΔV_{OUT} = 25 V	3.5	5.5		3.5	5.5		V/µs
	$T_{MIN} < T_A < T_{MAX}$	2.0			2.0			V/µs
GBP	f_{TEST} = 25 kHz	7.5	8		7.5	8		MHz
	$T_{MIN} < T_A < T_{MAX}$	6.75			6.5			MHz
Phase Margin			57			57		Degrees
1% Settling Time	ΔV_{OUT} = ±2 V		1.15			1.15		µs
0.1% Settling Time	ΔV_{OUT} = ±2 V		1.5			1.5		µs
THD + N	f = 10 kHz, V_{OUT} = 5.6 V p-p, R_L = 10 kΩ, bandwidth = 80 kHz		0.001			0.001		%
Channel Separation	f = 1 kHz, R_L = 2 kΩ		115			115		dB
INPUT CHARACTERISTICS								
Input Resistance	Differential mode		100			100		kΩ
	Common mode		>1			>1		GΩ
Input Capacitance	Differential mode		9			9		pF
	Common mode		3			3		pF
SHDN AND SHDNx PINS								
Input Logic Low	Amplifier active, $V_{SHDN} < -V_S + 0.5$ V			$-V_S + 0.5$			$-V_S + 0.5$	V
Input Logic High	Amplifier shutdown, $V_{SHDN} > -V_S + 1.5$ V	$-V_S + 1.5$			$-V_S + 1.5$			V
Response Time	Amplifier active to shutdown		2.5			2.5		µs
	Amplifier shutdown to active		10			10		µs
Pull-Down Current	$V_{SHDN} = -V_S + 0.5$ V, $T_{MIN} < T_A < T_{MAX}$		0.6	3		0.6	3	µA
	$V_{SHDN} = -V_S + 1.5$ V, $T_{MIN} < T_A < T_{MAX}$		0.3	2.5		0.3	2.5	µA
OUTPUT CHARACTERISTICS								
Output Voltage Swing Low	V_{OD}[3] = 30 mV, no load		45	60		45	60	mV
	$T_{MIN} < T_A < T_{MAX}$			115			125	mV
	V_{OD} = 30 mV, I_{SINK} = 10 mA		260	325		260	325	mV
	$T_{MIN} < T_A < T_{MAX}$			435			450	mV
Output Voltage Swing High	V_{OD} = 30 mV, no load		45	55		45	55	mV
	$T_{MIN} < T_A < T_{MAX}$			140			165	mV
	V_{OD} = 30 mV, I_{SOURCE} = 10 mA		900	1100		900	1100	mV
	$T_{MIN} < T_A < T_{MAX}$			1500			1650	mV

SPECIFICATIONS

Table 2.

Parameter	Test Conditions/Comments	B Grade			H Grade			Unit
		Min	Typ	Max	Min	Typ	Max	
Short-Circuit Current	I_{SOURCE}	25	34		25	34		mA
	$T_{MIN} < T_A < T_{MAX}$	20			20			mA
	I_{SINK}	40	50		40	50		mA
	$T_{MIN} < T_A < T_{MAX}$	20			20			mA
POWER SUPPLY								
Maximum Operating Voltage[4]				50			50	V
Voltage Range	Guaranteed by PSRR	3.15		50	3.15		50	V
Supply Current/Channel	Amplifier active		1.65	1.8		1.65	1.8	mA
	$T_{MIN} < T_A < T_{MAX}$			2.45			2.6	mA
	V_{SY} = ±25 V		1.75	2		1.75	2	mA
	$T_{MIN} < T_A < T_{MAX}$			2.7			2.85	mA
	Amplifier shutdown, $V_{SHDN} = -V_S + 1.5$ V		17	24		17	24	µA
	$T_{MIN} < T_A < T_{MAX}$			27			27	µA
PSRR	V_{SY} = 3.15 V to 50 V	123	136		123	136		dB
	$T_{MIN} < T_A < T_{MAX}$	119			120			dB
THERMAL SHUTDOWN[5]								
Temperature	T_J		175			175		°C
Hysteresis			20			20		°C
Operating Temperature	T_A	−40		+125	−55		+150	°C

[1] Thermoelectric voltages present in the high speed production test limit the measurement accuracy of this parameter. The limits shown in Table 2 are determined by test capability and are not necessarily indicative of actual device performance.

[2] Offset voltage drift is guaranteed through lab characterization and is not production tested.

[3] V_{OD} is +30 mV for V_{OUT} high and −30 mV for V_{OUT} low.

[4] Maximum operating voltage is limited by the TDDB of on-chip capacitor oxides. The amplifier tolerates temporary transient overshoot up to the specified absolute maximum rating and the dc supply voltage must be limited to the maximum operating voltage.

[5] Thermal shutdown is lab characterized only and is not tested in production.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage[1]	
Transient	60 V
Continuous	50 V
Power Dissipation (P_D)	See Figure 3
Differential Input Voltage	±80 V
±IN Pin Voltage	
Continuous	−5 V to +80 V
Survival	−10 V to +80 V
±IN Pin Current	20 mA
SHDN and SHDNx Voltage[2]	−0.3 V to +60 V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C
Junction Temperature (T_J)	175°C

[1] Maximum supply voltage is limited by the TDDB of on-chip capacitor oxides. The amplifiers tolerate temporary transient overshoot up to the specified transient maximum rating. The continuous operating supply voltage must be limited to no more than 50 V.

[2] SHDN is Pin 5 on the ADA4099-1. SHDNx refers to SHDN1 and SHDN2 (Pin 5 and Pin 6, respectively) on the ADA4099-2 10-lead LFCSP).

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Junction temperatures (T_J) exceeding 125°C promote accelerated aging. The ADA4099-1 and ADA4099-2 demonstrates ±25 V supply operation beyond 1400 hours at T_A = 140°C.

MAXIMUM POWER DISSIPATION

The maximum safe power dissipation (P_D) on the device is limited by the associated rise in either case temperature (T_C) or T_J on the die. At approximately T_C = 150°C, which is the glass transition temperature, the properties of the plastic changes. Exceeding this temperature limit, even temporarily, may change the stresses that the package exerts on the die, which permanently shifts the parametric performance of the ADA4099-1 and ADA4099-2. Exceeding T_J = 175°C for an extended period may result in changes in the silicon devices and may cause failure of the device.

The P_D on the package is the sum of the quiescent power dissipation and the power dissipated in the package due to the output load drive. The quiescent power is expressed in the following equation:

$$V_{SY} \times I_{SY}$$

where I_{SY} is the quiescent current.

The P_D due to the load drive depends on the application. The P_D due to load drive is calculated by multiplying the load current by the associated voltage drop across the device. RMS voltages and currents must be used in these calculations.

Airflow increases heat dissipation, effectively reducing θ_{JA}. Additional metal that is directly in contact with the package leads from metal traces through vias, ground, and power planes reduces θ_{JA}.

Figure 3 shows the maximum P_D vs. T_A for the single and dual 6-lead TSOT packages on a JEDEC standard, 4-layer board, with $-V_S$ connected to a pad that is thermally connected to a printed circuit board (PCB) plane. θ_{JA} values are approximations.

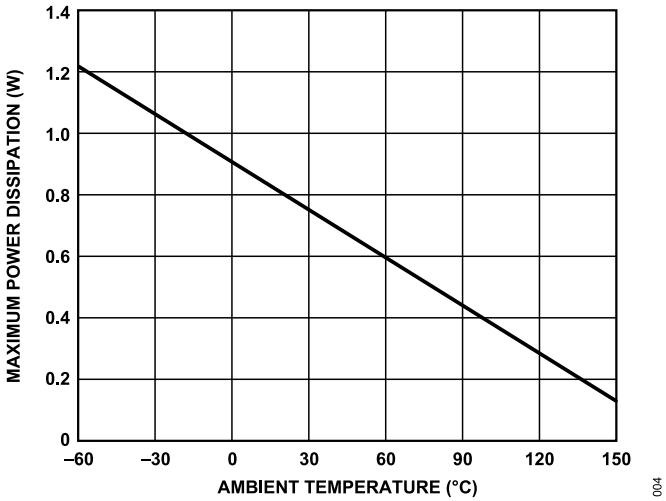


Figure 3. Maximum Power Dissipation vs. Ambient Temperature

THERMAL RESISTANCE

Thermal performance is directly linked to PCB design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the junction to ambient thermal resistance.

Table 4. Thermal Resistance

Package Type	θ_{JA}	Unit
UJ-6	192	°C/W
R-8	120	°C/W
RM-8	163	°C/W
05-08-1699	43	°C/W

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Field induced charged device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

ABSOLUTE MAXIMUM RATINGS

ESD Ratings for ADA4099-1 and ADA4099-2

Table 5. ADA4099-1 6-Lead TSOT, ADA4099-2 8-Lead SOIC_N, ADA4099-2 8-Lead MSOP, ADA4099-2 10-Lead LFCSP

ESD Model	Withstand Threshold (kV)	Class
HBM	±2	2
FICDM	±1.25	3

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

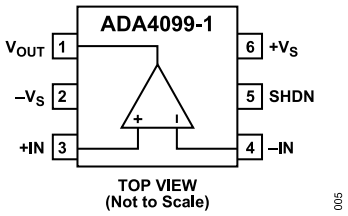


Figure 4. Pin Configuration for ADA4099-1 6-Lead TSOT

Table 6. Pin Function Descriptions for ADA4099-1 6-Lead TSOT

Pin No.	Mnemonic	Description
1	V_{OUT}	Amplifier Output.
2	$-V_S$	Negative Power Supply. In single-supply applications, this pin is normally soldered to a low impedance ground plane. In split supply applications, bypass this pin with a capacitance of at least 0.1 µF to a low impedance ground plane, as close to the pin as possible.
3	+IN	Noninverting Input of the Amplifier.
4	−IN	Inverting Input of the Amplifier.
5	SHDN	Op Amp Shutdown. The threshold for shutdown is approximately 1 V above the negative supply. If this pin is not connected or hard tied to $-V_S$, the amplifier is active. If asserted high ($V_{SHDN} > -V_S + 1.5$ V), the amplifier is placed in a shutdown state, and the output of the amplifier goes to a high impedance state. If this pin is left unconnected, it is recommended to connect a small capacitor of 1 nF between SHDN and $-V_S$ to prevent signals from −IN from capacitively coupling to the SHDN pin.
6	$+V_S$	Positive Power Supply. Bypass this pin with a capacitance of at least 0.1 µF to a low impedance ground plane, as close to the pin as possible.

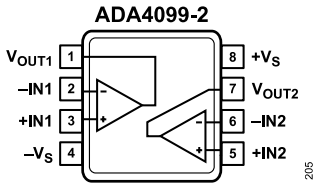


Figure 5. Pin Configuration for ADA4099-2 8-Lead SOIC_N and 8-Lead MSOP

Table 7. Pin Function Descriptions for ADA4099-2 8-Lead SOIC_N and 8-Lead MSOP

Pin No.	Mnemonic	Description
1	V_{OUT1}	Amplifier Output, Channel 1.
2	−IN1	Inverting Input of the Amplifier, Channel 1.
3	+IN1	Noninverting Input of the Amplifier, Channel 1.
4	$-V_S$	Negative Power Supply. In single-supply applications, this pin is normally soldered to a low impedance ground plane. In split supply applications, bypass this pin with a capacitance of at least 0.1 µF to a low impedance ground plane, as close to the pin as possible.
5	+IN2	Inverting Input of the Amplifier, Channel 2.
6	−IN2	Noninverting Input of the Amplifier, Channel 2.
7	V_{OUT2}	Amplifier Output, Channel 2.
8	$+V_S$	Positive Power Supply. Bypass this pin with a capacitance of at least 0.1 µF to a low impedance ground plane, as close to the pin as possible.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

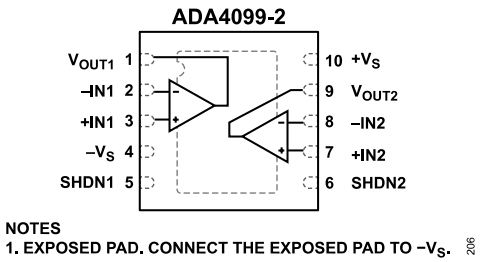


Figure 6. Pin Configuration for ADA4099-2 10-Lead LFCSP

Table 8. Pin Function Descriptions for ADA4099-2 10-Lead LFCSP

Pin No.	Mnemonic	Description
1	V_{OUT1}	Amplifier Output, Channel 1.
2	−IN1	Inverting Input of the Amplifier, Channel 1.
3	+IN1	Noninverting Input of the Amplifier, Channel 1.
4	$-V_S$	Negative Power Supply. In single-supply applications, this pin is normally soldered to a low impedance ground plane. In split supply applications, bypass this pin with a capacitance of at least 0.1 µF to a low impedance ground plane, as close to the pin as possible.
5	SHDN1	Op Amp Shutdown, Channel 1. The threshold for shutdown is approximately 1 V above the negative supply. If this pin is not connected or hard tied to $-V_S$, the amplifier is active. If asserted high ($V_{SHDN} > -V_S + 1.5$ V), the amplifier is placed in a shutdown state, and the output of the amplifier goes to a high impedance state. If this pin is left unconnected, it is recommended to connect a small capacitor of 1 nF between SHDN1 and $-V_S$ to prevent signals from −IN from capacitively coupling to the SHDN1 pin.
6	SHDN2	Op Amp Shutdown, Channel 2. The threshold for shutdown is approximately 1 V above the negative supply. If this pin is not connected or hard tied to $-V_S$, the amplifier is active. If asserted high ($V_{SHDN} > -V_S + 1.5$ V), the amplifier is placed in a shutdown state, and the output of the amplifier goes to a high impedance state. If this pin is left unconnected, it is recommended to connect a small capacitor of 1 nF between SHDN2 and $-V_S$ to prevent signals from −IN from capacitively coupling to the SHDN2 pin.
7	+IN2	Inverting Input of the Amplifier, Channel 2.
8	−IN2	Noninverting Input of the Amplifier, Channel 2.
9	V_{OUT2}	Amplifier Output, Channel 2.
10	$+V_S$	Positive Power Supply. Bypass this pin with a capacitance of at least 0.1 µF to a low impedance ground plane, as close to the pin as possible.
	EPAD	Exposed Pad. Connect the exposed pad to $-V_S$.

TYPICAL PERFORMANCE CHARACTERISTICS

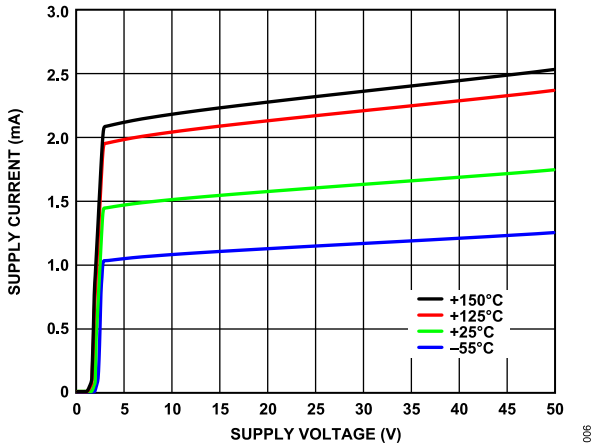


Figure 7. Supply Current vs. Supply Voltage

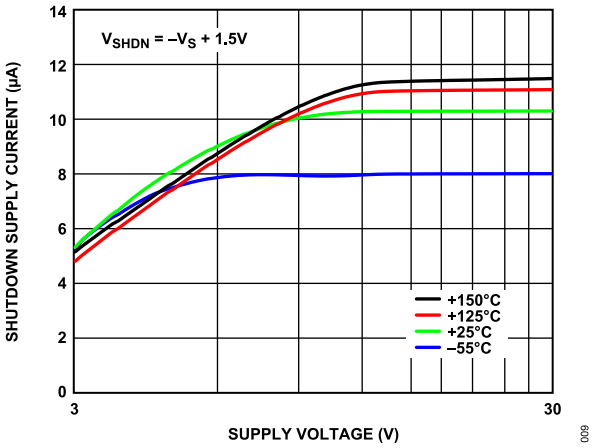


Figure 10. Shutdown Supply Current vs. Supply Voltage

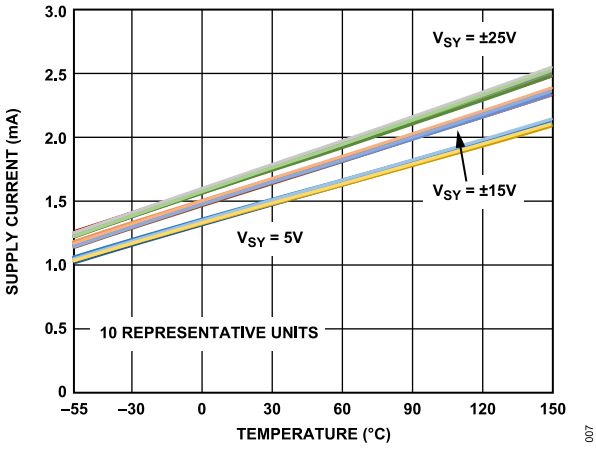


Figure 8. Supply Current vs. Temperature Across Various Supply Voltages

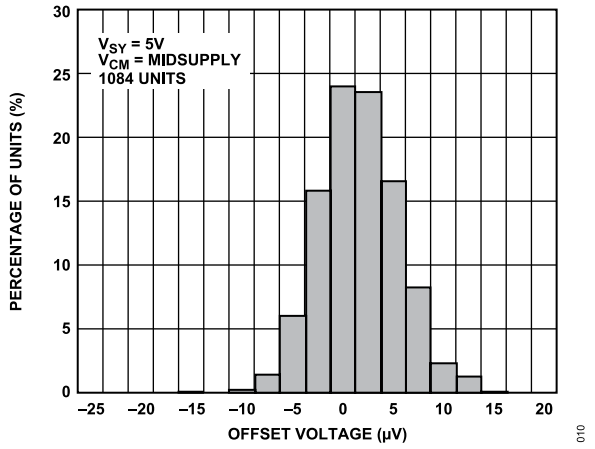


Figure 11. Typical Distribution of Input Offset Voltage, V_{SY} = 5 V

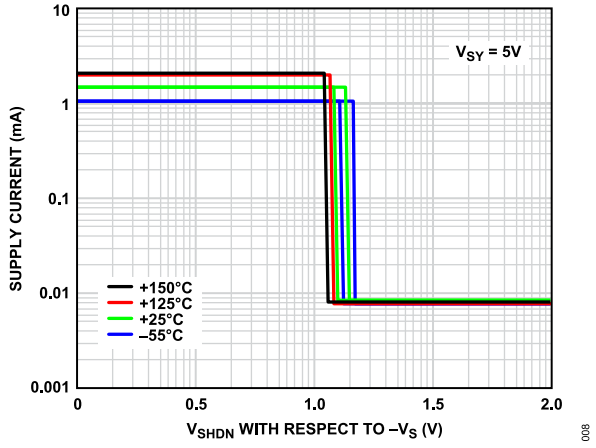


Figure 9. Supply Current vs. V_{SHDN} with Respect to $-V_S$

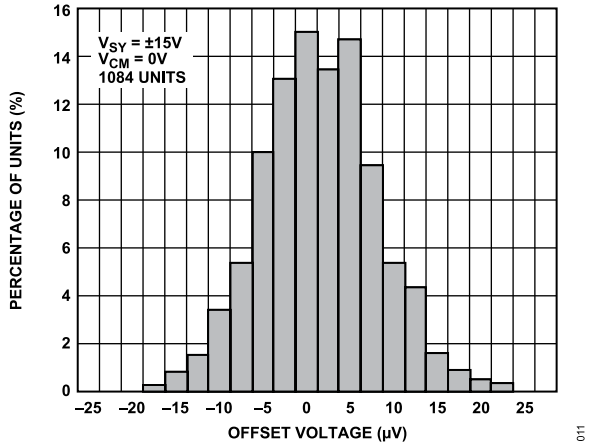


Figure 12. Typical Distribution of Input Offset Voltage with V_{SY} = ±15 V

TYPICAL PERFORMANCE CHARACTERISTICS

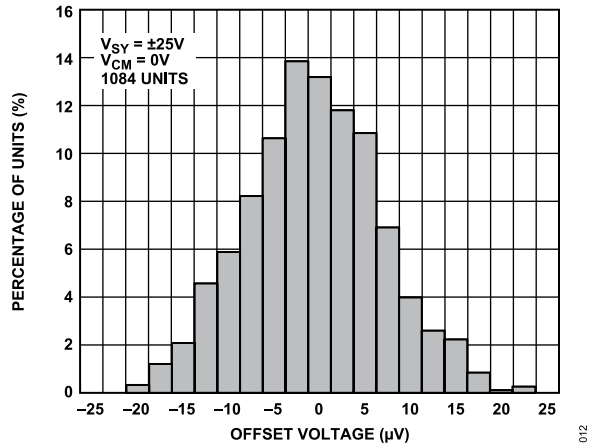


Figure 13. Typical Distribution of Input Offset Voltage with V_{SY} = ±25 V

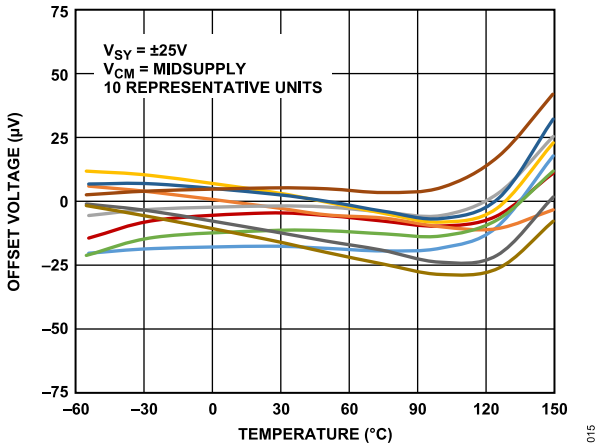


Figure 16. Offset Voltage vs. Temperature with V_{SY} = ±25 V

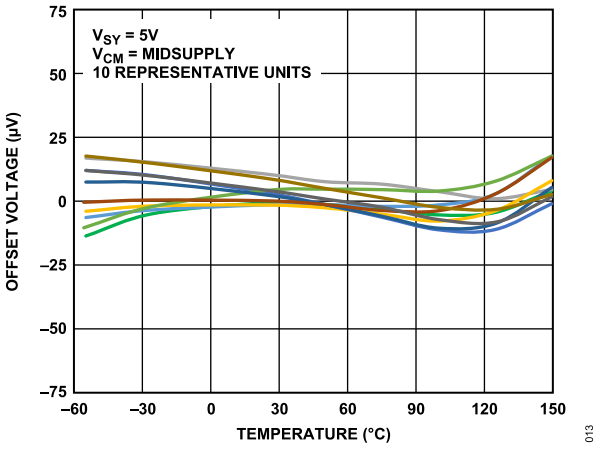


Figure 14. Offset Voltage vs. Temperature with V_{SY} = 5 V

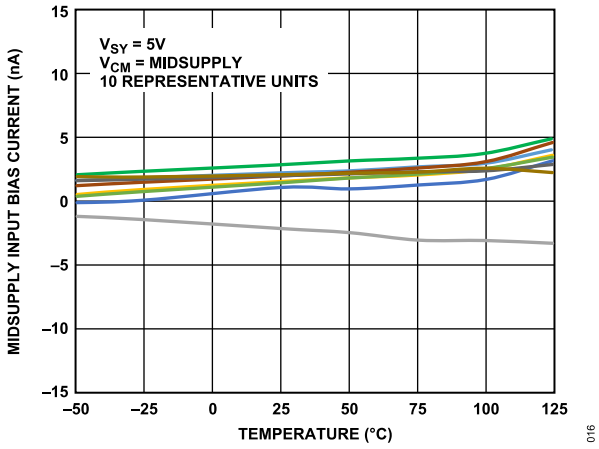


Figure 17. Midsupply Input Bias Current vs. Temperature with V_{SY} = 5 V

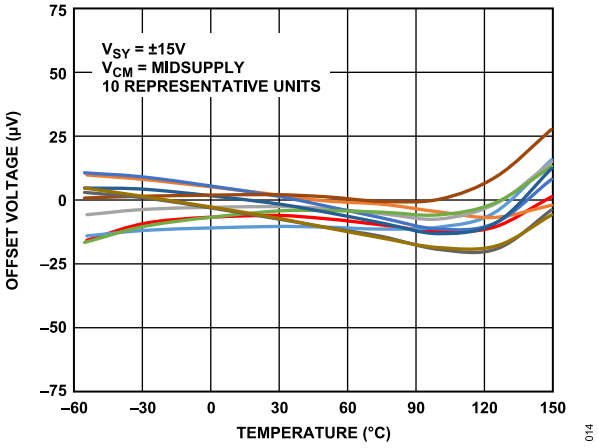


Figure 15. Offset Voltage vs. Temperature with V_{SY} = ±15 V

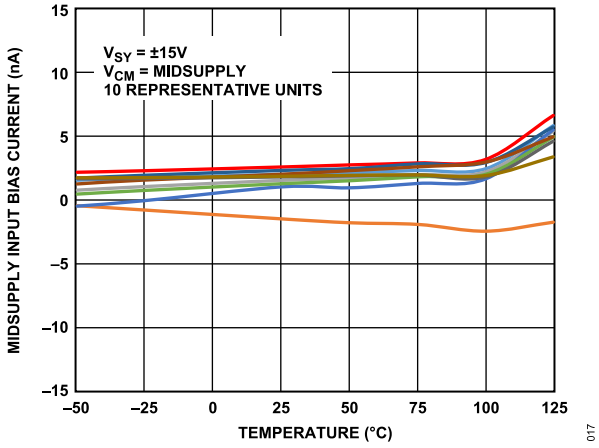


Figure 18. Midsupply Input Bias Current vs. Temperature with V_{SY} = ±15 V

TYPICAL PERFORMANCE CHARACTERISTICS

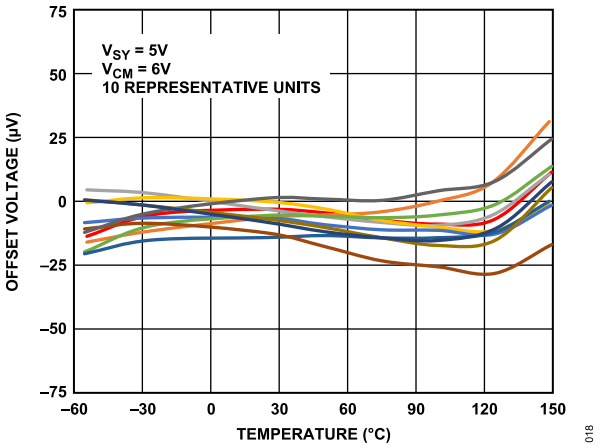


Figure 19. Offset Voltage vs. Temperature with V_{CM} = 6 V, Over-The-Top

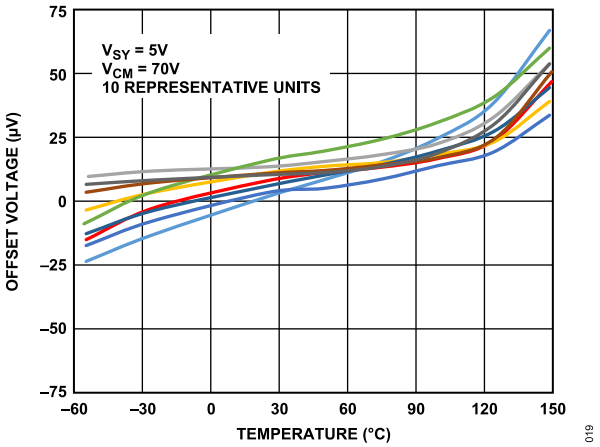


Figure 20. Offset Voltage vs. Temperature with V_{CM} = 70 V

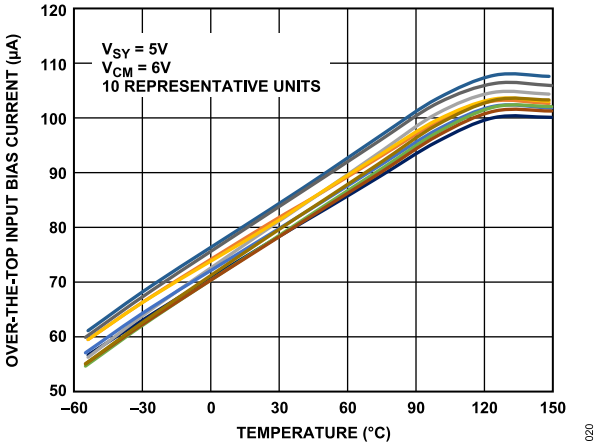


Figure 21. Over-The-Top Input Bias Current vs. Temperature with V_{CM} = 6 V

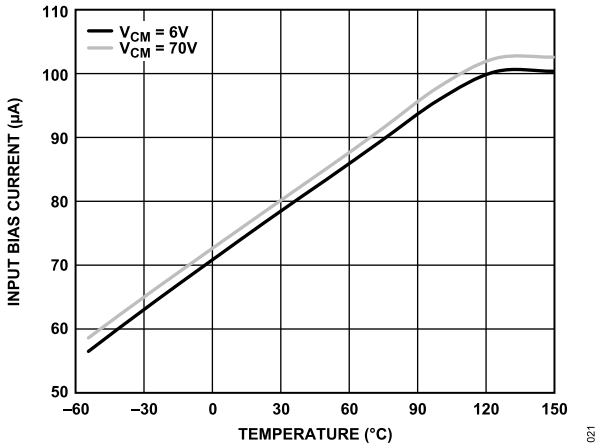


Figure 22. Input Bias Current vs. Temperature with V_{SY} = 5 V, Over-The-Top

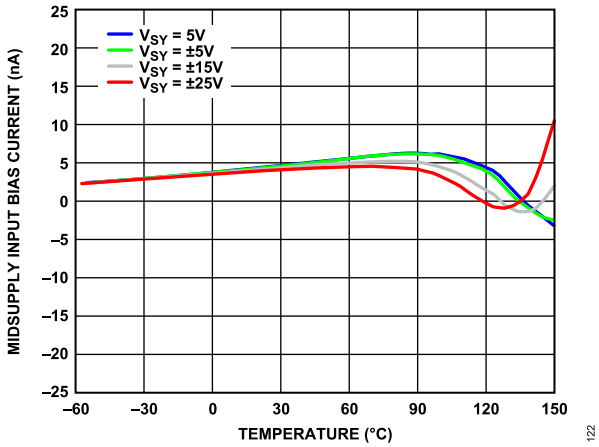


Figure 23. Midsupply Input Bias Current vs. Temperature Across Various Supply Voltages

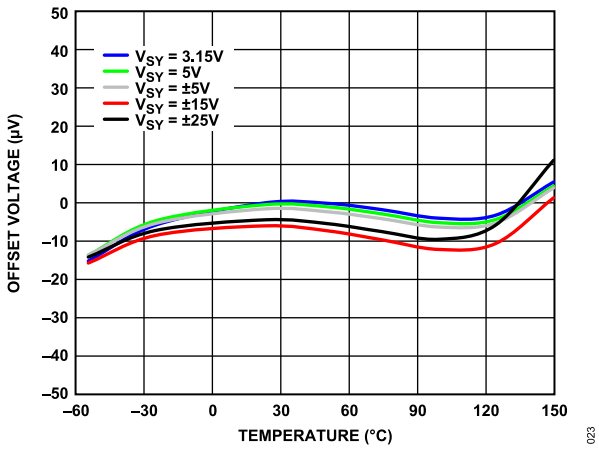


Figure 24. Offset Voltage vs. Temperature Across Various Supply Voltages

TYPICAL PERFORMANCE CHARACTERISTICS

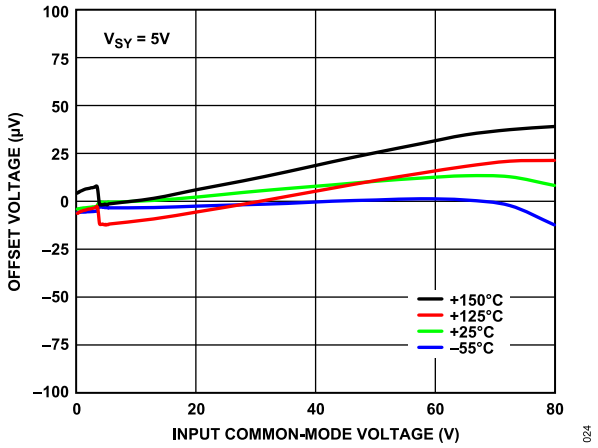


Figure 25. Offset Voltage vs. Input Common-Mode Voltage over the Input Common-Mode Range

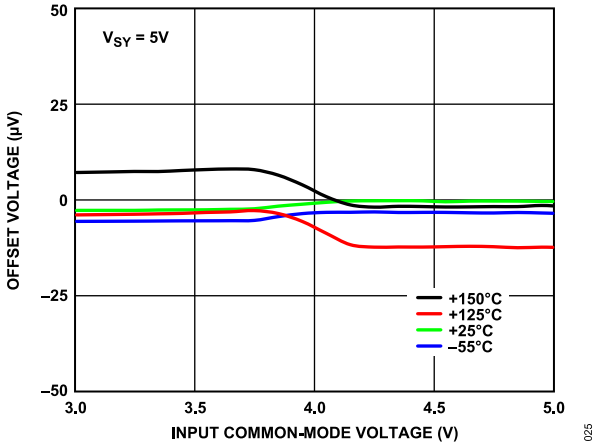


Figure 26. Offset Voltage vs. Input Common-Mode Voltage from Normal Operation to Over-The-Top Operation

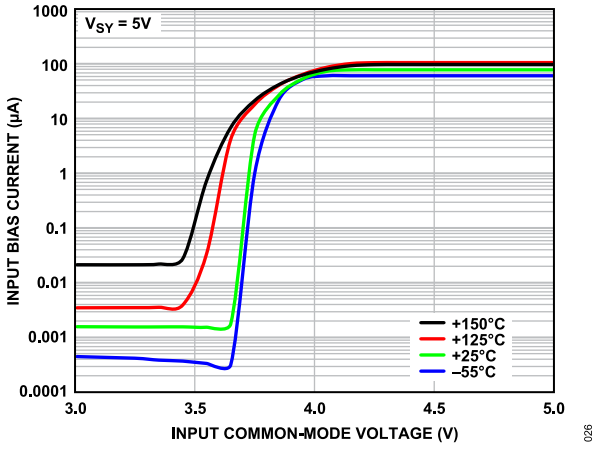


Figure 27. Input Bias Current vs. Input Common-Mode Voltage from Normal Operation to Over-The-Top Operation

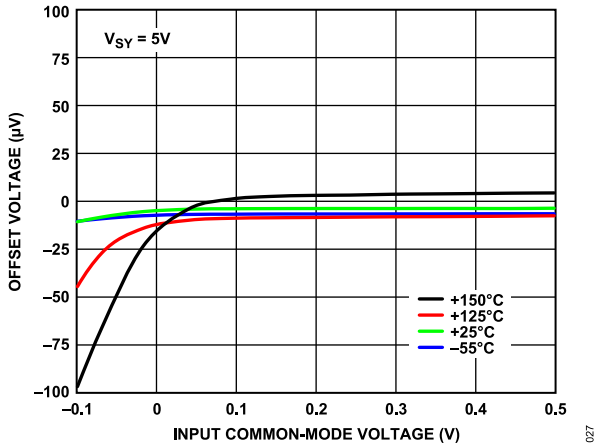


Figure 28. Offset Voltage vs. Input Common-Mode Voltage for Ground Sensing Applications

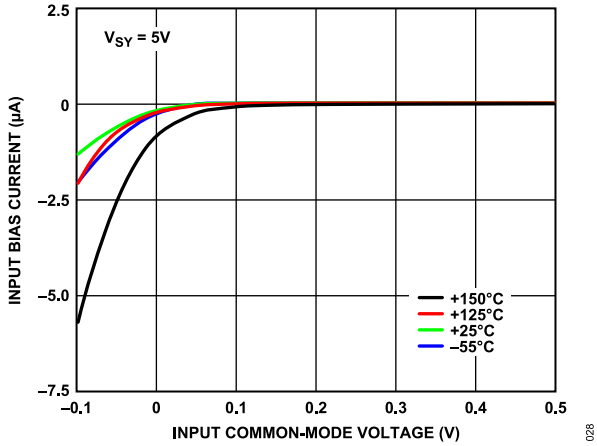


Figure 29. Input Bias Current vs. Input Common-Mode Voltage for Ground Sensing Applications

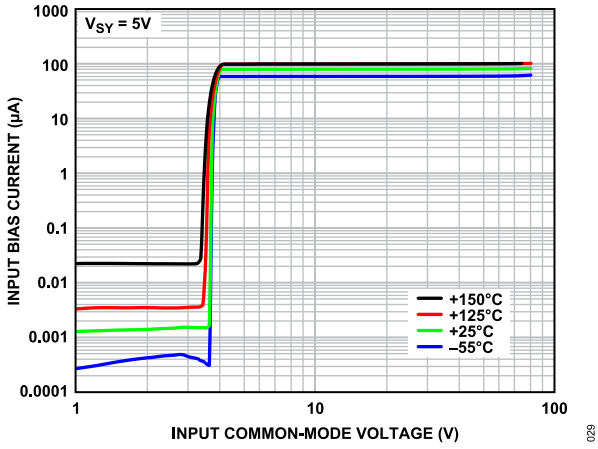


Figure 30. Input Bias Current vs. Input Common-Mode Voltage

TYPICAL PERFORMANCE CHARACTERISTICS

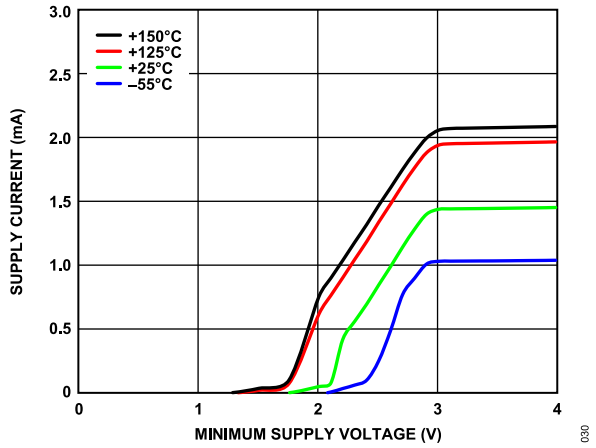


Figure 31. Supply Current vs. Minimum Supply Voltage

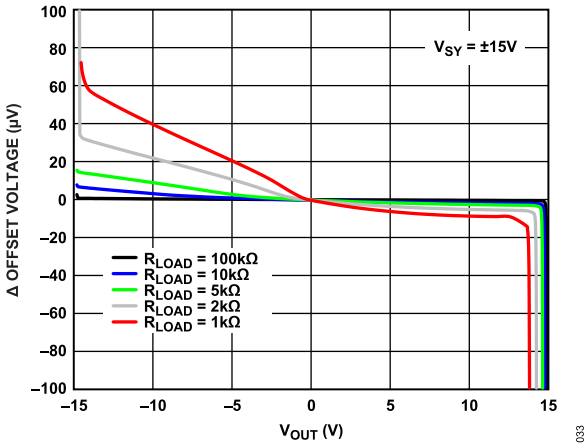


Figure 34. Δ Offset Voltage vs. Output Voltage (V_{OUT})

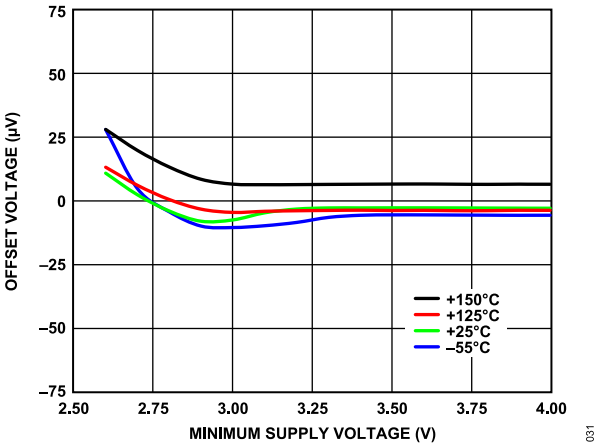


Figure 32. Offset Voltage vs. Minimum Supply Voltage

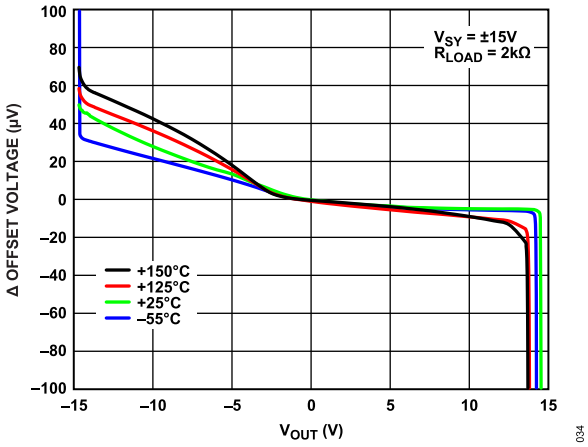


Figure 35. Δ Offset Voltage vs. V_{OUT} (2 kΩ Load)

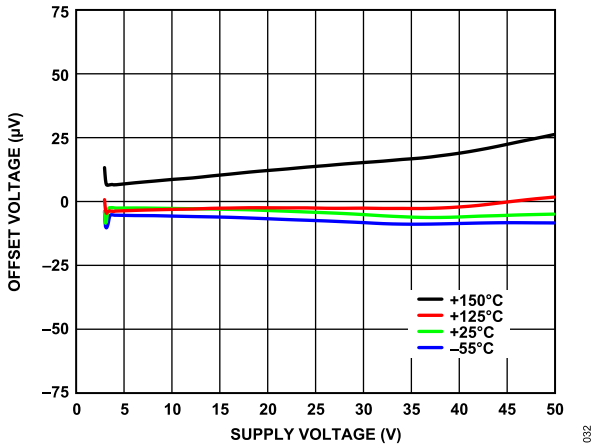


Figure 33. Offset Voltage vs. Supply Voltage

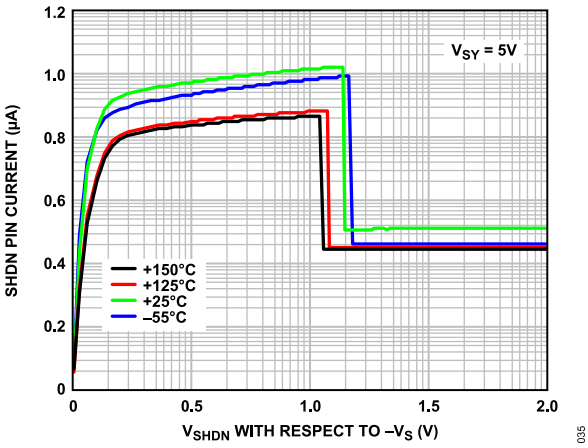


Figure 36. SHDN Pin Current vs. V_{SHDN} with Respect to $-V_S$ over Various Temperatures

TYPICAL PERFORMANCE CHARACTERISTICS

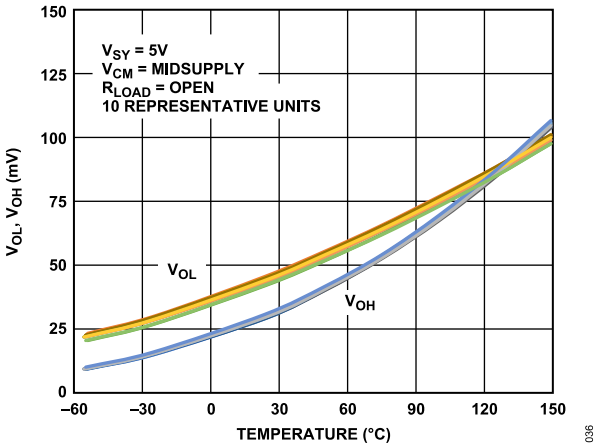


Figure 37. Output Voltage Low (V_{OL}) and Output Voltage High (V_{OH}) vs. Temperature

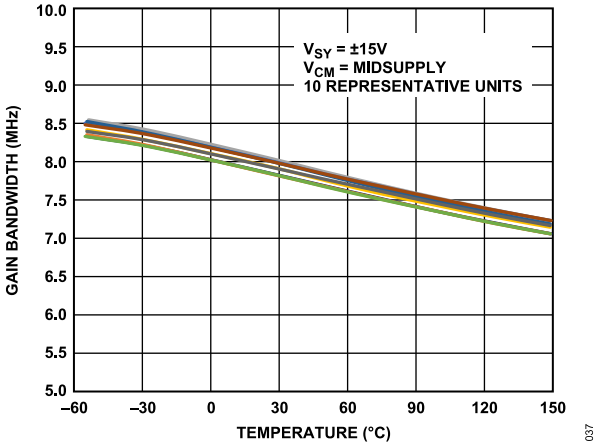


Figure 38. Gain Bandwidth vs. Temperature

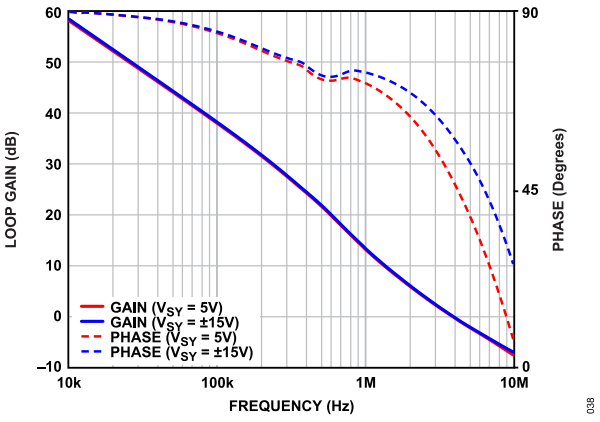


Figure 39. Loop Gain and Phase vs. Frequency

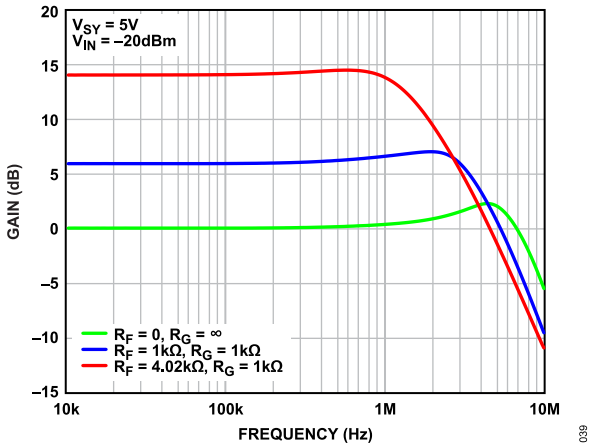


Figure 40. Noninverting Small Signal Frequency Response

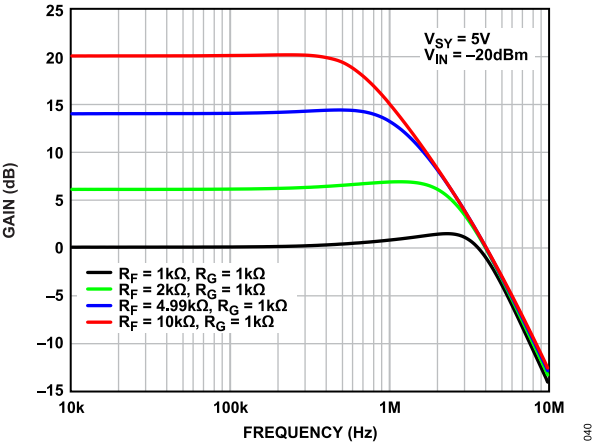


Figure 41. Inverting Small Signal Frequency Response

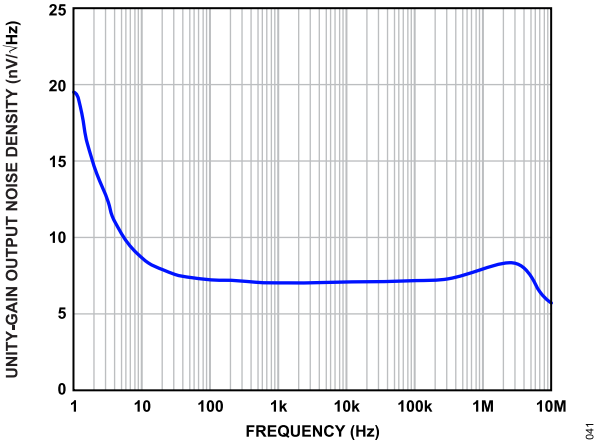


Figure 42. Unity-Gain Output Noise Density vs. Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

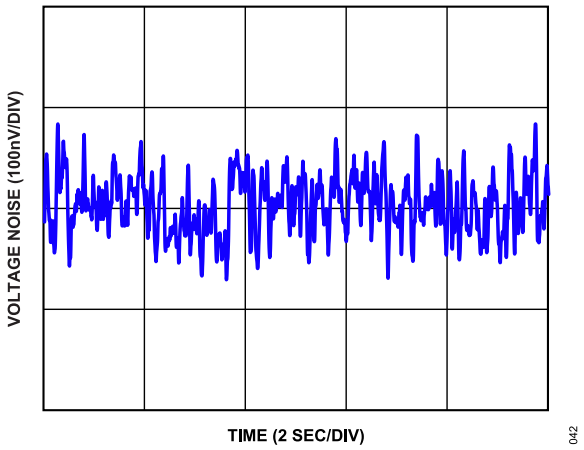


Figure 43. 0.1 Hz to 10 Hz Noise

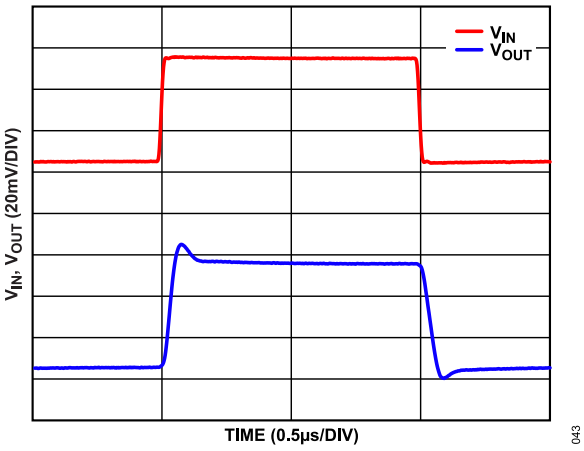


Figure 44. Unity-Gain Small Signal Step Response

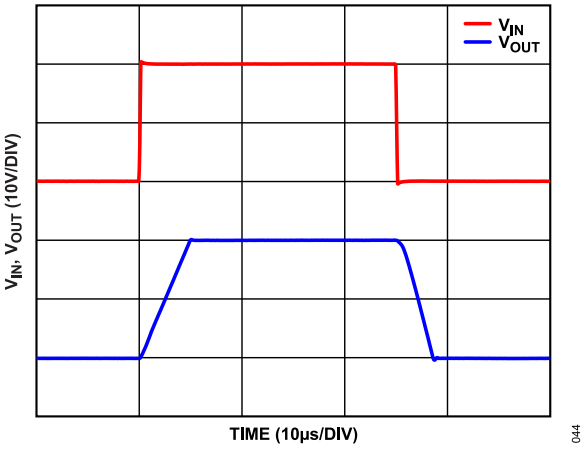


Figure 45. Unity-Gain Large Signal Step Response

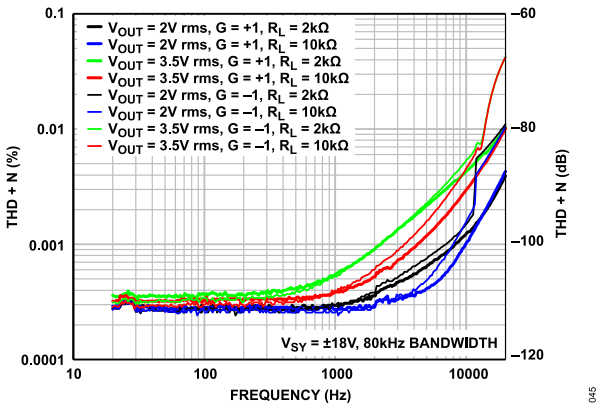


Figure 46. THD + N vs. Frequency over Load

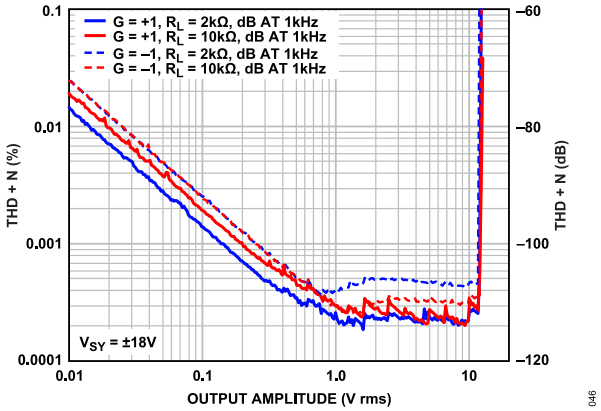


Figure 47. THD + N vs. Output Amplitude

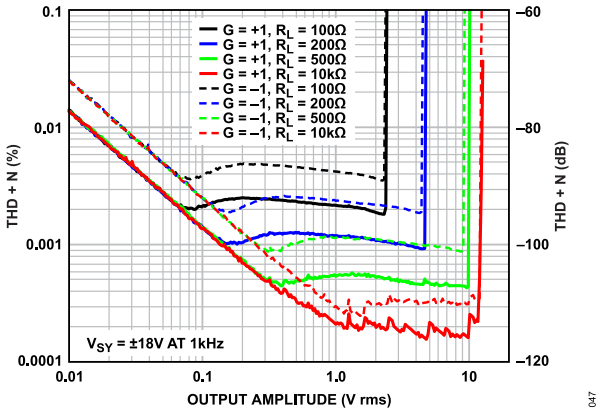


Figure 48. THD + N vs. Output Amplitude and Load

TYPICAL PERFORMANCE CHARACTERISTICS

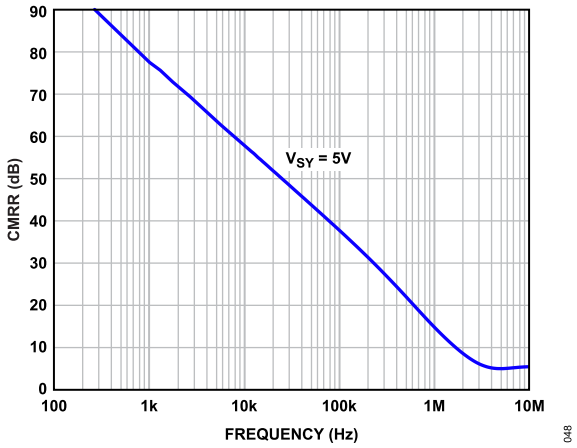


Figure 49. CMRR vs. Frequency

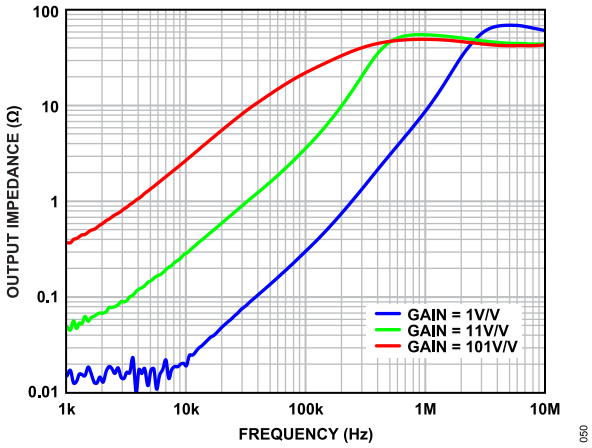


Figure 51. Output Impedance vs. Frequency

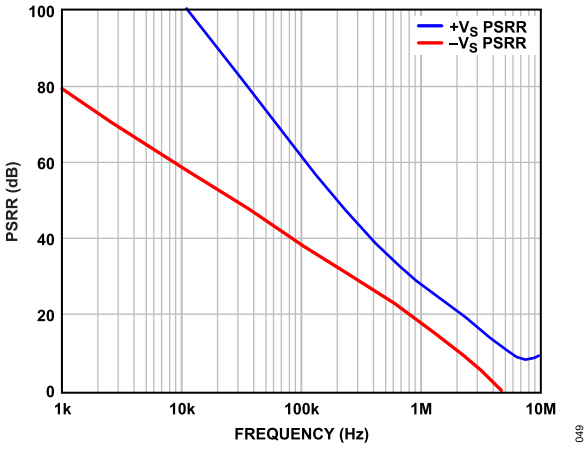


Figure 50. PSRR vs. Frequency

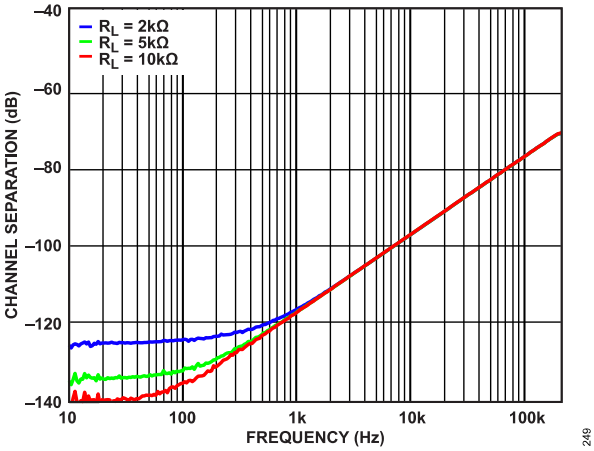


Figure 52. Channel Separation vs. Frequency

THEORY OF OPERATION

The ADA4099-1 and ADA4099-2 are single/dual robust, voltage feedback amplifiers that combine unity-gain stability with low offset, low offset drift, and 7 nV/√Hz of input noise. Figure 55 shows a simplified schematic of the device. The ADA4099-1 and ADA4099-2 have two input stages: a common emitter differential input stage consisting of the Q1 and Q2 PNP transistors that operate with the inputs biased between $-V_S$ and 1.5 V below $+V_S$, and a common base input stage that consists of the Q3 to Q6 PNP transistors that operate when the common-mode input is biased $>+V_S - 1.5$ V. These input stages result in two distinct operating regions, as shown in Figure 53.

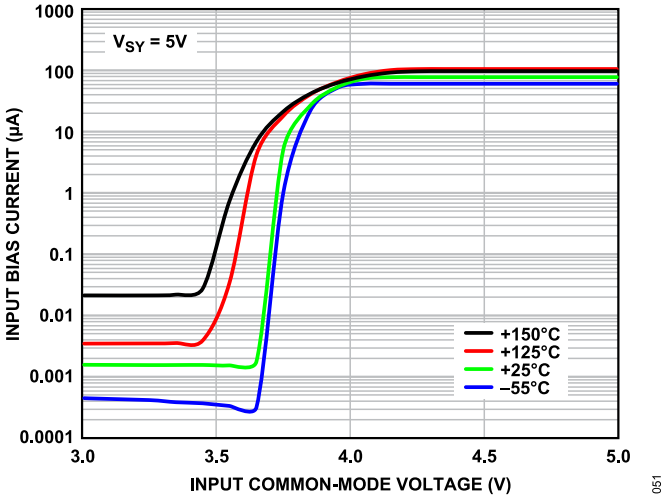


Figure 53. Input Bias Current vs. Input Common-Mode Voltage over Temperature, V_{SY} = 5 V

For common-mode input voltages that are approximately 1.5 V below the $+V_S$ supply, where Q1 and Q2 are active (see Figure 53), the common emitter PNP input stage is active and the input bias current is typically <4 nA. When the common-mode input is above $+V_S - 1.5$ V, the Q9 transistor turns on, which diverts bias current away from the common emitter differential input pair to the mirror that consists of M3 and M4. The current from M4 biases the common base differential input pair (Q3 to Q6). The Over-The-Top input pair operates in a common base configuration and the input bias current increases to ~82.5 µA. The offset voltages of both input stages are tightly trimmed and are specified in Table 1 and Table 2.

As the input common-mode transitions to the Over-The-Top region, the input CMRR degrades slightly when compared to the rest of the input common-mode range, as shown in Figure 54.

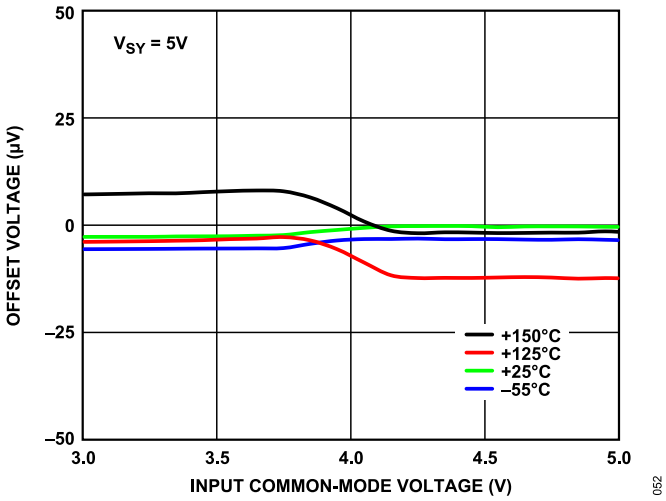


Figure 54. Offset Voltage vs. Input Common-Mode Voltage over Temperature, V_{SY} = 5 V

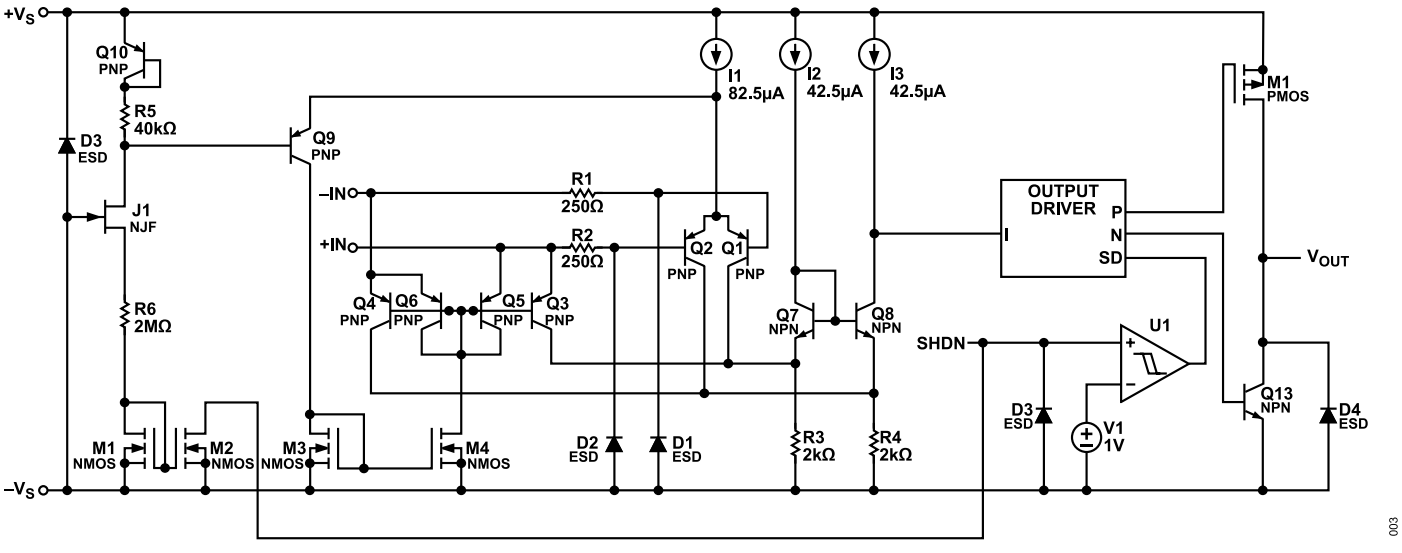


Figure 55. Simplified ADA4099-1 and ADA4099-2 Schematic

THEORY OF OPERATION

INPUT PROTECTION

The inputs are protected against temporary voltage excursions to 10 V below $-V_S$ (see Figure 56) by an internal 250 Ω resistor (see Figure 55). This resistor limits the current in the series D1 diode and D2 diode that are tied to the bases of the Q1 and Q2 transistors, respectively. Adding additional external series resistance extends the protection to >10 V below $-V_S$, at the cost of stability and added thermal noise. The input stage of the ADA4099-1 and ADA4099-2 incorporates phase reversal protection to prevent the output from phase reversing for inputs below $-V_S$. The ADA4099-1 and ADA4099-2 op amps do not have clamping diodes between the inputs and can be differentially overdriven up to 80 V without damage, inducing parametric shifts, or drawing appreciable input current. Figure 57 summarizes the input fault types that can be applied to the ADA4099-1 and ADA4099-2 without compromising input integrity.

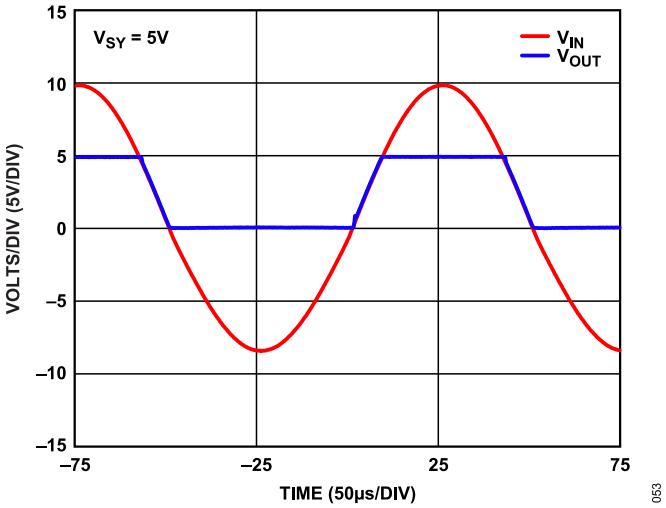


Figure 56. ADA4099-1 and ADA4099-2 as Unity-Gain Buffers with Noninverting Inputs Driven Beyond the Supply (V_{SY} = 5 V)

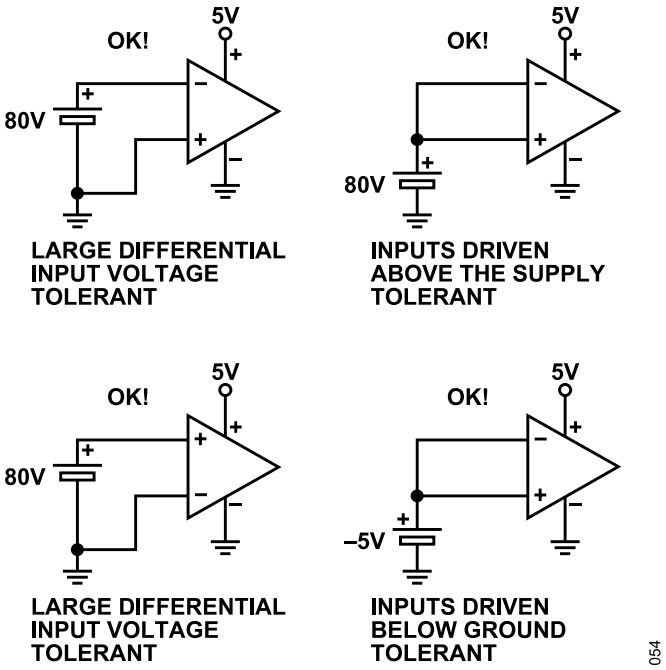


Figure 57. ADA4099-1 and ADA4099-2 Fault Tolerant Conditions

OVER-THE-TOP OPERATION CONSIDERATIONS

When the ADA4099-1 and ADA4099-2 input common-modes are biased near or >+V_S supply, the amplifiers operate in the Over-The-Top configuration. The differential input pair that controls amplifier operation is the common base pair, Q3 to Q6 (see Figure 55).

Input bias currents change from <±4 nA in normal operation to approximately 82.5 µA in Over-The-Top operation when the input stage transitions from common emitter to common base. The Over-The-Top input bias currents are well matched, and the associated offset is typically <250 nA. Ensure that the impedance connected to the inverting and noninverting inputs is well matched to avoid any input bias current induced voltage offsets.

Differential input impedance, R_{IN} (see Figure 58), decreases from >100 kΩ in normal operation to ~600 Ω in Over-The-Top operation (see Table 1 and Table 2).

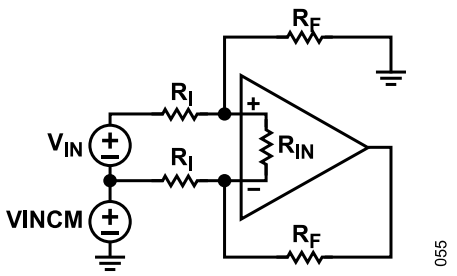


Figure 58. Difference Amplifier Configured for Normal Operation and Over-The-Top Operation

THEORY OF OPERATION

This R_{IN} resistance appears across the summing nodes in Over-The-Top operation due to the configuration of the common base input stage.

The R_{IN} value is derived from the specified I_B that flows to the op amp inputs, as expressed in the following equation:

$$R_{IN} = 2kT/(qI_B)$$

where:
k is Boltzmann's constant.
T is the operating temperature.
q is the charge of an electron.
I_B is the operating input bias current in Over-The-Top operation.

The inputs are biased proportional to absolute temperature. Therefore, R_{IN} is relatively constant with temperature. This resistance appears across the summing nodes of the amplifiers, which is forced to 0 V differentially by the feedback action of the amplifiers and can seem relatively harmless. However, depending on the configuration, this input resistance can boost the noise gain, lower overall amplifier loop gain and closed-loop bandwidth, and raise output noise. The singular benefit of this configuration is an increase in closed-loop amplifier stability.

In normal mode ($-V_S < V_{CM} < +V_S - 1.5$ V), R_{IN} is typically large compared to the value of the gain setting resistors (R_F and R_I), and R_{IN} can be ignored.

In this case, the noise gain is defined by the following equation:

$$Noise\ Gain = 1 + R_F/R_I$$

When the amplifiers transition to Over-The-Top operation with the input common-mode biased near or above the $+V_S$ supply, consider the value of R_{IN}.

The noise gain of the amplifiers increases as shown in the following equation:

$$Noise\ Gain_{OTT} = \left(\left(1 + \frac{R_F}{R_I||R_{IN} + R_I||R_F}\right) \times \left(1 + \frac{R_I||R_F}{R_{IN}}\right)\right)$$

where $Noise\ Gain_{OTT}$ is the Over-The-Top noise gain.

The dc closed-loop gain remains mostly unaffected (R_F/R_I). However, the loop gain of the amplifiers decreases, as expressed in the following equation:

$$\frac{A_{OL}}{1 + \frac{R_F}{R_I}} \text{ to } \frac{A_{OL}}{Noise\ Gain_{OTT}}$$

Likewise, the closed-loop bandwidth (BW_{CLOSED_LOOP}) of the amplifiers changes, going from normal operation to Over-The-Top operation.

In normal operation,

$$BW_{CLOSED\_LOOP} \approx \frac{GBP}{1 + \frac{R_F}{R_I}}$$

In Over-The-Top operation,

$$BW_{CLOSED\_LOOP} \approx \frac{GBP}{Noise\ Gain_{OTT}}$$

Output voltage noise density (e_{no}) is impacted when the device transitions from normal operation to Over-The-Top operation. Resistor noise is neglected in both modes of operation in the following equations:

In normal operation, neglecting resistor noise,

$$e_{no} \cong e_n\left(1 + \frac{R_F}{R_I}\right)$$

where e_n is input referred voltage noise density.

In Over-The-Top operation, neglecting resistor noise,

$$e_{no} \cong e_n \times Noise\ Gain_{OTT}$$

OUTPUT

The output of the ADA4099-1 and ADA4099-2 can swing rail-to-rail to within 45 mV of either supply with no load. The output can source and sink ~30 mA. The amplifiers are internally compensated to drive at least 100 pF of load capacitance (C_L). Adding a series resistance of 50 Ω between the output and larger capacitive loads extends the capacitive drive capability of the amplifiers.

If the ADA4099-1 and ADA4099-2 enter shutdown, the V_{OUT} pin appears as high impedance with two steering diodes connected to either supply. In this state, the output typically leaks <5 nA.

SHUTDOWN PINS

The ADA4099-1 and ADA4099-2 have dedicated shutdown pins (SHDN for the ADA4099-1, and SHDN1 and SHDN2 for the ADA4099-2 10-lead LFCSP) to place the amplifiers in a very low power shutdown state when asserted high. A logic high is defined by a voltage ≥1.5 V applied to SHDN and SHDNx with respect to the $-V_S$ pin. In shutdown, the amplifiers draw <15 µA of supply current (see Figure 59) and the V_{OUT} pin is placed in a high impedance state.

THEORY OF OPERATION

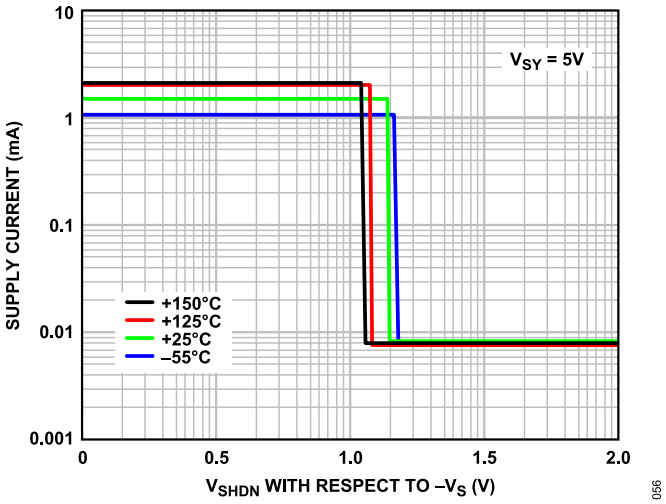


Figure 59. Supply Current vs. V_{SHDN} with Respect to $-V_S$

SHDN or SHDNx can be driven beyond the $+V_S$ supply up to the absolute maximum voltage (60 V with respect to $-V_S$) and draws little current (<1.5 µA). For normal active amplifier operation, SHDN or SHDNx can be floated or driven by an external voltage source low (within 0.5 V of $-V_S$). If SHDN or SHDNx are left floating, an internal current source (~600 nA) pulls SHDN or SHDNx to $-V_S$, which places the amplifiers into a default, active amplifying state. Because of the close proximity of the −IN pin (ADA4099-1) or −INx pins (ADA4099-2 10-lead LFCSP) and SHDN or SHDNx, fast edges on the −IN pin or −INx pins may ac-couple to the adjacent high impedance SHDN or SHDNx, inadvertently placing the devices in shutdown. If this scenario is a concern, add a 1 nF capacitor between SHDN or SHDNx and the $-V_S$ pin.

Alternatively, the amplifiers can be effectively placed in a low power state by removing $+V_S$. In this low power state, the inputs typically leak <1 nA with either ±IN pin or either ±INx biased between $-V_S$ and 70 V above $-V_S$. If the ±IN pins or ±INx pins are taken below $-V_S$, they appear as a diode connected to the $-V_S$ supply in series with a resistance of 250 Ω. In this condition, limit the current to <30 mA.

Using an external source to drive the output beyond either $\pm V_S$ supply under shutdown conditions may produce unlimited current and may damage the device.

APPLICATIONS INFORMATION

LARGE RESISTOR GAIN OPERATION

The ADA4099-1 and ADA4099-2 have approximately 12 pF of input capacitance.

The parallel combination of the feedback resistor (R_F) and gain setting resistor (R_G) on the inverting input can combine with this input capacitance (C_{IN}) to form a pole that can reduce bandwidth, cause frequency response peaking, or produce oscillations (see Figure 61). To mitigate these consequences, place a feedback capacitor with a value of $C_F > C_{IN}(R_G/R_F)$ in parallel with R_F for summing node impedances >1 kΩ ($R_F||R_G$>1 kΩ). This capacitor placement cancels the input pole and optimizes dynamic performance (see Figure 60).

For applications where the noise gain is unity ($R_G \rightarrow \infty$), and the feedback resistor exceeds 1 kΩ, $C_F \geq C_{IN}$. Optimize PCB layouts to keep layout related summing node capacitance to an absolute minimum.

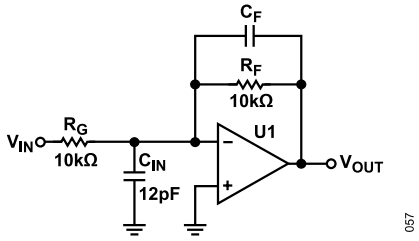


Figure 60. Inverting Gain Schematic

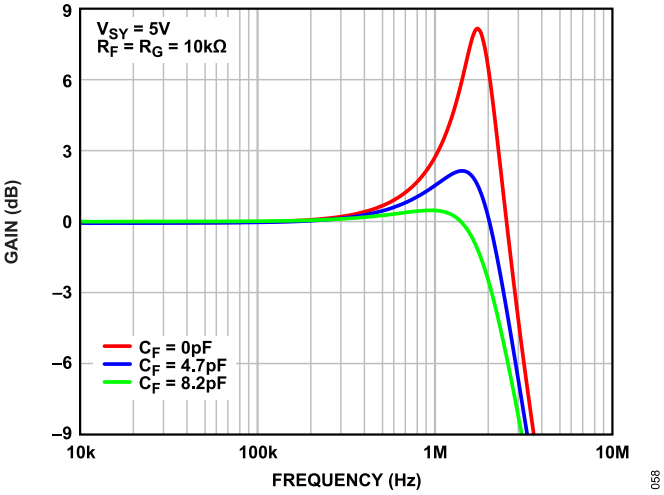


Figure 61. Inverting Gain of 1, Small Signal Frequency Response, $R_F = R_G$ = 10 kΩ

RECOMMENDED VALUES FOR VARIOUS GAINS

Table 9 is a reference for determining various recommended gains and associated noise performance. The total impedance seen at the inverting input is kept to <1 kΩ for gains >1 to maintain ideal small signal bandwidth.

Table 9. Gains and Associated Recommended Resistor Values (T_A = 25°C)

Gain	R_G (kΩ)	R_F (kΩ)	C_F (pF)	Approximate −3 dB Frequency (MHz)	Total System Noise (nV/√Hz at 1 kHz), Referred to Input
+1	Not applicable	0	Not applicable	8	6.8
+2	1	1	0	4	7.2
+2	10	10	8.2	2.7	11
+5	1	4.02	0	1.5	7.4
−1	10	10	8.2	2.1	22
−1	1	1	0	4.8	14.4
−2	1	2	0	2.9	11.3
−5	1	4.99	0	1.4	9.2
−10	1	10	0	0.75	8.7

APPLICATIONS INFORMATION

NOISE

To analyze the noise performance of an amplifier circuit, identify the noise sources, and then determine if each source has a significant contribution to the overall noise performance of the amplifiers. To simplify the noise calculations, noise spectral densities (NSDs) are used rather than actual voltages, to leave bandwidth out of the expressions. NSD is generally expressed in nV/√Hz and is equivalent to the noise in a 1 Hz bandwidth.

The noise model shown in Figure 62 has six individual noise sources: the Johnson noise of the three resistors (R1 to R3), the op amp voltage noise, and the current noise ($I_{N\pm}$) in each input of the amplifiers. Each noise source has its own contribution to the noise at the output. Noise is generally specified as referring to input (RTI), but it is often simpler to calculate the noise referred to the output (RTO), and then divide by the noise gain to obtain the RTI noise.

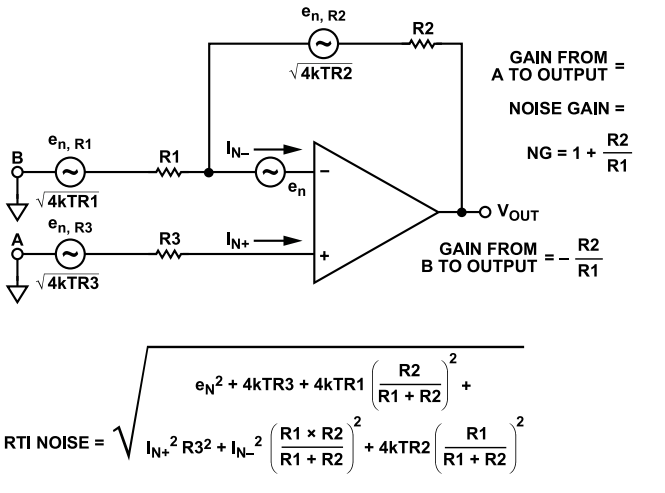


Figure 62. Op Amp Noise Analysis Model

Assuming $I_{N+} = I_{N-} = I_N$, the equation for RTI noise can be simplified to the following form:

$$RTI\ Noise = \sqrt{e_n^2 + e_{n,R}^2 + \left(I_N R_{EQ}\right)^2}$$

$$e_{n,R} = \sqrt{4kTR_{EQ}}$$

$$R_{EQ} = R_3 + R_1 || R_2$$

where:
e_n is the op amp voltage noise.
$e_{n,R}$ is the thermal noise contribution of the surrounding R1 to R3 resistors.
R_{EQ} is the equivalent input resistance.
T is the absolute temperature in Kelvin.

A 50 Ω resistor generates a Johnson noise of 1 nV/√Hz at 25°C.

For optimal performance, the lower bound of resistance in a feedback network is determined by the amount of quiescent power and distortion that can be tolerated. The upper bound is determined by the resistor and current noise density. The ADA4099-1 and ADA4099-2 have an e_n of 7 nV/√Hz.

If resistor and current noise contributions are less than half this value, the e_n introduced by the op amps dominates and provides optimal noise performance of the devices.

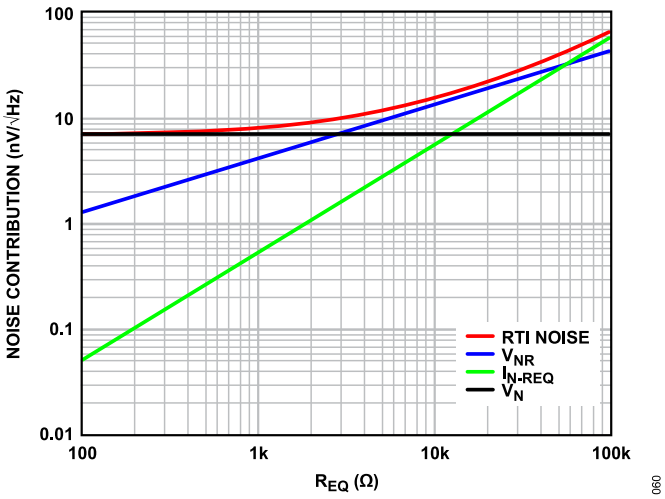


Figure 63. Noise Contributions vs. Equivalent Input Resistance (R_{EQ})

For the ADA4099-1 and ADA4099-2, this lower bound of resistance in the feedback network is about 750 Ω. For the amplifier configuration shown in Figure 62, R_{EQ} < 750 Ω provides stable noise performance. If noise performance is not important, e_n is typically fixed for a given T_A, $e_{n,R}$ increases with the square root of the resistor value, and the $I_N \times R_{EQ}$ resistance increases linearly, but does not impact total noise until it approaches the value of $e_{n,R}$. With R_{EQ} < ~60 kΩ, $e_{n,R}$ is larger than $I_N \times R_{EQ}$. A safe value for R_{EQ} is ~30 kΩ to ensure that I_N is not the majority contributor to total noise seen by the input.

Figure 63 shows the noise contributions for the range of resistance values discussed in this section.

DISTORTION

There are two main contributors of distortion in op amps: output crossover distortion as the output transitions from sourcing to sinking, and distortion caused by nonlinear common-mode rejection. If the op amps are operating in an inverting configuration, there is no common-mode induced distortion. If the op amps are operating in the noninverting configurations within the normal input common-mode range ($-V_S$ to $+V_S$ − 1.5 V), distortion is acceptable. When the inputs transition from normal to Over-The-Top operation or vice versa, a significant degradation occurs in linearity due to the change of input circuitry.

As R_L decreases, distortion increases due to a net decrease in loop gain and greater signal swings internal to the amplifiers that are necessary to drive the load. The lowest distortion can be achieved with the ADA4099-1 and ADA4099-2 operating in Class A operation

APPLICATIONS INFORMATION

in an inverting configuration, with the input common-mode biased at midsupply.

POWER DISSIPATION AND THERMAL SHUTDOWN

The ADA4099-1 and ADA4099-2 can drive heavy loads on power supplies up to ±25 V. Therefore, ensure that T_J on the integrated circuit does not exceed 175°C.

Junction temperatures exceeding 125°C promote accelerated aging. Reliability of the ADA4099-1 and ADA4099-2 may be impaired if the junction temperature exceeds 175°C. If the junction temperature exceeds 175°C, the ADA4099-1 and ADA4099-2 have a final safety measure in the form of a thermal shutdown that shuts off the output stage and reduces the internal device currents. When this thermal shutdown function triggers, the output remains disabled in a high impedance state until the junction temperature drops 20°C. Persistent heavy loads and elevated ambient temperatures can cause the ADA4099-1 and ADA4099-2 to oscillate in and out of thermal shutdown depending on the power dissipated on the die, until the heavy load is removed (see Figure 64).

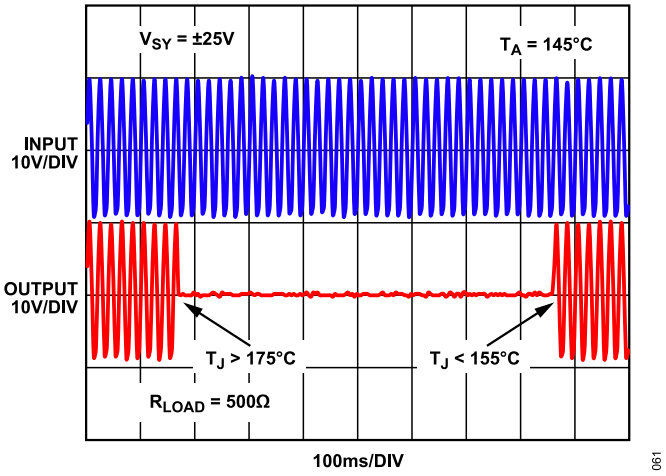


Figure 64. ADA4099-1 and ADA4099-2 Cycling In and Out of Thermal Shutdown

It is not recommended to operate near the maximum junction temperature.

Typically, T_J can be estimated from T_A and the device power dissipation ($P_D \times \theta_{JA}$), as shown in the following equation:

$$T_J = T_A + P_D \times \theta_{JA}$$

The power dissipation in the IC varies as a function of supply voltage, the output voltage, and load resistance. For a given supply voltage, the worst case power dissipation ($P_{D(MAX)}$) in the IC occurs when the supply current is maximum, and the output voltage is at half of either supply voltage.

$$P_{D(MAX)} = V_s I_{s(MAX)} + \frac{\left(\frac{V_{SY}}{2}\right)^2}{R_L}$$

For a given supply voltage, use Figure 65 as a guide for estimating the minimum load resistance that the ADA4099-1 and ADA4099-2 can drive for a given supply voltage and a given rise in junction temperature (ΔT_J). For example, to limit ΔT_J to 50°C, the load driven on the ±15 V supplies (+30 V total supply) must not be lower than 1.2 kΩ. It is assumed that θ_{JA} is 192°C/W.

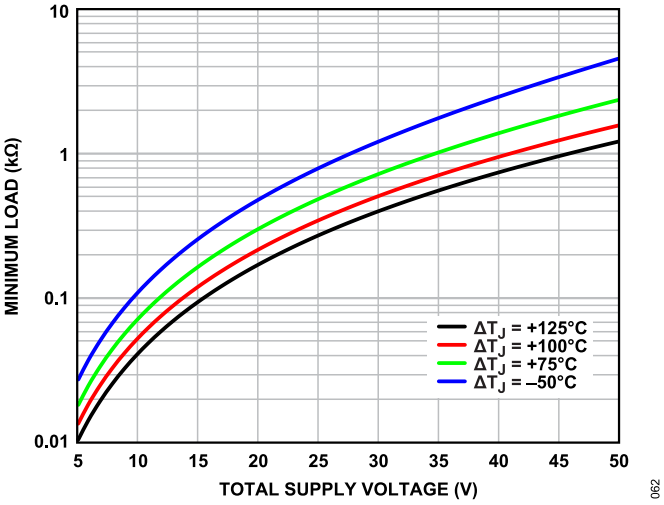


Figure 65. Minimum Load Resistance for Given ΔT_J and V_{SY}

CIRCUIT LAYOUT CONSIDERATIONS

Careful and deliberate attention to detail when laying out the ADA4099-1 and ADA4099-2 boards yields optimal performance. Power supply bypassing, parasitic capacitance, and component selection all contribute to the overall performance of the amplifiers.

POWER SUPPLY BYPASSING

On single supplies, solder the $-V_S$ supply pin directly to a low impedance ground plane. Bypass the $+V_S$ pin to a low impedance ground plane with a low effective series resistance (ESR) multilayer ceramic capacitor (MLCC) of 0.1 µF, typically, as close to the $\pm V_S$ supply pins as possible. When driving heavy loads, add 10 µF of supply capacitance. When using split supplies, these conditions are applicable to the $-V_S$ supply pin.

The ADA4099-1 and ADA4099-2 have an internal current source of ~0.6 µA on the SHDN (ADA4099-1) and SHDNx (ADA4099-2 10-lead LFCSP) pins to pull the pins down to $-V_S$ and place the amplifiers in the default amplifying state. If the shutdown state is not required, hard tie SHDN or SHDNx to the $-V_S$ pin. If SHDN or SHDNx is left floating or driven by a source with significant source impedance (>100 Ω), bypass the $-V_S$ supply pin with a small, 1 nF capacitor to prevent stray signals from coupling on SHDN or SHDNx, which can inadvertently trigger shutdown.

GROUNDING

Use ground and power planes where possible to reduce the resistance and inductance of the supply and ground returns. Place bypass capacitors as close as possible to the $\pm V_S$ supply pins, with

APPLICATIONS INFORMATION

the other ends connected to the ground plane. It is recommended to use a bypass capacitor of at least 0.1 µF when driving light loads (load currents < 100 µA), and more capacitance when driving heavier loads. Routing from the output to the load and return to the ground plane must have minimal loop area to keep inductance to a minimum.

ESD PROTECTION WHEN POWERED

ICs react to ESD strikes differently when unpowered vs. powered, which falls under IEC-61000-4-2 standards (see the Absolute Maximum Ratings section). A device that performs well under HBM conditions can perform poorly under International Electrotechnical Commission (IEC) conditions. The ADA4099-1 and ADA4099-2 are thoroughly abused with ESD strikes under IEC conditions to create a front-end circuit protection scheme that protects the devices if subjected to ESD strikes. Figure 66 and Figure 67 show two different protection schemes that extend the protection of the ADA4099-1 and ADA4099-2 to ±8 kV ESD strikes.

Consider the following when selecting components:

- A component size of 0805 or larger to reduce chance of arc-over.
- Pulse withstanding, thick film resistors.
- C0G MLCC with a minimum rating of 100 V.
- Bidirectional, transient voltage suppression (TVS) diodes.

In the circuit shown in Figure 66, R1 is a 220 Ω, Panasonic, 0805, ERJ-P6 series, and C1 is a 100 pF, Yageo, 0805, 100 V, C0G/NPO.

ADVANTAGES	DISADVANTAGES
INEXPENSIVE (~5 CENTS)	R1 INTRODUCES THERMAL NOISE
SMALL FOOTPRINT	RC NETWORK LIMITS SPEED
MINIMAL LEAKAGE	NEED TO CAREFULLY CHARACTERIZE CAPACITOR
	NOT AS ROBUST AGAINST REPEATED STRIKES

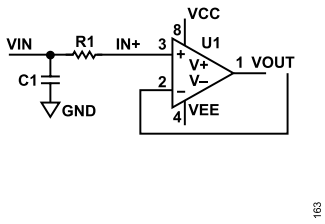


Figure 66. ESD Protection Circuit (RC Network)

In the circuit shown in Figure 67, R1 is a 220 Ω, Panasonic, 0805, ERJ-P6 series, and D1 is a Bourns CDSOD323-T36SC. An ESD varistor can be considered for D1.

For more information on system level ESD considerations, see the technical article, *When Good Electrons Go Bad: How to Protect Your Analog Front End*, on the Analog Devices, Inc., website.

RELATED PRODUCTS

Table 10 describes several alternative precision amplifiers that can also be considered for certain applications.

ADVANTAGES	DISADVANTAGES
INEXPENSIVE (20 TO 30 CENTS)	R1 INTRODUCES NOISE
SMALL FOOTPRINT	D1 HAS LEAKAGE CURRENT
VERY ROBUST	D1 HAS CAPACITANCE (5pF TO 300pF)

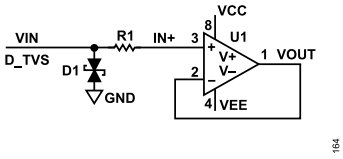


Figure 67. ESD Protection Circuit (R-TVS Network)

Table 10. ADA4099-1 and ADA4099-2 Related Products

Model	V_{OS} (µV)	I_B (nA)	GBP (kHz)	e_n (nV/√Hz)	I_{SY} (µA)	Input Common-Mode Range (V)
ADA4099-1	25	10	8000	7	1500	$-V_S$ to $-V_S$ + 70
ADA4099-2	25	10	8000	7	1500	$-V_S$ to $-V_S$ + 70
ADA4077-1	35	1	3900	7	500	$-V_S$ to $+V_S$
LT6015	50	5	3200	18	335	$-V_S$ to $-V_S$ + 76
LT6014	60	0.4	1600	9.5	165	$-V_S$ to $+V_S$
LT1494	375	1	2.7	185	1.5	$-V_S$ to $-V_S$ + 36
LT1490A	500	8	180	50	55	$-V_S$ to $-V_S$ + 44

APPLICATIONS INFORMATION

TYPICAL APPLICATIONS

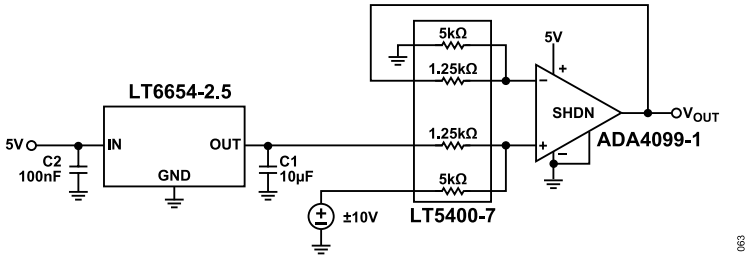


Figure 68. ±10 V to 0 V to +5 V Funnel Amplifier, High CMRR and ±80 V Input Protection via LT5400-7 Resistor Network (ADA4099-1 6-lead TSOT)

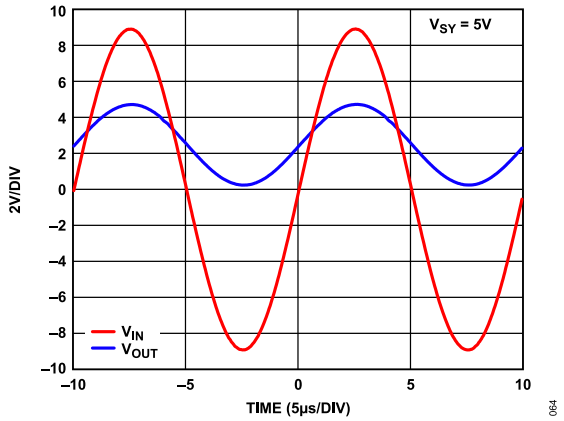


Figure 69. ±10 V to 0 V to +5 V Funnel Amplifier, Input and Output Voltages

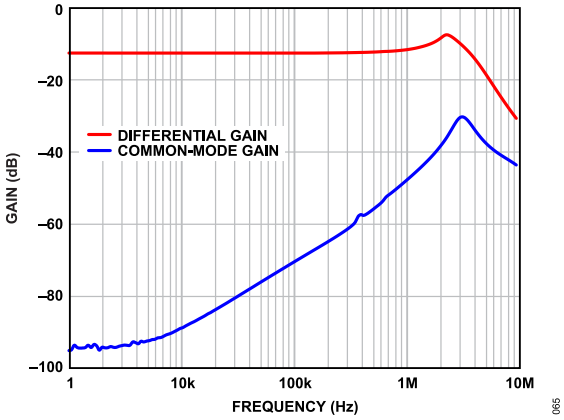


Figure 70. ±10 V to 0 V to +5 V Funnel Amplifier, System Gain

APPLICATIONS INFORMATION

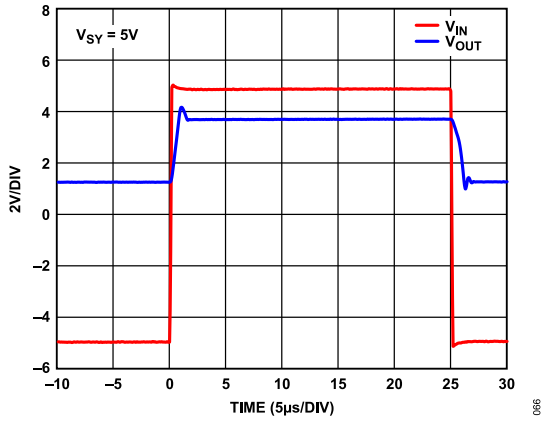


Figure 71. ±10 V to 0 V to +5 V Funnel Amplifier, Large Signal Pulse Response

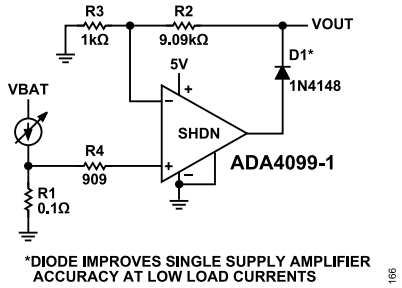


Figure 72. 1 V/A Low-Side Current Sense (ADA4099-1 6-lead TSOT)

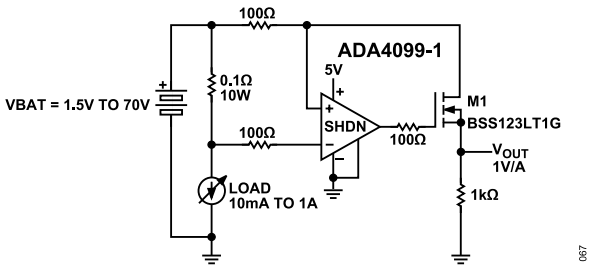


Figure 73. 1 V/A High-Side Current Sense (ADA4099-1 6-lead TSOT)

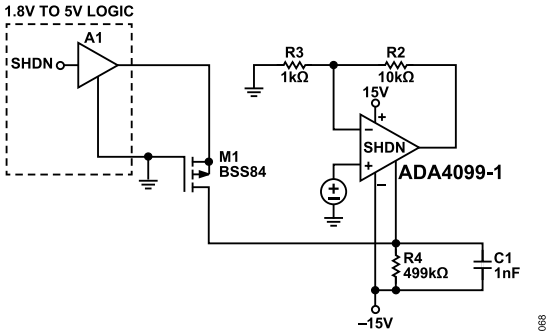
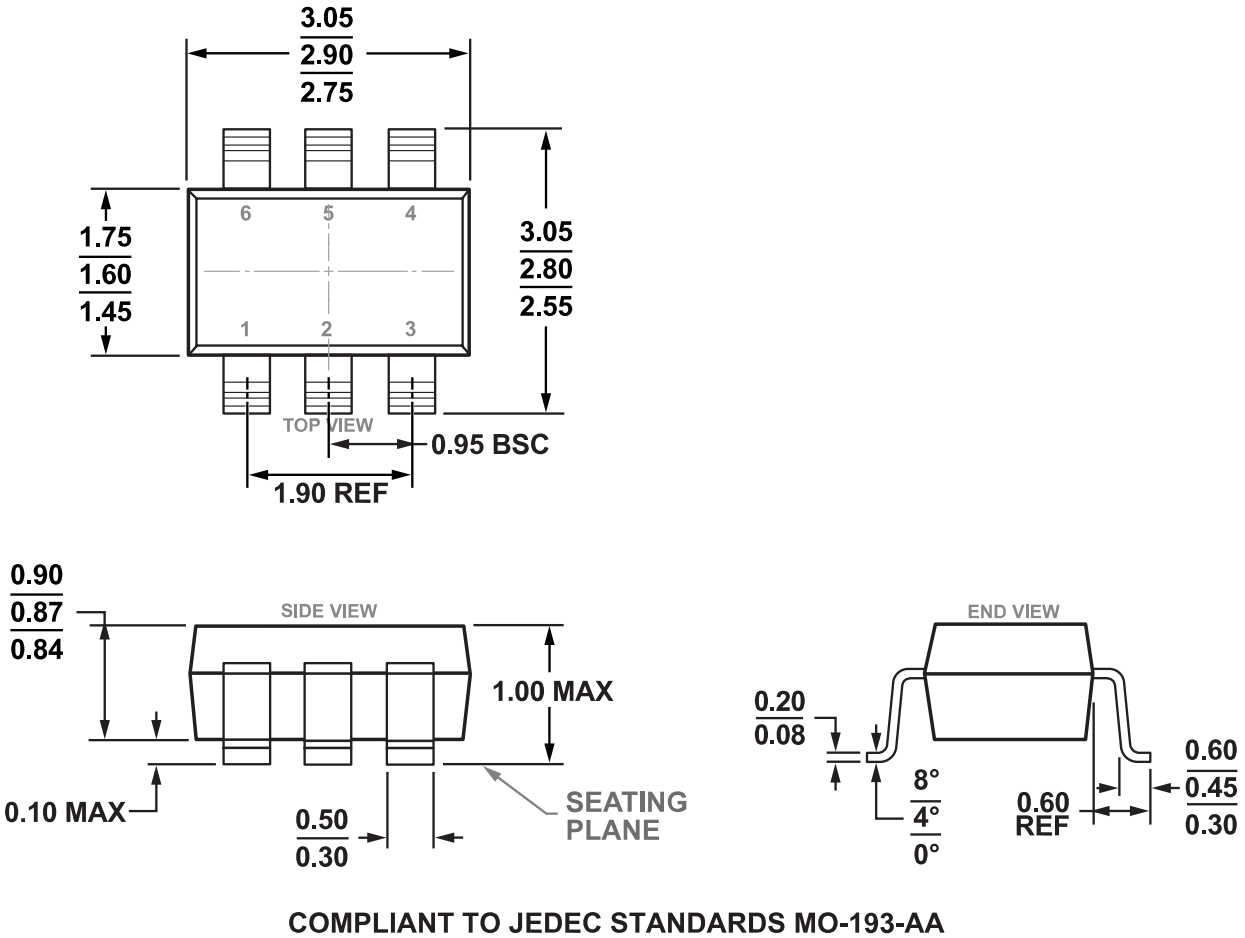


Figure 74. Microprocessor Control of SHDN Pin in Split Supply Applications (ADA4099-1 6-lead TSOT)

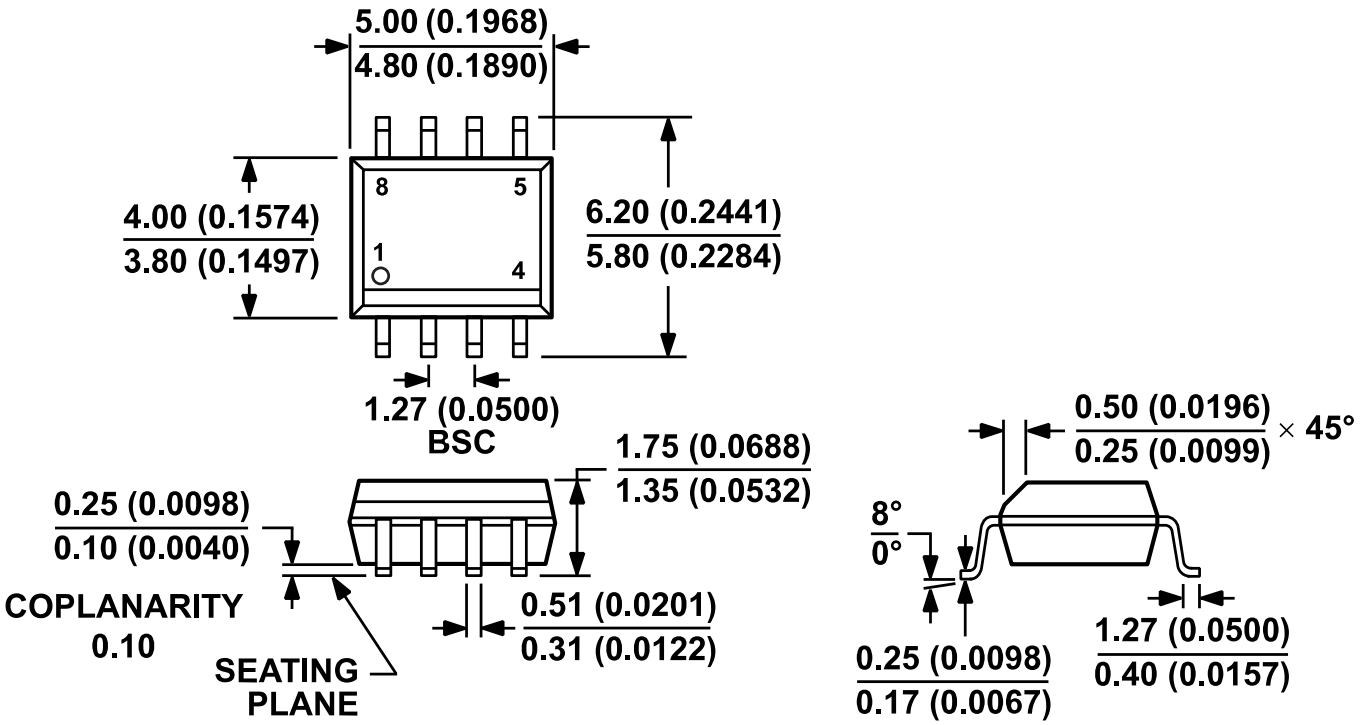
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-193-AA

Figure 75. 6-Lead Small Outline Transistor Package [TSOT]
(UJ-6)
Dimensions shown in millimeters

OUTLINE DIMENSIONS



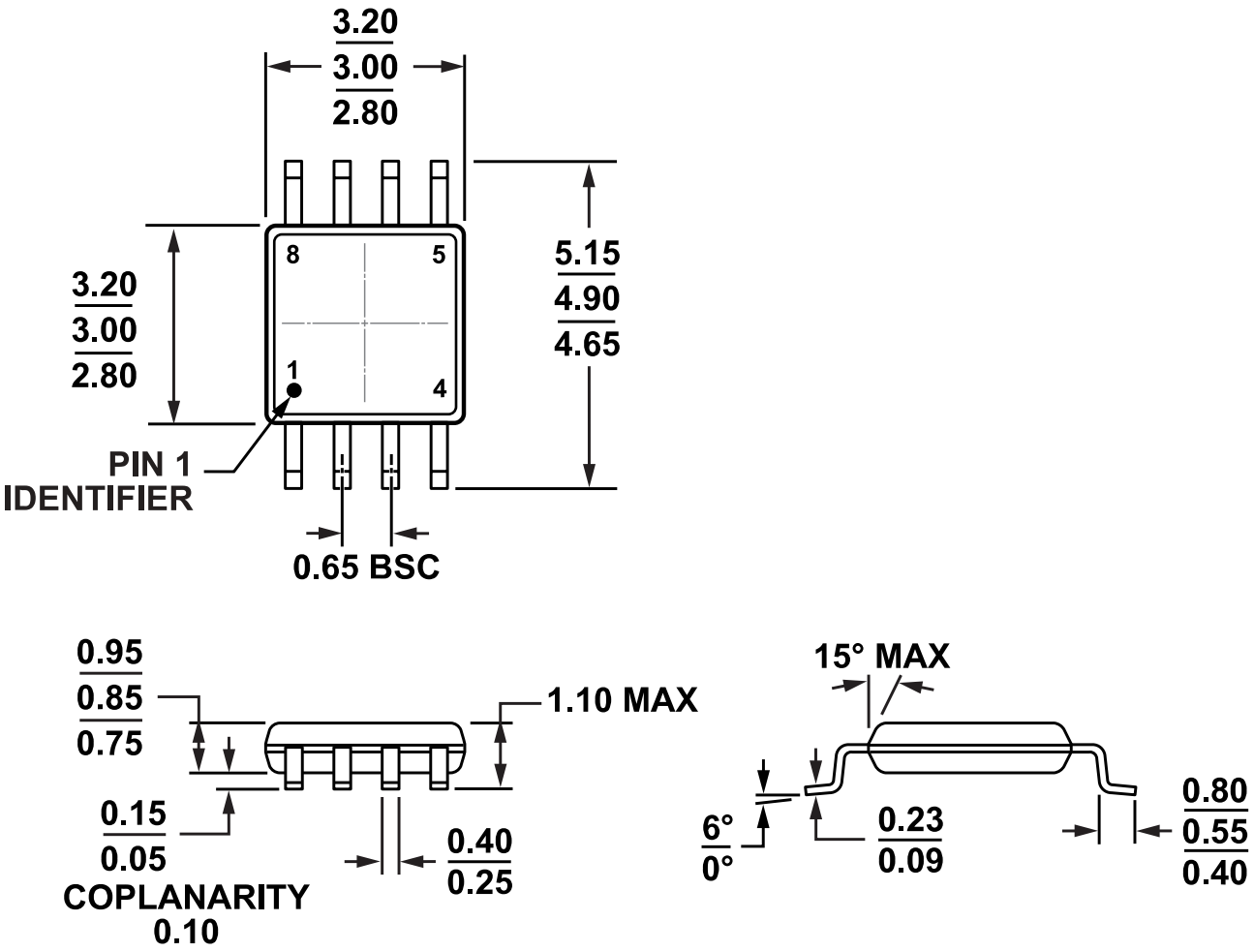
COMPLIANT TO JEDEC STANDARDS MS-012-AA

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

012407-A

Figure 76. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

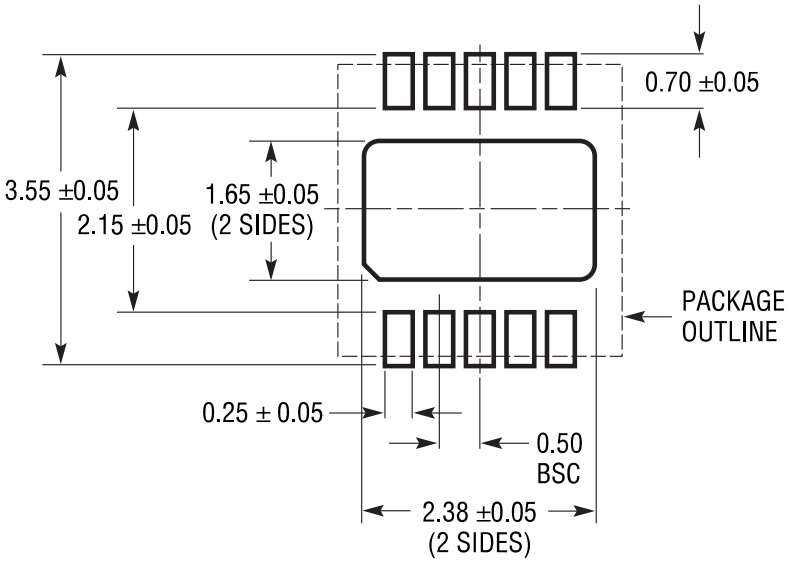
OUTLINE DIMENSIONS



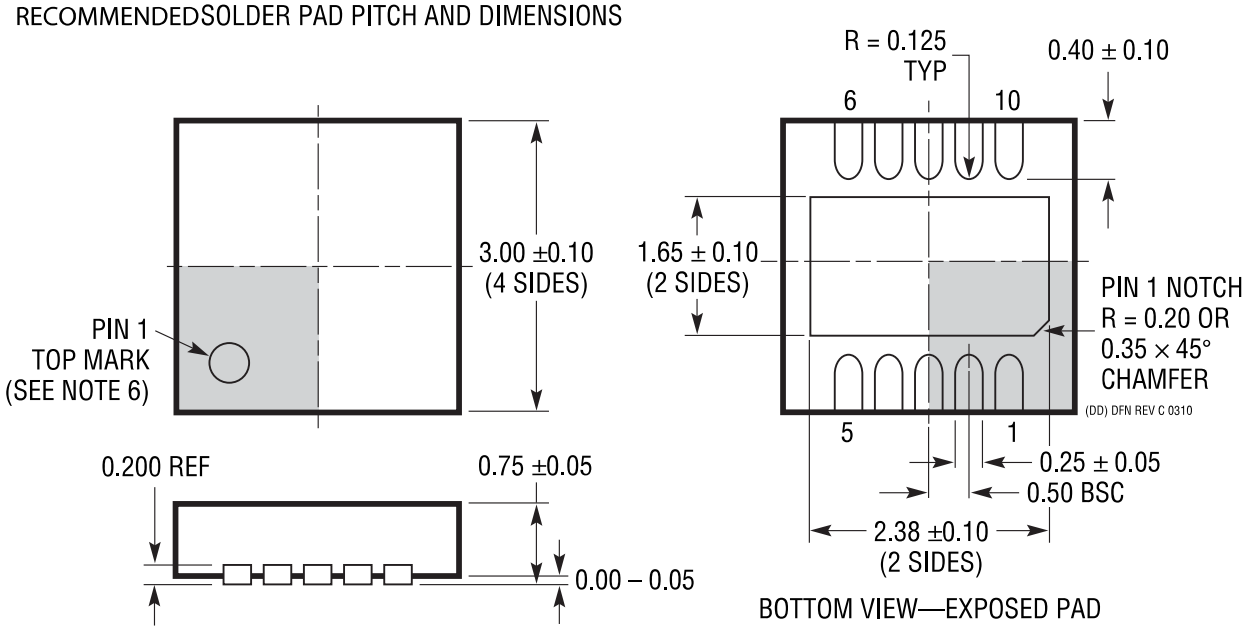
COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 77. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

OUTLINE DIMENSIONS



RECOMMENDEDSOLDER PAD PITCH AND DIMENSIONS



BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-2). CHECK THE LTC WEBSITE DATA SHEET FOR CURRENT STATUS OF VARIATION ASSIGNMENT
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

Figure 78. 10-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body and 0.75 mm Package Height
(05-08-1699)
Dimensions shown in millimeters

OUTLINE DIMENSIONS

Updated: January 07, 2022

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Marking Code
ADA4099-1BUJZ-R5	-40°C to +125°C	6-Lead TSOT	UJ-6	Y7P
ADA4099-1BUJZ-RL7	-40°C to +125°C	6-Lead TSOT	UJ-6	Y7P
ADA4099-1HUJZ-RL7	-55°C to +150°C	6-Lead TSOT	UJ-6	Y7Q
ADA4099-2BCPZ	-40°C to +125°C	10-Lead LFCSP (3mm x 3mm w/ EP)	05-08-1699	A44
ADA4099-2BCPZ-RL7	-40°C to +125°C	10-Lead LFCSP (3mm x 3mm w/ EP)	05-08-1699	A44
ADA4099-2BRMZ	-40°C to +125°C	8-Lead MSOP	RM-8	A44
ADA4099-2BRMZ-RL7	-40°C to +125°C	8-Lead MSOP	RM-8	A44
ADA4099-2BRZ	-40°C to +125°C	8-Lead SOIC_N	R-8	
ADA4099-2BRZ-RL7	-40°C to +125°C	8-Lead SOIC_N	R-8	
ADA4099-2HCPZ	-55°C to +150°C	10-Lead LFCSP (3mm x 3mm w/ EP)	05-08-1699	A45
ADA4099-2HCPZ-RL7	-55°C to +150°C	10-Lead LFCSP (3mm x 3mm w/ EP)	05-08-1699	A45
ADA4099-2HRZ	-55°C to +150°C	8-Lead SOIC_N	R-8	
ADA4099-2HRZ-RL7	-55°C to +150°C	8-Lead SOIC_N	R-8	

[1] Z = RoHS Compliant Part.

EVALUATION BOARDS

Model[1]	Description
EVAL-ADA4099-1HUJZ	Evaluation Board, Single TSOT
EVAL-ADA4099-2BCPZ	Evaluation Board, Dual LFCSP

[1] Z = RoHS Compliant Part.