55 V, EMI Enhanced, Zero Drift, Ultralow Noise, Rail-to-Rail Output Operational Amplifier

Known Good Die

ADA4522-2-KGD

FEATURES

- Low offset voltage: 5 µV maximum at 5.0 V and 30 V
- Extremely low offset voltage drift: 22 nV/°C maximum at 30 V
- Low voltage noise density: 5.8 nV/√Hz typical
- Low peak-to-peak voltage noise: 117 nV p-p from 0.1 Hz to 10 Hz typical
- Low input bias current: 50 pA typical
- Unity-gain crossover: 3 MHz
- Single-supply operation: input voltage range includes ground and rail-to-rail output
- Wide range of operating voltages
  - Single-supply operation: 4.5 V to 55 V
  - Dual-supply operation: ±2.25 V to ±27.5 V
- Integrated EMI filters
- Unity-gain stable

APPLICATIONS

- Inductance, capacitance, and resistance (LCR) meter/megohmmeter front-end amplifiers
- Load cell and bridge transducers
- Magnetic force balance scales
- High precision shunt current sensing
- Thermocouple/resistance temperature detector (RTD) sensors
- Programmable logic controller (PLC) input and output amplifiers

GENERAL DESCRIPTION

The ADA4522-2-KGD is a dual channel, zero drift op amp with low noise and power, ground sensing inputs, and rail-to-rail output, optimized for total accuracy over time, temperature, and voltage conditions. The wide operating voltage and temperature ranges, as well as the high open-loop gain and low dc and ac errors make the device well suited for amplifying small input signals and for accurately reproducing larger signals in a wide variety of applications.

The ADA4522-2-KGD performance is specified at 5.0 V, 30 V, and 55 V power supply voltages, and the device operates over the 4.5 V to 55 V range. The ADA4522-2-KGD is an excellent selection for applications using single-ended supplies of 5 V and 30 V or for applications using higher single supplies and dual supplies of ±2.5 V and ±15 V. The ADA4522-2-KGD uses on-chip filtering to achieve high immunity to electromagnetic interference (EMI).

The ADA4522-2-KGD is fully specified over the −40°C to +125°C extended industrial temperature range.

Additional application and technical information can be found in the ADA4522-2 data sheet.

Known Good Die (KGD): these die are fully guaranteed to data sheet specifications.

Rev. 0
Document Feedback
Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
©2019 Analog Devices, Inc. All rights reserved.
Technical Support
www.analog.com

TABLE OF CONTENTS

REVISION HISTORY

10/2019—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—5.0 V OPERATION

Supply voltage (V_{SY}) = 5.0 V, common-mode voltage (V_{CM}) = V_{SY}/2 V, and T_A = 25°C, unless otherwise specified.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	$V_{CM} = V_{SY}/2$		0.7	5	µV
		−40°C ≤ T_A ≤ +125°C			6.5	µV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			2.5	15	nV/°C
Input Bias Current	I_B			50	150	pA
		−40°C ≤ T_A ≤ +85°C			500	pA
		−40°C ≤ T_A ≤ +125°C			2	nA
Input Offset Current	I_{OS}			80	250	pA
		−40°C ≤ T_A ≤ +85°C			350	pA
		−40°C ≤ T_A ≤ +125°C			500	pA
Input Voltage Range	IVR		0		3.5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 3.5 V	135	155		dB
		−40°C ≤ T_A ≤ +125°C	130			dB
Large Signal Voltage Gain	A_{VO}	Load resistance (R_L) = 10 kΩ, output voltage (V_{OUT}) = 0.5 V to 4.5 V	125	145		dB
		−40°C ≤ T_A ≤ +125°C	125			dB
Input Resistance						
Differential Mode	R_{INDM}			30		kΩ
Common Mode	R_{INCM}			100		GΩ
Input Capacitance						
Differential Mode	C_{INDM}			7		pF
Common Mode	C_{INCM}			35		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 10 kΩ to $V_{SY}/2$	4.97	4.98		V
		−40°C ≤ T_A ≤ +125°C	4.95			V
Output Voltage Low	V_{OL}	R_L = 10 kΩ to $V_{SY}/2$		20	30	mV
		−40°C ≤ T_A ≤ +125°C			50	mV
Continuous Output Current	I_{OUT}	Dropout voltage = 1 V		14		mA
Short-Circuit Current Source	I_{SC+}			22		mA
		T_A = 125°C		15		mA
Short-Circuit Current Sink	I_{SC-}			29		mA
		T_A = 125°C		19		mA
Closed-Loop Output Impedance	Z_{OUT}	Frequency = 1 MHz, closed-loop gain (A_V)= +1		4		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	For single-supply operation, V_{SY} = +4.5 V to +55 V, and for dual-supply operation, V_{SY} = ±2.25 V to ±27.5 V	150	160		dB
		−40°C ≤ T_A ≤ +125°C	145			dB
Supply Current per Amplifier	I_{SY}	Output current (I_{OUT}) = 0 mA		830	900	µA
		−40°C ≤ T_A ≤ +125°C			950	µA

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE						
Slew Rate	SR+	R_L = 10 kΩ, C_L = 50 pF, A_V = 1		1.4		V/µs
	SR−	R_L = 10 kΩ, C_L = 50 pF, A_V = 1		1.3		V/µs
Gain Bandwidth Product	GBP	Input voltage (V_{IN}) = 10 mV p-p, R_L = 10 kΩ, C_L = 50 pF, A_{VO} = 100		2.7		MHz
Unity-Gain Crossover	UGC	V_{IN} = 10 mV p-p, R_L = 10 kΩ, C_L = 50 pF, A_{VO} = 1		3		MHz
−3 dB Closed-Loop Bandwidth	f_{-3dB}	V_{IN} = 10 mV p-p, R_L = 10 kΩ, C_L = 50 pF, A_V = 1		6.5		MHz
Phase Margin	ΦM	V_{IN} = 10 mV p-p, R_L = 10 kΩ, C_L = 50 pF, A_{VO} = 1		64		Degrees
Settling Time to 0.1%	t_S	V_{IN} = 1 V step, R_L = 10 kΩ, C_L = 50 pF, A_V = 1		4		µs
Channel Separation	CS	V_{IN} = 1 V p-p, f = 10 kHz, R_L = 10 kΩ, C_L = 50 pF		98		dB
EMI Rejection Ratio of +IN x	EMIRR	V_{IN} = 100 mV_{PEAK}, frequency = 400 MHz		72		dB
		V_{IN} = 100 mV_{PEAK}, frequency = 900 MHz		80		dB
		V_{IN} = 100 mV_{PEAK}, frequency = 1800 MHz		83		dB
		V_{IN} = 100 mV_{PEAK}, frequency = 2400 MHz		85		dB
NOISE PERFORMANCE						
Total Harmonic Distortion + Noise	THD + N	A_V = +1, frequency = 1 kHz, V_{IN} = 0.6 V rms				
Bandwidth = 80 kHz				0.001		%
Bandwidth = 500 kHz				0.02		%
Peak-to-Peak Voltage Noise	$e_{N\ p-p}$	A_V = 100, frequency = 0.1 Hz to 10 Hz		117		nV p-p
Voltage Noise Density	e_N	A_V = 100, frequency = 1 kHz		5.8		nV/√Hz
Peak-to-Peak Current Noise	$i_{N\ p-p}$	A_V = 100, frequency = 0.1 Hz to 10 Hz		16		pA p-p
Current Noise Density	i_N	A_V = 100, frequency = 1 kHz		0.8		pA/√Hz

ELECTRICAL CHARACTERISTICS—30 V OPERATION

V_{SY} = 30 V, V_{CM} = V_{SY}/2 V, and T_A = 25°C, unless otherwise specified.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	V_{CM} = V_{SY}/2		1	5	µV
		−40°C ≤ T_A ≤ +125°C			7.2	µV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			4	22	nV/°C
Input Bias Current	I_B			50	150	pA
		−40°C ≤ T_A ≤ +85°C			500	pA
		−40°C ≤ T_A ≤ +125°C			3	nA
Input Offset Current	I_{OS}			80	300	pA
		−40°C ≤ T_A ≤ +85°C			400	pA
		−40°C ≤ T_A ≤ +125°C			500	pA
Input Voltage Range	IVR		0		28.5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 28.5 V	145	160		dB
		−40°C ≤ T_A ≤ +125°C	140			dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ, V_{OUT} = 0.5 V to 29.5 V	140	150		dB
		−40°C ≤ T_A ≤ +125°C	135			dB
Input Resistance						
Differential Mode	R_{INDM}			30		kΩ
Common Mode	R_{INCM}			400		GΩ
Input Capacitance						
Differential Mode	C_{INDM}			7		pF
Common Mode	C_{INCM}			35		pF

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 10 kΩ to V_{SY}/2	29.87	29.89		V
		−40°C ≤ T_A ≤ +125°C	29.80			V
Output Voltage Low	V_{OL}	R_L = 10 kΩ to V_{SY}/2		110	130	mV
		−40°C ≤ T_A ≤ +125°C			200	mV
Continuous Output Current	I_{OUT}	Dropout voltage = 1 V		14		mA
Short-Circuit Current Source	I_{SC+}			21		mA
		T_A = 125°C		15		mA
Short-Circuit Current Sink	I_{SC-}			33		mA
		T_A = 125°C		22		mA
Closed-Loop Output Impedance	Z_{OUT}	Frequency = 1 MHz, A_V = +1		4		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = 4.5 V to 55 V	150	160		dB
		−40°C ≤ T_A ≤ +125°C	145			dB
Supply Current per Amplifier	I_{SY}	I_{OUT} = 0 mA		830	900	µA
		−40°C ≤ T_A ≤ +125°C			950	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR+	R_L = 10 kΩ, C_L = 50 pF, A_V = 1		1.8		V/µs
	SR−	R_L = 10 kΩ, C_L = 50 pF, A_V = 1		0.9		V/µs
Gain Bandwidth Product	GBP	V_{IN} = 10 mV p-p, R_L = 10 kΩ, C_L = 50 pF, A_{VO} = 100		2.7		MHz
Unity-Gain Crossover	UGC	V_{IN} = 10 mV p-p, R_L = 10 kΩ, C_L = 50 pF, A_{VO} =1		3		MHz
−3 dB Closed-Loop Bandwidth	$f_{-3\ dB}$	V_{IN} = 10 mV p-p, R_L = 10 kΩ, C_L = 50 pF, A_V = 1		6.5		MHz
Phase Margin	Φ_M	V_{IN} = 10 mV p-p, R_L = 10 kΩ, C_L = 50 pF, A_{VO} = 1		64		Degrees
Settling Time to 0.1%	t_S	V_{IN} = 10 V step, R_L = 10 kΩ, C_L = 50 pF, A_V = 1		12		µs
Settling Time to 0.01%	t_S	V_{IN} = 10 V step, R_L = 10 kΩ, C_L = 50 pF, A_V = 1		14		µs
Channel Separation	CS	V_{IN} = 10 V p-p, f = 10 kHz, R_L = 10 kΩ, C_L = 50 pF		98		dB
EMI Rejection Ratio of +IN x	EMIRR	V_{IN} = 100 mV_{PEAK}, frequency = 400 MHz		72		dB
		V_{IN} = 100 mV_{PEAK}, frequency = 900 MHz		80		dB
		V_{IN} = 100 mV_{PEAK}, frequency = 1800 MHz		83		dB
		V_{IN} = 100 mV_{PEAK}, frequency = 2400 MHz		85		dB
NOISE PERFORMANCE						
Total Harmonic Distortion + Noise	THD + N	A_V = +1, frequency = 1 kHz, V_{IN} = 6 V rms				
Bandwidth = 80 kHz				0.0005		%
Bandwidth = 500 kHz				0.004		%
Peak-to-Peak Voltage Noise	$e_{N\ p-p}$	A_V = 100, frequency = 0.1 Hz to 10 Hz		117		nV p-p
Voltage Noise Density	e_N	A_V = 100, frequency = 1 kHz		5.8		nV/√Hz
Peak-to-Peak Current Noise	$i_{N\ p-p}$	A_V = 100, frequency = 0.1 Hz to 10 Hz		16		pA p-p
Current Noise Density	i_N	A_V = 100, frequency = 1 kHz		0.8		pA/√Hz

ELECTRICAL CHARACTERISTICS—55 V OPERATION

V_{SY} = 55 V, V_{CM} = V_{SY}/2 V, T_A = 25°C, unless otherwise specified.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	V_{CM} = V_{SY}/2		1.5	7	µV
		−40°C ≤ T_A ≤ +125°C			10	µV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			6	30	nV/°C
Input Bias Current	I_B			50	150	pA
		−40°C ≤ T_A ≤ +85°C			500	pA
		−40°C ≤ T_A ≤ +125°C			4.5	nA
Input Offset Current	I_{OS}			80	300	pA
		−40°C ≤ T_A ≤ +85°C			400	pA
		−40°C ≤ T_A ≤ +125°C			500	pA
Input Voltage Range	IVR		0		53.5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 53.5 V	140	144		dB
		−40°C ≤ T_A ≤ +125°C	135			dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ, V_{OUT} = 0.5 V to 54.5 V	135	137		dB
		−40°C ≤ T_A ≤ +125°C	125			dB
Input Resistance						
Differential Mode	R_{INDM}			30		kΩ
Common Mode	R_{INCM}			1000		GΩ
Input Capacitance						
Differential Mode	C_{INDM}			7		pF
Common Mode	C_{INCM}			35		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 10 kΩ to V_{SY}/2	54.75	54.8		V
		−40°C ≤ T_A ≤ +125°C	54.65			V
Output Voltage Low	V_{OL}	R_L = 10 kΩ to V_{SY}/2		200	250	mV
		−40°C ≤ T_A ≤ +125°C			350	mV
Continuous Output Current	I_{OUT}	Dropout voltage = 1 V		14		mA
Short-Circuit Current Source	I_{SC+}			21		mA
		T_A = 125°C		15		mA
Short-Circuit Current Sink	I_{SC-}			32		mA
		T_A = 125°C		22		mA
Closed-Loop Output Impedance	Z_{OUT}	Frequency = 1 MHz, A_V = +1		4		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = 4.5 V to 55 V	150	160		dB
		−40°C ≤ T_A ≤ +125°C	145			dB
Supply Current per Amplifier	I_{SY}	I_{OUT} = 0 mA		830	900	µA
		−40°C ≤ T_A ≤ +125°C			950	µA

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE						
Slew Rate	SR+	R_L = 10 kΩ, C_L = 50 pF, A_V = 1		1.7		V/µs
	SR-	R_L = 10 kΩ, C_L = 50 pF, A_V = 1		0.8		V/µs
Gain Bandwidth Product	GBP	V_{IN} = 10 mV p-p, R_L = 10 kΩ, C_L = 50 pF, A_{VO} = 100		2.7		MHz
Unity-Gain Crossover	UGC	V_{IN} = 10 mV p-p, R_L = 10 kΩ, C_L = 50 pF, A_{VO} = 1		3		MHz
−3 dB Closed-Loop Bandwidth	$f_{-3\ dB}$	V_{IN} = 10 mV p-p, R_L = 10 kΩ, C_L = 50 pF, A_V = 1		6.5		MHz
Phase Margin	Φ_M	V_{IN} = 10 mV p-p, R_L = 10 kΩ, C_L = 50 pF, A_{VO} = 1		64		Degrees
Settling Time to 0.1%	t_S	V_{IN} = 10 V step, R_L = 10 kΩ, C_L = 50 pF, A_V = 1		12		µs
Settling Time to 0.01%	t_S	V_{IN} = 10 V step, R_L = 10 kΩ, C_L = 50 pF, A_V = 1		14		µs
Channel Separation	CS	V_{IN} = 10 V p-p, f = 10 kHz, R_L = 10 kΩ, C_L = 50 pF		98		dB
EMI Rejection Ratio of +IN x	EMIRR	V_{IN} = 100 mV_{PEAK}, frequency = 400 MHz		72		dB
		V_{IN} = 100 mV_{PEAK}, frequency = 900 MHz		80		dB
		V_{IN} = 100 mV_{PEAK}, frequency = 1800 MHz		83		dB
		V_{IN} = 100 mV_{PEAK}, frequency = 2400 MHz		85		dB
NOISE PERFORMANCE						
Total Harmonic Distortion + Noise	THD + N	A_V = +1, frequency = 1 kHz, V_{IN} = 10 V rms				
Bandwidth = 80 kHz				0.0007		%
Bandwidth = 500 kHz				0.003		%
Peak-to-Peak Voltage Noise	$e_{N\ p-p}$	A_V = 100, frequency = 0.1 Hz to 10 Hz		117		nV p-p
Voltage Noise Density	e_N	A_V = 100, frequency = 1 kHz		5.8		nV/√Hz
Peak-to-Peak Current Noise	$i_{N\ p-p}$	A_V = 100, frequency = 0.1 Hz to 10 Hz		16		pA p-p
Current Noise Density	i_N	A_V = 100, frequency = 1 kHz		0.8		pA/√Hz

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage	60 V
Input Voltage Range	(V–) – 300 mV to (V+) + 300 mV
Input Current[1]	±10 mA
Differential Input Voltage	±5 V
Output Short-Circuit Duration to Ground	Indefinite
Temperature Range	
Storage	–65°C to +150°C
Operating	–40°C to +125°C
Junction	–65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

[1] The input pins have clamp diodes connected to the power supply pins. Limit the input current to 10 mA or less whenever input signals exceed the power supply rail by 0.3 V.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

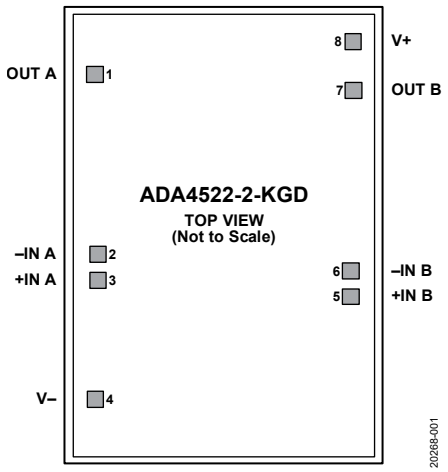

Figure 1. Pad Configuration

Table 5. Pad Function Descriptions[1]

Pad Number	Mnemonic	X Coordinate	Y Coordinate	Description
1	OUT A	−627	+782	Output, Channel A
2	−IN A	−613	−93	Inverting Input, Channel A
3	+IN A	−613	−219	Noninverting Input, Channel A
4	V−	−626	−797	Negative Supply Voltage
5	+IN B	+613	−298	Noninverting Input, Channel B
6	−IN B	+613	−172	Inverting Input, Channel B
7	OUT B	+627	+703	Output, Channel B
8	V+	+626	+944	Positive Supply Voltage

[1] All dimensions are referenced from the center of the die to the center of each bond pad.

OUTLINE DIMENSIONS

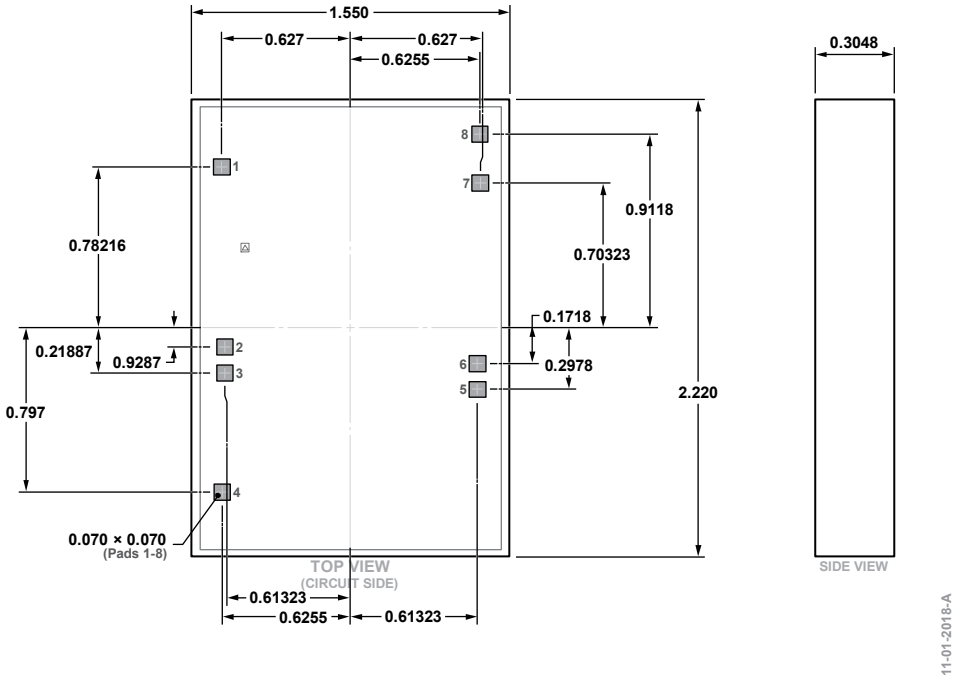

Figure 2. 8-Pad Bare Die [CHIP]
(C-8-17)
Dimensions shown in millimeters

DIE SPECIFICATIONS AND ASSEMBLY RECOMMENDATIONS

Table 6. Die Specifications

Parameter	Value	Unit
Chip Size	1470 × 2140	µm
Scribe Line Width	80 × 80	µm
Die Size	1550 × 2220	µm
Thickness	305	µm
Backside	V– or left floating	V
Passivation	10 kA high density plasma oxide + 7 kA nitride	Not applicable
Bond Pads (Minimum)	70 × 70	µm
Bond Pad Composition	0.5 Aluminum (Al), copper (Cu)	%

Table 7. Assembly Recommendations

Assembly Component	Recommendation
Die Attach	Hitachi CEL 9240HF10AK
Bonding Method	1 mil gold
Bonding Sequence	Unspecified

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADA4522-2-KGD-WP	−40°C to +125°C	8-Pad Bare Die [CHIP], Waffle Pack	C-8-17

[1] Z = RoHS Compliant Part.

©2019 Analog Devices, Inc. All rights reserved. Trademarks and registered trademarks are the property of their respective owners.
D20268-0-10/19(0)