ANALOG DEVICES

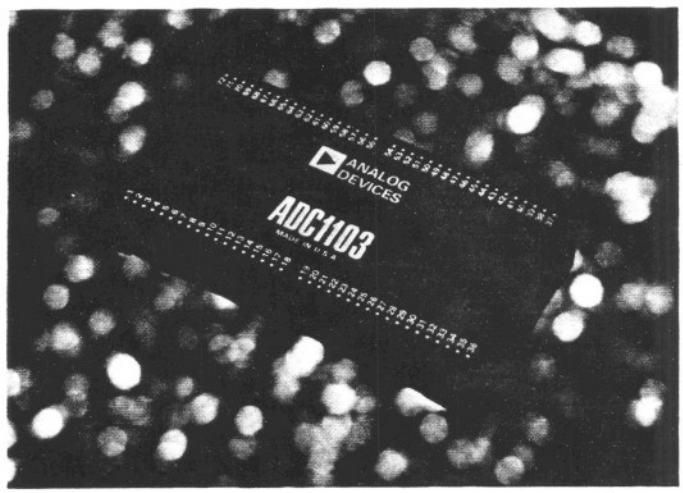
Fast A/D Converter

ADC1103

FEATURES

High Speed
- 8 Bits in 1.0μs max
- 10 Bits in 1.5μs max
- 12 Bits in 3.5μs max

Error Relative to Full Scale ±1LSB max
Gain TC ±10ppm/°C max
User Choice of Three Input Ranges
Small 2″ x 4″ x 0.75″ Module



GENERAL DESCRIPTION

The ADC1103 is a high speed analog-to-digital converter packaged in a small 2″ x 4″ x 0.75″ module. It is available in 8, 10, and 12 bit versions. The 8 bit model performs a conversion in 1.0μs max, the 10 bit version in 1.5μs max, and the 12 bit unit in 3.5μs max. The ADC1103 uses the successive approximations technique to convert analog input voltages into natural binary, offset binary, or two's complement coded parallel output digital data. Careful design and the use of Schottky TTL have resulted in a very fast A/D converter that features an error relative to full scale of only ±1LSB max. The unit has a maximum gain TC of only ±10ppm/°C.

Three analog input ranges are available. The user, with connections at the module pins, can select the 0 to +10V range, the -5V to +5V range, or the -10V to +10V range. When using the 0 to +10V range, the output coding is natural binary. However, when using either the -5V to +5V range or the -10V to +10V range, either offset binary or two's complement coding can be selected. The user can also choose to short cycle the converter (i.e., have it perform conversions of less than the maximum number of bits).

APPLICATIONS

The ADC1103 is a general purpose fast A/D converter. It is especially well suited for applications requiring high throughput rates with no compromise in accuracy. A typical application would be a multiple channel data acquisition system, where a high throughput rate/channel is needed. The ADC1103's high speed makes it an excellent choice for such applications as fast Fourier transform analysis, radar pulse analysis, conversion of analog data acquired from simultaneous sample-and-hold data collection systems, and for conversion of analog data to be fed into digital filters and correlators.

TIMING

As shown in Figure 1, the STATUS output is set to a logic "1" on the leading edge of the convert command pulse. On the trailing edge of the convert command pulse, the MSB output is set to a logic "1", the remaining bit outputs are set to "0", and the conversion commences.

The output data is valid 4ns prior to the "1" to "0" transition of the STATUS output (or "0" to "1" transition of the $\overline{\text{STATUS}}$ output). This set-up time is sufficient to allow the output data to be strobed into a following Schottky TTL register on either of these two edges. If a standard TTL register is used, data should not be strobed into it until at least 16ns after the STATUS and $\overline{\text{STATUS}}$ transitions occur. The SERIAL DATA output (which does not appear on the standard unit) is of the nonreturn-to-zero type (NRZ). The data is available, MSB first, on successive "0" to "1" DATA STROBE transitions.

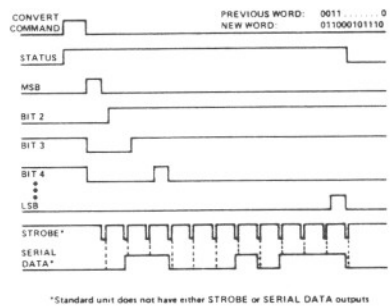


Figure 1. Timing Diagram

Route 1 Industrial Park; P.O. Box 280; Norwood, Mass. 02062
Tel: 617/329-4700 TWX: 710/394-6577
West Coast Tel: 213/595-1783
Mid-West Tel: 312/297-8710

SPECIFICATIONS (typical @ +25°C and nominal supply voltages, unless otherwise noted)

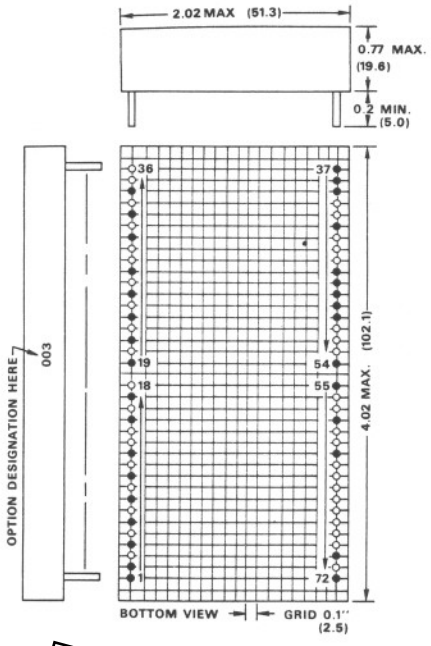
RESOLUTION	
ADC1103-001	8 Bits
ADC1103-002	10 Bits
ADC1103-003	12 Bits
CONVERSION TIME	
ADC1103-001	1.0μs, max
ADC1103-002	1.5μs, max
ADC1103-003	3.5μs, max
ACCURACY[1]	
Error Relative to Full Scale[2]	±1LSB max
Quantization Error	±½LSB max
Differential Nonlinearity Error[2]	±1LSB max
Missing Codes[3]	No missing codes from 0 to +70°C
TEMPERATURE COEFFICIENTS	
Gain TC	±10ppm/°C of reading, max
Zero TC (Unipolar Input)	±5ppm/°C of full scale, max
(Bipolar Input)	±10ppm/°C of range, max
Differential Nonlinearity TC	±5ppm/°C of range, max
INPUT VOLTAGE RANGES	0 to +10V, ±10V, ±5V
INPUT IMPEDANCE	
0 to +10V and ±5V Ranges	2.50k ohms
±10V Range	5.00k ohms
CONVERT COMMAND	Positive pulse, 50ns min width, 1μs max rise and fall times, TTL compatible
PARALLEL DATA OUTPUT	
With Unipolar Input Range	Positive true binary
With Bipolar Input Range	Positive true offset binary or two's complement
SERIAL DATA OUTPUT[4]	Bits valid on successive "0" to "1" transitions of Data Strobe pulses, with MSB first. TTL compatible.
STATUS OUTPUT	"1" during conversion. Complement also available. TTL compatible.
LOGIC FANOUTS AND LOADINGS	
Convert Command Input	5 TTL unit loads
Parallel Data Outputs	8 TTL unit loads/bit
STATUS Output	8 TTL unit loads
$\overline{\text{STATUS}}$ Output	8 TTL unit loads
Serial Data Output[4]	8 TTL unit loads
Clock Inhibit Input	1 TTL unit load
Data Strobe Output[4]	8 TTL unit loads
ADJUSTMENTS	
Zero (or Offset)	External 100k ohm potentiometer across ±15V with slider to pin 46.
Gain	External 100k ohm potentiometer across ±15V with slider to pin 70.
POWER REQUIREMENTS	+15VDC ±3% @ 85mA max -15VDC ±3% @ -80mA max +5VDC ±5% @ 525mA max
POWER SUPPLY SENSITIVITY[5]	±0.003%/%△V (±15V only) typical ±0.007%/%△V (±15V only) max
TEMPERATURE RANGE	
Operating	0 to +70°C
Storage	-55°C to +125°C
PRICES (1-9)	
ADC1103-001	$473.
ADC1103-002	$484.
ADC1103-003	$495.

[1] Warm-up time to rated accuracy is 5 minutes.
[2] ±½LSB for the ADC1103-001 and ADC1103-002.
[3] Except the ADC1103-003 which is guaranteed to have no missing codes at +25°C.
[4] The standard unit does not have a serial output, or a data strobe output. Contact the factory for price and availability of models with serial output.
[5] This specification is valid only when the +15V supply tracks the -15V supply (or vice versa).

Specifications subject to change without notice.

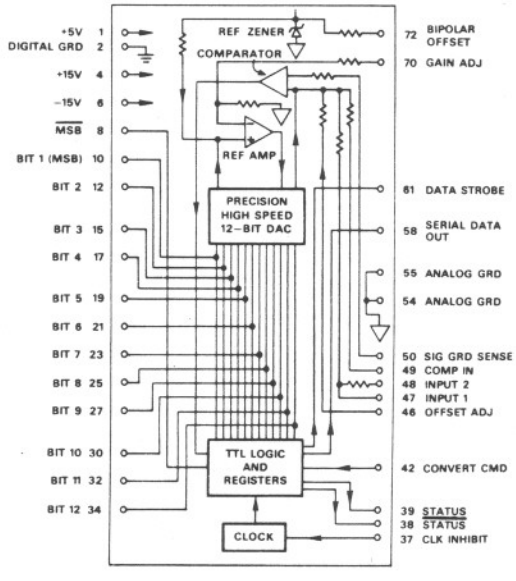
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



NOTE:
Terminal pins installed only in shaded hole locations.
All pins are 0.019" ±0.001" (0.48mm ±0.03mm) dia. half-hard brass, gold plated per MIL-G-45204B, Class I, Type II.
For plug-in mounting card, order Board No. AC1549 @ $25.00.

BLOCK DIAGRAM AND PIN DESIGNATIONS



NOTE:
The standard model does not have a serial output, and therefore pins 58 and 61 are deleted from it.
The ADC1103-002 does not contain pins 32 and 34. The ADC1103-001 does not contain pins 27, 30, 32 and 34.

ANALOG SIGNAL INPUT CONNECTIONS

The ADC1103 offers a choice of three input ranges, any of which may be selected by the user. The table below shows the connections required for each range.

INPUT RANGE SELECTION

Input Range in Volts	Connect Input Signal To	Connect Pin 49 To
0 to +10V	Pin 47	Pins 54 and 55*
-5V to +5V	Pin 47	Pin 72
-10V to +10V	Pin 48	Pin 72

*Also connect a 3.0kΩ ±5% resistor between pin 72 and pins 54 and 55.

Signal ground sense (pin 50) should normally be jumpered to analog ground (pins 54 and 55). However, in the event there is an offset in the ground wiring, it may be possible to eliminate it by connecting pin 50 instead directly to the signal or analog ground of the device feeding the analog input signal to the ADC1103. In any case, pin 50 *must not* be left open with nothing connected to it.

If a high input impedance is required, it can be achieved by using a high speed operational amplifier as an input buffer. Analog Devices' Model 48 fast settling differential amplifier, packaged in a small 1.125" x 1.125" x 0.4" module, is an ideal choice.

OUTPUT CODING

When using the 0 to +10V range, the ouput coding is natural binary, positive true. When using the ±5V or ±10V ranges, the coding can be either positive true offset binary or positive true two's complement at the user's option. The only difference between the two codes is the state of the MSB. The MSB output (pin 10) is used for offset binary coding, while the $\overline{\text{MSB}}$ output (pin 8) is used for two's complement coding.

GAIN AND OFFSET ADJUSTMENTS

Gain and offset adjustments are performed with external 100k ohm, 20 turn potentiometers connected across the ±15V power supply. The slider of the gain adjustment potentiometer is connected to pin 70, and the slider of the offset potentiometer is connected to pin 46. The gain adjustment potentiometer has a range of about ±20 LSB's, and the offset potentiometer has a range of about ±10 LSB's.

Proper gain and offset calibration requires great care, and the use of extremely sensitive and accurate reference instruments. The voltage source used as a signal source must be very stable. It should be capable of being set to within 1/10LSB of the desired value at both ends of its range.

The gain and offset calibrations will be independent of each other if the offset adjustment (or zero adjustment, if using the 0 to +10V range) is made first. These adjustments are not made with zero and full scale input signals, and it may be helpful to understand why. An A/D converter will produce a given digital word output for a small range of input signals, the average width of the range being one LSB. If the input test signal is set at a point where the converter should be on the verge of switching to the next value, the unit can be calibrated so that it does switch to the next value at just that point. With a high speed convert command rate and a visual display, these adjustments can be performed in a very accurate and sensitive way. Analog Devices' Conversion Handbook gives more detailed information on testing and calibrating A/D and D/A converters.

The following table will be useful in calculating the input voltage settings needed during gain and offset calibration.

VOLTAGE EQUIVALENT OF ½LSB FOR CONVERTERS OF VARIOUS RESOLUTIONS AND INPUT VOLTAGE RANGES

Converter Resolution	Input Voltage Range*		
	5 Volts	10 Volts	20 Volts
8 Bits	9.77mV	19.53mV	39.06mV
10 Bits	2.44mV	4.88mV	9.77mV
12 Bits	0.61mV	1.22mV	2.44mV

*Where range = +F.S. – (-F.S.)

OFFSET (OR ZERO) CALIBRATION

Set the input voltage precisely to ½LSB above zero when using the 0 to +10V range, or to ½LSB above nominal minus full scale when using either the ±5V or ±10V range. Then adjust the offset potentiometer until the converter is just on the verge of switching between all "0's" and having just its LSB on.

GAIN CALIBRATION

Set the input voltage precisely to a value equal to ½LSB less than the point where the converter would have all bits at a logic "1". Note that this is 1½LSB's less than nominal full scale. For example, full scale of a 0 to +10V 12 bit A/D converter is actually +9.9976 Volts. Gain adjustment should be made with an input ½LSB less than that value, or +9.9963 Volts. Adjust the gain potentiometer to the point where the last bit just comes on. In a 12 bit converter, this would be where the output code just barely changes from 111111111110 to 111111111111.

CLOCK INHIBIT CONNECTIONS

Clock Inhibit (pin 37) normally must be externally jumpered to $\overline{\text{STATUS}}$ (pin 38). The only exception to this would occur when it is desired to short cycle the converter (i.e., have it perform a conversion of less than the maximum number of bits). In such an instance, pin 37 would instead be jumpered to the N + 1 bit output, where N is the number of bits in the conversion. For example, the 12 bit ADC1103–003 would perform 7 bit conversions if pin 37 were jumpered to the Bit 8 output (pin 25). The conversion time would be 7/12 x 3.5μs max = 2.04μs max.

When operating the converter in the short cycle mode, the STATUS (pin 39) and $\overline{\text{STATUS}}$ (pin 38) outputs are no longer valid. Instead, the N + 1 bit output becomes a $\overline{\text{STATUS}}$ output (i.e., "0" during a conversion).

WIRING CONSIDERATIONS

Because of the ADC1103's very high speed and its 12 bit capability, good wiring practices are essential for best performance. Care should be taken to ensure that the analog ground connection is a good, solid connection. The digital inputs and outputs should be kept away from the analog signals. Analog ground and digital ground are tied together internally, but it is important that no digital ground signals be present in a path serving as an analog ground return. When de-

signing a PC board to accept the ADC1103, it is suggested that as much ground plane area as possible be left underneath the ADC1103.

The +5V and ±15V power inputs are internally bypassed, but it is recommended that additional bypass capacitors be added externally. The capacitors should be located as near the module pins as possible. The +5V bypass capacitor should be connected between the +5V input (pin 1) and digital ground (pin 2). The ±15V bypass capacitors should be connected between pin 4 and analog ground, and pin 6 and analog ground. The capacitors would typically be 10μF (or greater) tantalum types.

RECOMMENDED POWER SUPPLIES

The ADC1103 requires +15 volts at 85mA max, -15V at 80mA max, and +5V at 525mA max. Analog Devices' Model 902 ±15V modular power supply is rated at 100mA, making it an ideal choice for the ADC1103's ±15 volt power requirements. Analog Devices' Model 905 modular power supply puts out +5V at up to 1.0 amperes, which makes it well suited to supplying the ADC1103's +5V needs. The Model 902 is priced at $49 (1-9) and the Model 905 is priced at $69 (1-9).

IMPROVING POWER SUPPLY REJECTION

Most of the power supply sensitivity called out in the specifications is due to variations in the voltage applied to the gain and offset adjustment potentiometers. This specification can therefore be improved by at least an order of magnitude by using the circuit shown below in Figure 2.

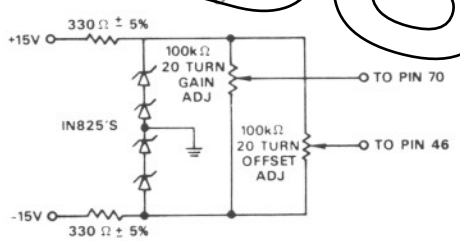


Figure 2. Zener Diode Isolated Adjustment Pots

SERIAL OUTPUT

The standard ADC1103 *does not* include a serial output. For this reason, SERIAL OUTPUT (pin 58) and DATA STROBE (pin 61) do not appear on the standard unit.
The conversion time on any units containing a serial output is increased by about 20ns/bit. The data is transmitted MSB first, and the coding is natural binary for a unipolar input, or offset binary for a bipolar input. Each serial data bit is valid beginning 16ns prior to the rising edge ("0" to "1" transition) of its strobe pulse. This permits the serial data to be clocked into a receiving shift register on successive strobe pulse rising edges. Each of the strobe pulses is between 16ns and 22ns wide, and in a complete conversion there are exactly as many strobe pulses as there are bits.

THE AC1549 MOUNTING CARD

The ADC1103's very high speed demands that considerable thought be given to the wiring connected to the module, even when simply evaluating the unit in a temporary laboratory bench set-up. To assist with such evaluations, an AC1549 Mounting Card is available. This 4½" x 6" printed circuit card has sockets that allow an ADC1103 to be plugged directly onto it. It also has provisions for an Analog Devices' Model 48 fast settling op amp which, if used, serves as an input buffer. The card includes gain and offset adjustment potentiometers, and power supply bypass capacitors. It mates with a Cinch 251-22-30-160 (or equivalent) edge connector, which is supplied with the card.

REPETITIVE CONVERSIONS

When making repetitive conversions, a small time interval must be allowed between the completion of one conversion and the beginning of the next. This results in a maximum throughput rate of 769kHz for the ADC1103-001, 526kHz for the ADC1103-002 and 250kHz for the ADC1103-003.

The ADC1103 can be interrupted during a conversion with a new convert command. The unit will reset and begin a new conversion. However, if it is so interrupted, the convert command pulse should be at least 300ns wide for the ADC1103-001, at least 400ns for the ADC1103-002, and at least 500ns wide for the ADC1103-003. This will give the ADC1103's clock sufficient time to reset before beginning the new conversion.

HIGH THROUGHPUT RATE DATA ACQUISITION

The ADC1103's high speed allows it to be used in data acquisition applications where a high throughput rate is required. For example, Figure 3 shows a sequentially addressed, eight channel data acquisition subsystem capable of acquiring data to 12 bit accuracy at a 220kHz throughput rate. The system uses an Analog Devices' MPX-8A Multiplexer, SHA-2A Sample-and-Hold Amplifier, and an ADC1103-003. Its sampling rate/channel is a very respectable 27.5kHz.

When using this system, the convert command should be at least 500ns wide. This allows the SHA-2A to settle to 12 bit accuracy before the ADC1103 commences its conversion. The SHA-2A is switched into the HOLD mode on the rising edge of the convert command pulse, but the conversion does not actually begin until the falling edge of the convert command pulse occurs.

The MPX-8A is advanced to the next channel at the same time the SHA-2A is switched into the HOLD mode. This allows the multiplexer to settle to a new analog input while the conversion of the previous channel's input is in progress. In this way, the MPX-8A's settling time does not affect the maximum throughput rate.

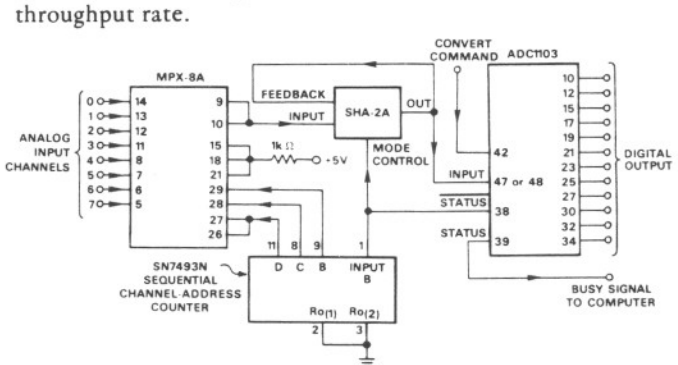


Figure 3. High Speed Data Acquisition Subsystem