ANALOG DEVICES

Dual RF PLL Frequency Synthesizers

ADF4206/ADF4207/ADF4208

FEATURES

ADF4206: 550 MHz/550 MHz
ADF4207: 1.1 GHz/1.1 GHz
ADF4208: 2.0 GHz/1.1 GHz
2.7 V to 5.5 V Power Supply
Selectable Charge Pump Supply (VP) Allows Extended Tuning Voltage in 3 V Systems
Selectable Charge Pump Currents
On-Chip Oscillator Circuit
Selectable Dual Modulus Prescaler
RF2: 32/33 or 64/65
RF1: 32/33 or 64/65
3-Wire Serial Interface
Power-Down Mode

APPLICATIONS

Wireless Handsets (GSM, PCS, DCS, CDMA, WCDMA)
Base Stations for Wireless Radio (GSM, PCS, DCS, CDMA, WCDMA)
Wireless LANS
Communications Test Equipment
CATV Equipment

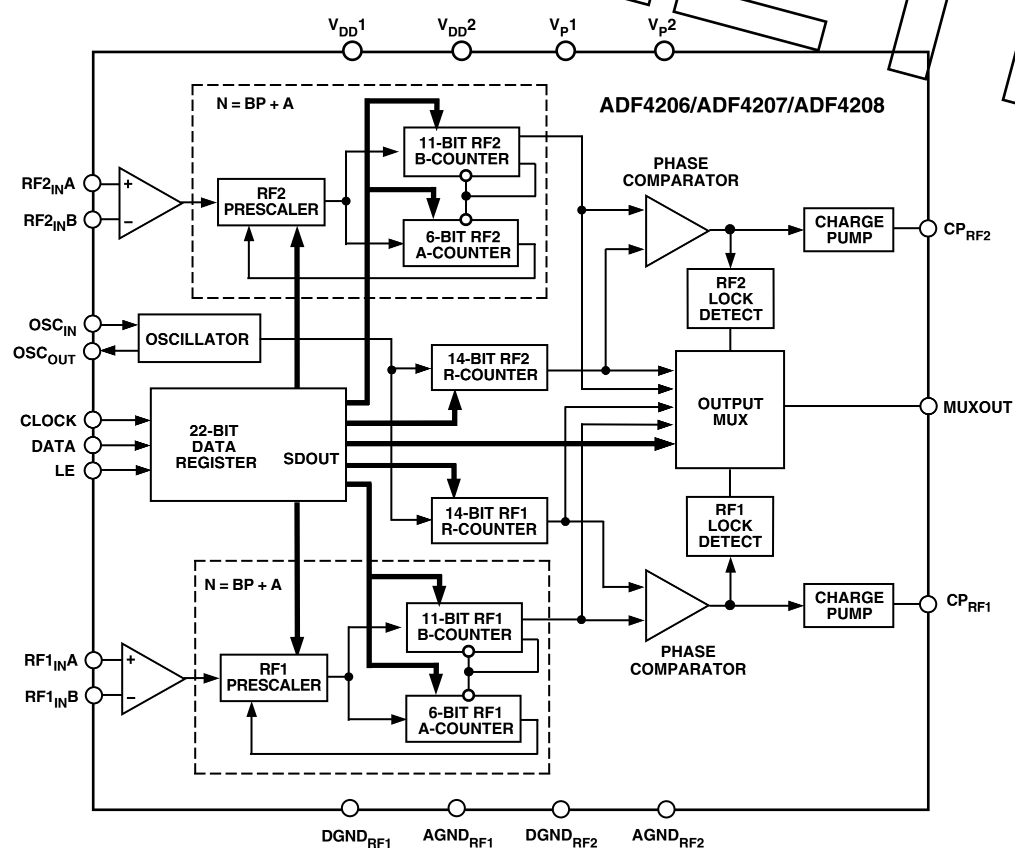
GENERAL DESCRIPTION

The ADF4206 family of dual frequency synthesizers can be used to implement local oscillators in the upconversion and downconversion sections of wireless receivers and transmitters. Each synthesizer consists of a low-noise digital PFD (Phase Frequency Detector), a precision charge pump, a programmable reference divider, programmable A and B counters and a dual-modulus prescaler (P/P + 1). The A (6-bit) and B (11-bit) counters, in conjunction with the dual modulus prescaler (P/P + 1), implement an N divider (N = BP + A). In addition, the 14-bit reference counter (R Counter), allows selectable REFIN frequencies at the PFD input. The on-chip oscillator circuitry allows the reference input to be derived from crystal oscillators.

A complete PLL (Phase-Locked Loop) can be implemented if the synthesizers are used with an external loop filter and VCOs (Voltage Controlled Oscillators).

Control of all the on-chip registers is via a simple 3-wire interface. The devices operate with a power supply ranging from 2.7 V to 5.5 V and can be powered down when not in use.

FUNCTIONAL BLOCK DIAGRAM



REV. 0

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ADF4206/ADF4207/ADF4208–SPECIFICATIONS[1] ($V_{DD}1 = V_{DD}2$ = 3 V ± 10%, 5 V ± 10%; $V_{DD}1$, $V_{DD}2 \le V_P1$, $V_P2 \le$ 6.0 V; $AGND_{RF1} = DGND_{RF1} = AGND_{RF2} = DGND_{RF2}$ = 0 V; $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted, dBm referred to 50 Ω.)

Parameter	B Version	B Chips[2]	Unit	Test Conditions/Comments
RF/IF CHARACTERISTICS (3 V)				See Figure 2 for input circuit.
RF1 Input Frequency ($RF1_{IN}$)				Use a square wave for frequencies lower than f_{MIN}.
ADF4206	0.05/0.55	0.05/0.55	GHz min/max	
ADF4207	0.08/1.1	0.08/1.1	GHz min/max	
ADF4208	0.08/2.0	0.08/2.0	GHz min/max	
RF Input Sensitivity	–15/+4	–15/+4	dBm min/max	
IF Input Frequency ($RF2_{IN}$)				
ADF4206	0.05/0.55	0.05/0.55	GHz min/max	
ADF4207/ADF4208	0.08/1.1	0.08/1.1	GHz min/max	
IF Input Sensitivity	–15/+4	–15/+4	dBm min/max	
Maximum Allowable Prescaler Output Frequency[3]	165	165	MHz max	
RF CHARACTERISTICS (5 V)				
RF1 Input Frequency ($RF1_{IN}$)				Use a square wave for frequencies lower than f_{MIN}.
ADF4206	0.05/0.55	0.05/0.55	GHz min/max	
ADF4207	0.08/1.1	0.08/1.1	GHz min/max	
ADF4208	0.08/2.0	0.08/2.0	GHz min/max	
RF Input Sensitivity	–10/+4	–10/+4	dBm min/max	
IF Input Frequency ($RF2_{IN}$)			MHz min/max	
ADF4206	0.05/0.55	0.05/0.55	GHz min/max	
ADF4207/ADF4208	0.08/1.1	0.08/1.1	GHz min/max	
IF Input Sensitivity	–10/+4	–10/+4	dBm min/max	
Maximum Allowable Prescaler Output Frequency[3]	200	200	MHz max	
REFIN CHARACTERISTICS				
REFIN Input Frequency	5/40	5/40	MHz min/max	For f < 5 MHz Use Square Wave 0 to V_{DD}
REFIN Input Sensitivity[4]	–2	–2	dBm min	AC-Coupled. When DC-Coupled, 0 to V_{DD} Max (CMOS-Compatible)
REFIN Input Capacitance	10	10	pF max	
REFIN Input Current	±100	±100	µA max	
PHASE DETECTOR				
Phase Detector Frequency[5]	55	55	MHz max	
CHARGE PUMP				
I_{CP} Sink/Source				
High Value	5	5	mA typ	
Low Value	1.25	1.25	mA typ	
Absolute Accuracy	2.5	2.5	% typ	
I_{CP} Three-State Leakage Current	1	1	nA typ	
LOGIC INPUTS				
V_{INH}, Input High Voltage	$0.8 \times V_{DD}$	$0.8 \times V_{DD}$	V min	
V_{INL}, Input Low Voltage	$0.2 \times V_{DD}$	$0.2 \times V_{DD}$	V max	
I_{INH}/I_{INL}, Input Current	±1	±1	µA max	
C_{IN}, Input Capacitance	10	10	pF max	
LOGIC OUTPUTS				
V_{OH}, Output High Voltage	V_{DD} – 0.4	V_{DD} – 0.4	V min	I_{OH} = 500 µA
V_{OL}, Output Low Voltage	0.4	0.4	V max	I_{OL} = 500 µA
POWER SUPPLIES				
$V_{DD}1$	2.7/5.5	2.7/5.5	V min/V max	
$V_{DD}2$	$V_{DD}1$	$V_{DD}1$		
V_P	$V_{DD}1$/6.0	$V_{DD}1$/6.0	V min/V max	$V_{DD}1$, $V_{DD}2 \le V_P1$, $V_P2 \le$ 6.0 V
I_{DD} ($I_{DD}1 + I_{DD}2$)[6]				
ADF4206	14	14	mA max	9.5 mA Typical at V_{DD} = 3 V, T_A = 25°C
ADF4207	16.5	16.5	mA max	11 mA Typical at V_{DD} = 3 V, T_A = 25°C
ADF4208	21	21	mA max	14 mA Typical at V_{DD} = 3 V, T_A = 25°C
$I_{DD}1$				
ADF4206	8	8	mA max	5.5 mA Typical at V_{DD} = 3 V, T_A = 25°C
ADF4207	9	9	mA max	6 mA Typical at V_{DD} = 3 V, T_A = 25°C
ADF4208	14	14	mA max	9 mA Typical at V_{DD} = 3 V, T_A = 25°C
$I_{DD}2$				
ADF4206	7.5	7.5	mA max	5 mA Typical at V_{DD} = 3 V, T_A = 25°C
ADF4207	8.5	8.5	mA max	5.5 mA Typical at V_{DD} = 3 V, T_A = 25°C
ADF4208	9	9	mA max	5.5 mA Typical at V_{DD} = 3 V, T_A = 25°C
I_P ($I_P1 + I_P2$)	1	1	mA max	T_A = 25°C
Low-Power Sleep Mode	0.5	0.5	µA typ	

Parameter	B Version	B Chips[2]	Unit	Test Conditions/Comments
NOISE CHARACTERISTICS				
Phase Noise Floor (RF1)[7]				
ADF4206	–169	–169	dBc/Hz typ	@ 25 kHz PFD Frequency
ADF4207	–171	–171	dBc/Hz typ	@ 25 kHz PFD Frequency
ADF4208	–173	–173	dBc/Hz typ	@ 25 kHz PFD Frequency
ADF4206	–160	–160	dBc/Hz typ	@ 200 kHz PFD Frequency
ADF4207	–162	–162	dBc/Hz typ	@ 200 kHz PFD Frequency
ADF4208	–164	–164	dBc/Hz typ	@ 200 kHz PFD Frequency
Phase Noise Performance[8]				@ VCO Output
ADF4206 (RF1, RF2)	–92	–92	dBc/Hz typ	@ 540 MHz Output, 200 kHz at PFD
ADF4207 (RF1, RF2)	–90	–90	dBc/Hz typ	@ 900 MHz Output, 200 kHz at PFD
ADF4207 (RF1, RF2)[9]	–81	–81	dBc/Hz typ	@ 836 MHz, 30 kHz at PFD
ADF4208 (RF1)	–85	–85	dBc/Hz typ	@ 1750 MHz Output, 200 kHz at PFD
ADF4208 (RF1)	–91	–91	dBc/Hz typ	@ 900 MHz Output, 200 kHz at PFD
ADF4208 (RF1)[10]	–66	–66	dBc/Hz typ	@ 1750 MHz Output, 200 kHz at PFD
ADF4208 (RF2)	–89	–89	dBc/Hz typ	@ 900 MHz Output, 200 kHz at PFD
Spurious Signals				
RF1, RF2 (20 kHz Loop B/W)	–80/–84	–80/–84	dB typ	@ 200 kHz/400 kHz and 200 kHz PFD
RF1, RF2 (1 kHz Loop B/W)	–65/–73	–65/–73	dB typ	@10 kHz/20 kHz and 10 kHz PFD

NOTES

[1]Operating temperature range is as follows: B Version: –40°C to +85°C.

[2]The B Chip specifications are given as typical values.

[3]This is the maximum operating frequency of the CMOS counters. The prescaler value should be chosen to ensure that the RF input is divided down to a frequency that is less than this value.

[4]$V_{DD}1 = V_{DD}2 = 3$ V; For $V_{DD}1 = V_{DD}2 = 5$ V, use CMOS-compatible levels.

[5]Guaranteed by design. Sample tested to ensure compliance.

[6]Typical values apply for $V_{DD} = 3$ V; P = 32; $RF1_{IN}1/RF2_{IN}2$ for ADF4206 = 540 MHz; $RF1_{IN}1/RF2_{IN}2$ for ADF4207 = 900 MHz; $RF1_{IN}1/RF2_{IN}2$ for ADF4208 = 900 MHz.

[7]The synthesizer phase noise floor is estimated by measuring the in-band phase noise at the output of the VCO and subtracting 20 logN (where N is the N divider value).

[8]The phase noise is measured at a 1 kHz unless otherwise noted. The phase noise is measured with the EVAL-ADF4206/ADF4207EB or the EVAL-AD4208EB Evaluation Board and the HP8562E Spectrum Analyzer. The spectrum analyzer provides the REFIN for the synthesizer (f_{REFOUT} = 10 MHz @ 0 dBm).

[9]f_{REFIN} = 10 MHz; f_{PFD} = 30 kHz; Offset Frequency = 300 Hz; $f_{RF/IF}$ = 836 MHz; N = 27866; Loop B/W = 3 kHz.

[10]f_{REFIN} = 10 MHz; f_{PFD} = 10 kHz; Offset Frequency = 200 Hz; f_{RF} = 1750 MHz; N = 175000; Loop B/W = 1 kHz.

Specifications subject to change without notice.

TIMING CHARACTERISTICS

($V_{DD}1 = V_{DD}2 = 3$ V ± 10%, 5 V ± 10%; $V_{DD}1$, $V_{DD}2 \leq V_P1$, $V_P2 \leq 6.0$ V; $AGND_{RF1} = DGND_{RF1} = AGND_{RF2} = DGND_{RF2} = 0$ V; $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted, dBm referred to 50 Ω.)

Parameter	Limit at T_{MIN} to T_{MAX} (B Version)	Unit	Test Conditions/Comments
t_1	10	ns min	DATA to CLOCK Setup Time
t_2	10	ns min	DATA to CLOCK Hold Time
t_3	25	ns min	CLOCK High Duration
t_4	25	ns min	CLOCK Low Duration
t_5	10	ns min	CLOCK to LE Setup Time
t_6	20	ns min	LE Pulsewidth

NOTES
Guaranteed by design but not production tested.
Specification subject to change without notice.

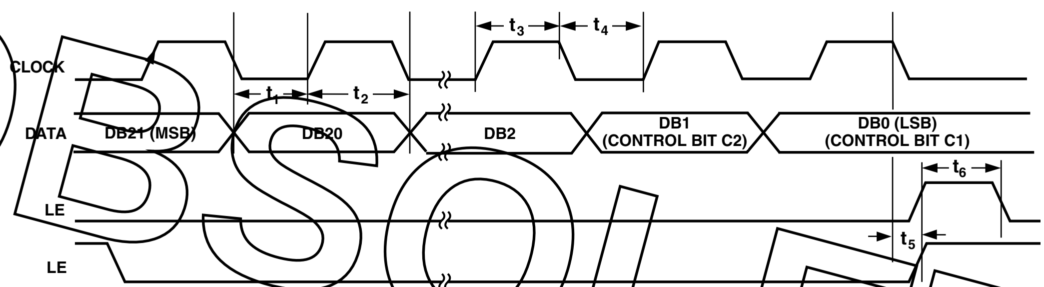


Figure 1. Timing Diagram

ABSOLUTE MAXIMUM RATINGS[1, 2]

(T_A = 25°C unless otherwise noted.)

$V_{DD}1$ to GND[3] . . . . –0.3 V to +7 V
$V_{DD}1$ to $V_{DD}2$ . . . . –0.3 V to +0.3 V
V_P1, V_P2 to GND . . . . –0.3 V to +7 V
V_P1, V_P2 to $V_{DD}1$ . . . . –0.3 V to +5.5 V
Digital I/O Voltage to GND . . . . . . –0.3 V to DV_{DD} + 0.3 V
Analog I/O Voltage to GND . . . . . . –0.3 V to V_P + 0.3 V
OSC_{IN}, OSC_{OUT}, $RF1_{IN}$ (A, B),
$RF2_{IN}$ (A, B) to GND . . . . . . –0.3 V to V_{DD} + 0.3 V
$RF_{IN}A$ to $RF_{IN}B$ (RF1, RF2) . . . . . . ±320 mV
Operating Temperature Range
Industrial (B Version) . . . . . . –40°C to +85°C
Storage Temperature Range . . . . . . –65°C to +150°C
Maximum Junction Temperature . . . . . . 150°C
TSSOP θ_{JA} Thermal Impedance . . . . . . 150.4°C/W
CSP θ_{JA} (Paddle Soldered) . . . . . . 122°C/W
CSP θ_{JA} (Paddle Not Soldered) . . . . . . 216°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) . . . . . . 215°C
Infrared (15 sec) . . . . . . 220°C

NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]This device is a high-performance RF integrated circuit with an ESD rating of < 2 kV and it is ESD sensitive. Proper precautions should be taken for handling and assembly.
[3]GND = AGND = DGND = 0 V.

TRANSISTOR COUNT

11749 (CMOS) and 522 (Bipolar).

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
ADF4206BRU	–40°C to +85°C	Thin Shrink Small Outline Package (TSSOP)	RU-16
ADF4207BRU	–40°C to +85°C	Thin Shrink Small Outline Package (TSSOP)	RU-16
ADF4208BRU	–40°C to +85°C	Thin Shrink Small Outline Package (TSSOP)	RU-20

*Contact the factory for chip availability.

CAUTION

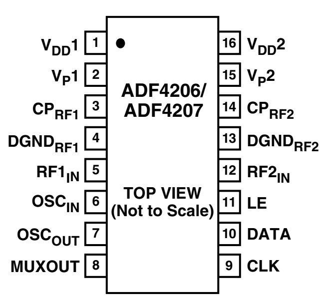
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADF4206/ADF4207/ADF4208 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic ADF4206/ ADF4207	ADF4208	Function
1	$V_{DD}1$	$V_{DD}1$	Positive Power Supply for the RF1 Section. A 0.1 µF capacitor should be connected between this pin and the RF1 ground pin, $DGND_{RF1}$. $V_{DD}1$ should have a value of between 2.7 V and 5.5 V. $V_{DD}1$ must have the same potential as $V_{DD}2$.
2	V_P1	V_P1	Power Supply for the RF1 Charge Pump. This should be greater than or equal to V_{DD}.
3	CP_{RF1}	CP_{RF1}	Output from the RF1 Charge Pump. This is normally connected to a loop filter which, in turn, drives the input to an external VCO.
4	$DGND_{RF1}$	$DGND_{RF1}$	Ground Pin for the RF1 Digital Circuitry.
5	$RF1_{IN}$	$RF1_{IN}A$	Input to the RF1 Prescaler. This low-level input signal is normally taken from the RF1 VCO.
6	OSC_{IN}	$RF_{IN}B$	Complementary Input to the RF1 Prescaler of the ADF4208. This point should be decoupled to the ground plane with a small bypass capacitor.
7	OSC_{OUT}	$AGND_{RF1}$	Ground Pin for the RF1 Analog Circuitry.
8	MUXOUT	OSC_{IN}	Oscillator Input. It has a $V_{DD}/2$ threshold and can be driven from an external CMOS or TTL logic gate.
9	CLK	OSC_{OUT}	Oscillator Output.
10	DATA	MUXOUT	This multiplexer output allows either the IF/RF lock detect, the scaled RF, or the scaled Reference Frequency to be accessed externally. See Table V.
11	LE	CLK	Serial Clock Input. This serial clock is used to clock in the serial data to the registers. The data is latched into the 22-bit shift register on the CLK rising edge. This input is a high impedance CMOS input.
12	$RF2_{IN}$	DATA	Serial Data Input. The serial data is loaded MSB first with the two LSBs being the control bits. This input is a high impedance CMOS input.
13	$DGND_{RF2}$	LE	Load Enable, CMOS Input. When LE goes high, the data stored in the shift registers is loaded into one of the four latches, the latch being selected using the control bits.
14	CP_{RF2}	$AGND_{RF2}$	Ground Pin for the RF2 Analog Circuitry.
15	V_P2	$RF2_{IN}B$	Complementary Input to the RF2 Prescaler. This point should be decoupled to the ground plane with a small bypass capacitor.
16	$V_{DD}2$	$RF2_{IN}A$	Input to the RF2 Prescaler. This low-level input signal is normally ac-coupled to the external VCO.
17		$DGND_{RF2}$	Ground Pin for the RF2, Digital, Interface, and Control Circuitry.
18		CP_{RF2}	Output from the RF2 Charge Pump. This is normally connected to a loop filter that drives the input to an external VCO.
19		V_P2	Power Supply for the RF2 Charge Pump. This should be greater than or equal to V_{DD}.
20		$V_{DD}2$	Positive Power Supply for the RF2, Interface, and Oscillator Sections. A 0.1 µF capacitor should be connected between this pin and the RF2 ground Pin, $DGND_{RF2}$. $V_{DD}2$ should have a value between 2.7 V and 5.5 V. $V_{DD}2$ must have the same potential as $V_{DD}1$.

PIN CONFIGURATIONS

TSSOP



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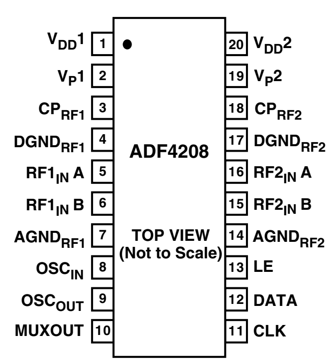
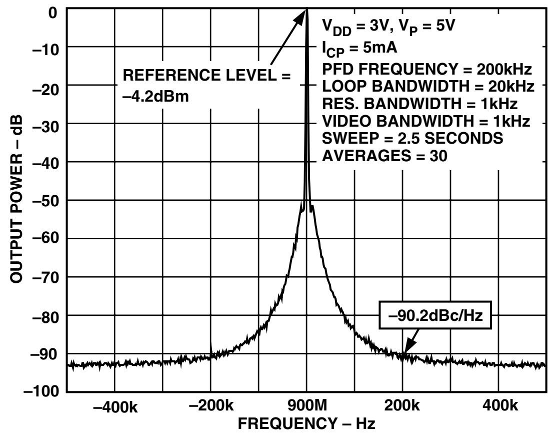


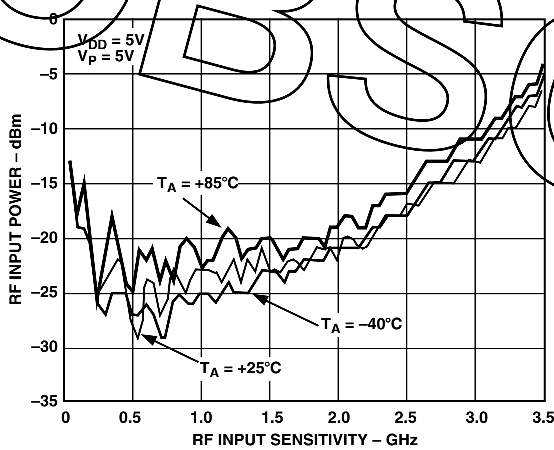
–Typical Performance Characteristics

FREQ-UNIT	PARAM-TYPE	DATA-FORMAT	KEYWORD	IMPEDANCE – OHMS	
GHz	S	MA	R	50	
FREQ	**MAGS11**	**ANGS11**	**FREQ**	**MAGS11**	**ANGS11**
0.0	0.957111193	–3.130429321	1.35	0.816886959	–51.80711782
0.15	0.963546793	–6.686426265	1.45	0.825983016	–56.20373378
0.25	0.953621785	–11.19913586	1.55	0.791737125	–61.21554647
0.35	0.953757706	–15.35637483	1.65	0.770543186	–61.88187496
0.45	0.929831379	–20.3793432	1.75	0.793897072	–65.39516615
0.55	0.908459709	–22.69144845	1.85	0.745765233	–69.24884474
0.65	0.897303634	–27.07001443	1.95	0.7517547	–71.21608147
0.75	0.876862863	–31.32240763	2.05	0.745594889	–75.93169947
0.85	0.849338092	–33.68058163	2.15	0.713387801	–78.8391674
0.95	0.858403269	–38.57674885	2.25	0.711578577	–81.71934806
1.05	0.841888714	–41.48606772	2.35	0.698487131	–85.49067481
1.15	0.840354983	–45.97597958	2.45	0.669871818	–88.41958754
1.25	0.822165839	–49.19163116	2.55	0.668353367	–91.70921678

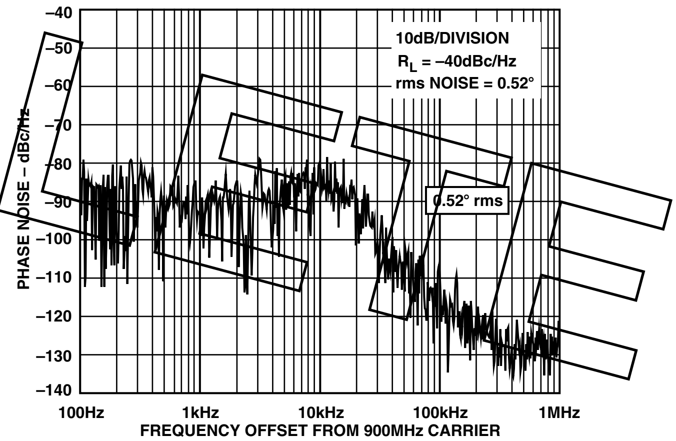
TPC 1. S-Parameter Data for the AD4208 RF1 Input (Up to 2.5 GHz)



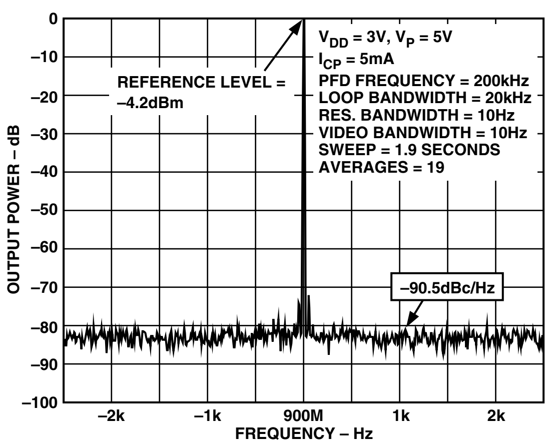
TPC 4. ADF4208 RF1 Reference Spurs (900 MHz, 200 kHz, 20 kHz)



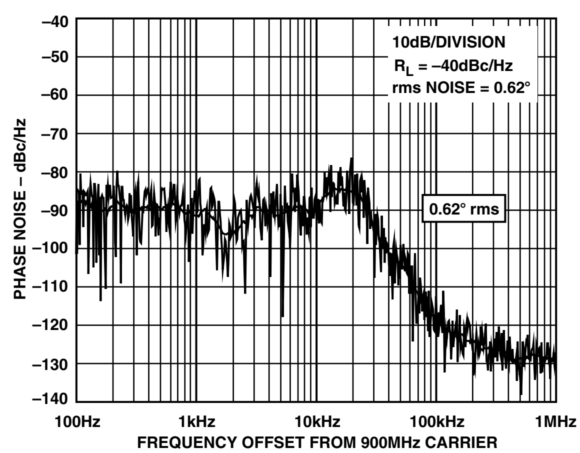
TPC 2. Input Sensitivity for the ADF4208 (RF1)



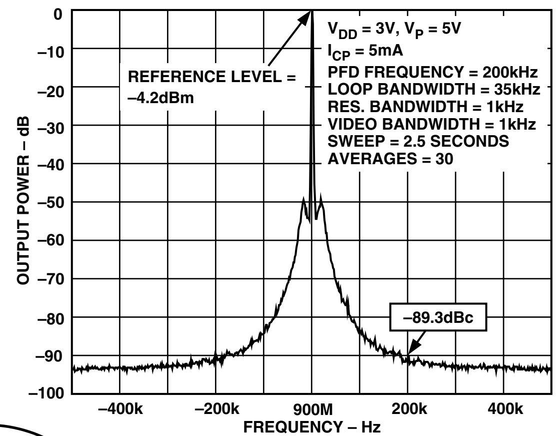
TPC 5. ADF4208 RF1 Integrated Phase Noise (900 MHz, 200 kHz, 20 kHz)



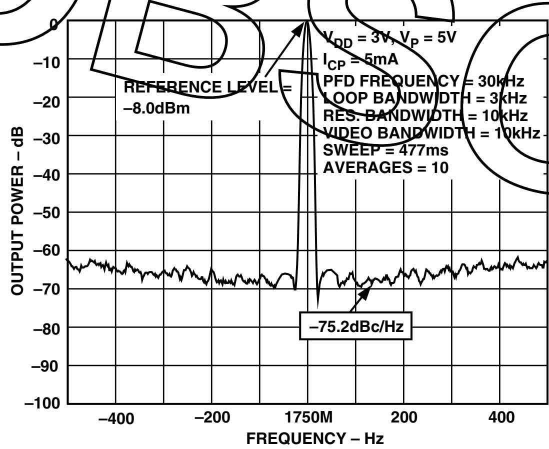
TPC 3. ADF4208 RF1 Phase Noise (900 MHz, 200 kHz, 20 kHz)



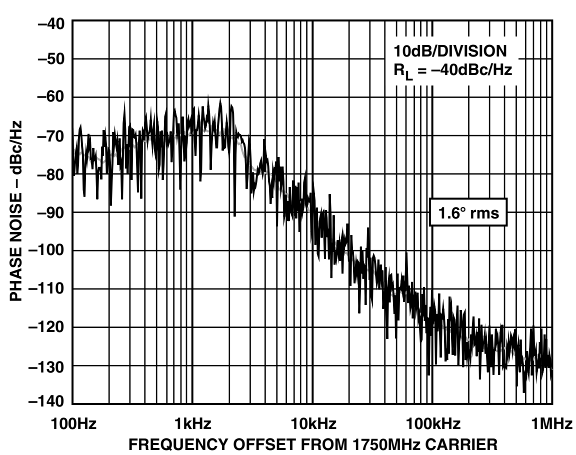
TPC 6. ADF4208 RF1 Integrated Phase Noise (900 MHz, 200 kHz, 35 kHz)



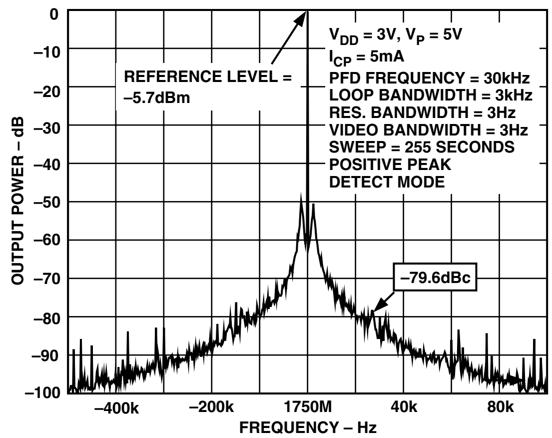
TPC 7. ADF4208 RF1 Reference Spurs (900 MHz, 200 kHz, 35 kHz)



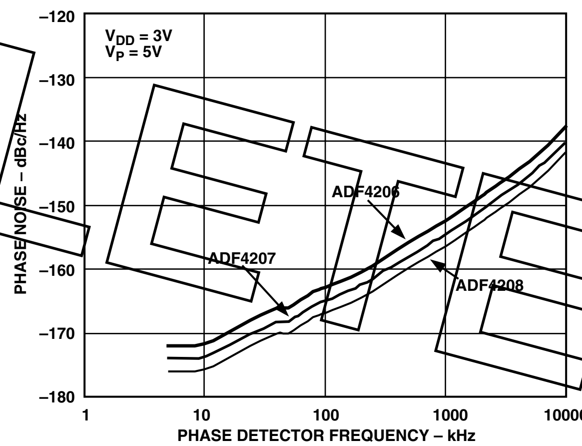
TPC 8. ADF4208 RF1 Phase Noise (1750 MHz, 30 kHz, 3 kHz)



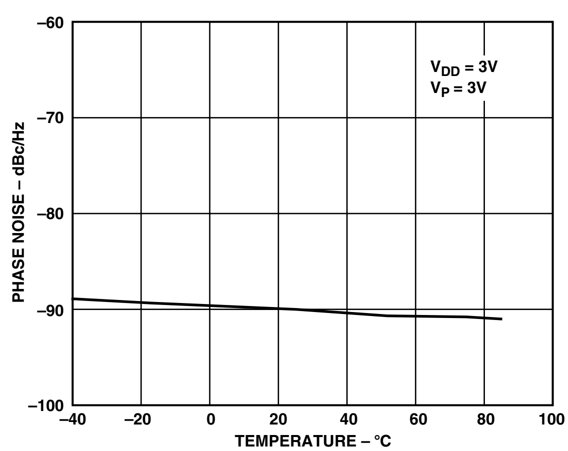
TPC 9. ADF4208 RF1 Integrated Phase Noise (1750 MHz, 30 kHz, 3 kHz)



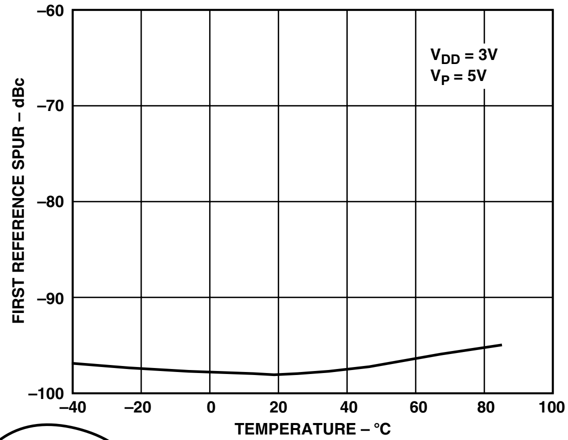
TPC 10. ADF4208 RF1 Reference Spurs (1750 MHz, 30 kHz, 3 kHz)



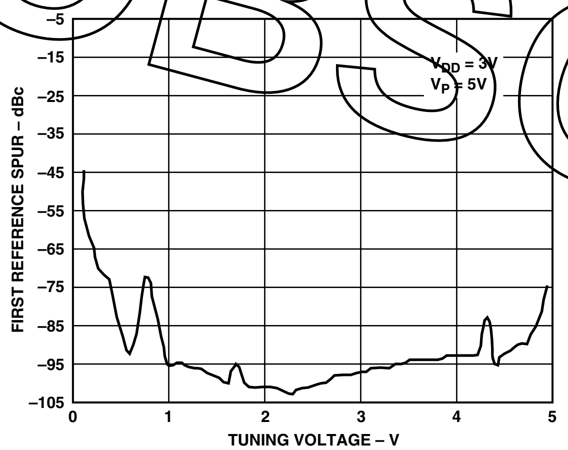
TPC 11. ADF4208 RF1 Phase Noise vs. PFD Frequency



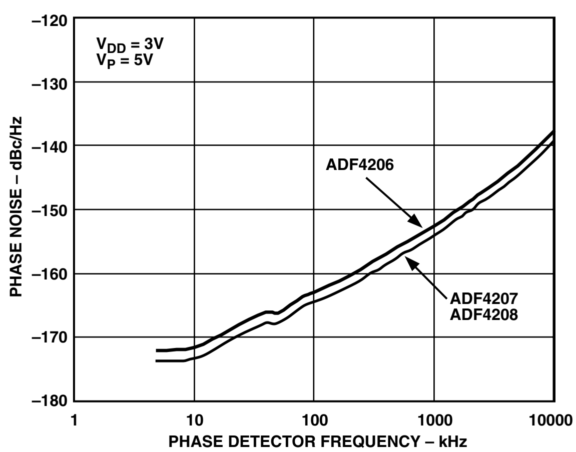
TPC 12. ADF4208 RF1 Phase Noise vs. Temperature (900 MHz, 200 kHz, 20 kHz)



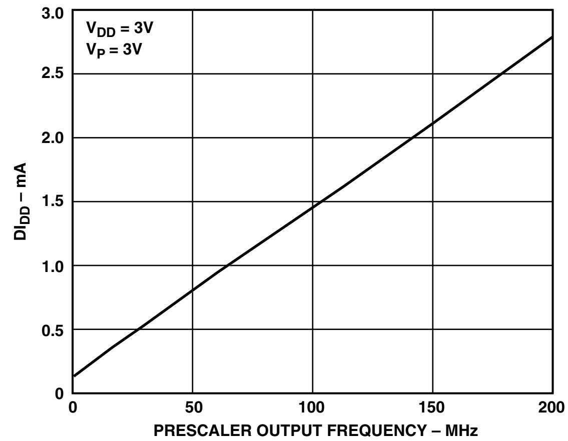
TPC 13. ADF4208 RF1 Reference Spurs vs. Temperature (900 MHz, 200 kHz, 20 kHz)



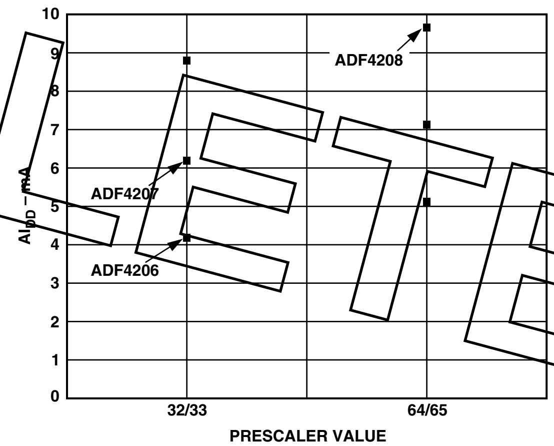
TPC 14. ADF4208 RF1 Reference Spurs vs. V_{TUNE} (900 MHz, 200 kHz, 20 kHz)



TPC 15. ADF4208 RF2 Phase Noise vs. PFD Frequency



TPC 16 DI_{DD} vs. Prescaler Output Frequency (All Models, RF1 and RF2)



TPC 17. ADF4206/ADF4207/ADF4208 AI_{DD} vs. Prescaler Value (RFI)

OBSOLETE

CIRCUIT DESCRIPTION

REFERENCE INPUT SECTION

The reference input stage is shown in Figure 2. SW1 and SW2 are normally closed switches. SW3 is normally open. When power-down is initiated, SW3 is closed and SW1 and SW2 are opened. Typical recommended external components are shown in Figure 2.

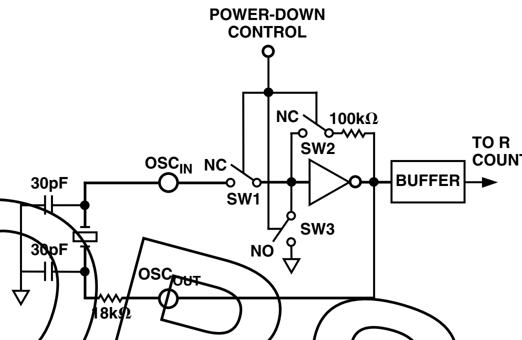


Figure 2. RF Input Stage

RF INPUT STAGE

The RF input stage is shown in Figure 3. It is followed by a 2-stage limiting amplifier to generate the CML clock levels needed for the prescaler.

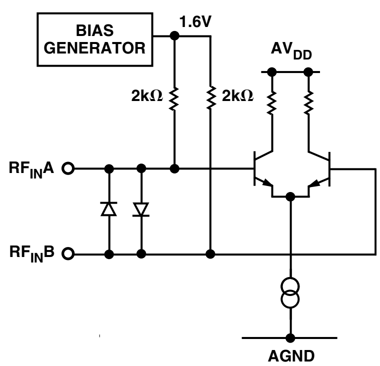


Figure 3. RF Input Stage

PRESCALER

The dual modulus prescaler (P/P + 1), along with the A and B counters, enables the large division ratio, N, to be realized (N = BP + A). This prescaler, operating at CML levels, takes the clock from the RF input stage and divides it down to a manageable frequency for the CMOS A and B counters. It is based on a synchronous 4/5 core.

The prescaler is selectable. Both RF1 and RF2 can be set to either 32/33 or 64/65. DB20 of the AB counter latch selects the value. See Tables IV and VI.

A AND B COUNTERS

The A and B CMOS counters combine with the dual modulus prescaler to allow a wide ranging division ratio in the PLL feedback counter. The devices are guaranteed to work when the prescaler output is 200 MHz or less.

Pulse Swallow Function

The A and B counters, in conjunction with the dual modulus prescaler, make it possible to generate output frequencies that are spaced only by the Reference Frequency divided by R. The equation for the VCO frequency is as follows:

$$f_{VCO} = [(P \times B) + A] \times f_{REFIN}/R$$

f_{VCO} = Output frequency of external voltage controlled oscillator (VCO).

P = Preset modulus of dual modulus prescaler (32/33, 64/65).

B = Preset Divide Ratio of binary 11-bit counter (1 to 2047).

A = Preset Divide Ratio of binary 6-bit A counter (0 to 63).

f_{REFIN} = Output frequency of the external reference frequency oscillator.

R = Preset divide ratio of binary 14-bit programmable reference counter (1 to 16383).

R COUNTER

The 14-bit R counter allows the input reference frequency to be divided down to produce the reference clock to the phase frequency detector (PFD). Division ratios from 1 to 16,383 are allowed.

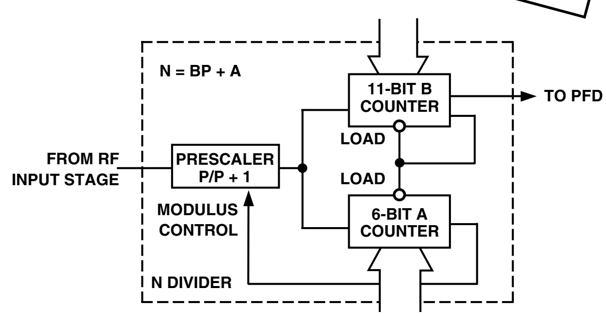


Figure 4. A and B Counters

PHASE FREQUENCY DETECTOR (PFD) AND CHARGE PUMP

The PFD takes inputs from the R counter and N counter (N = BP + A) and produces an output proportional to the phase and frequency difference between them. Figure 5 is a simplified schematic.

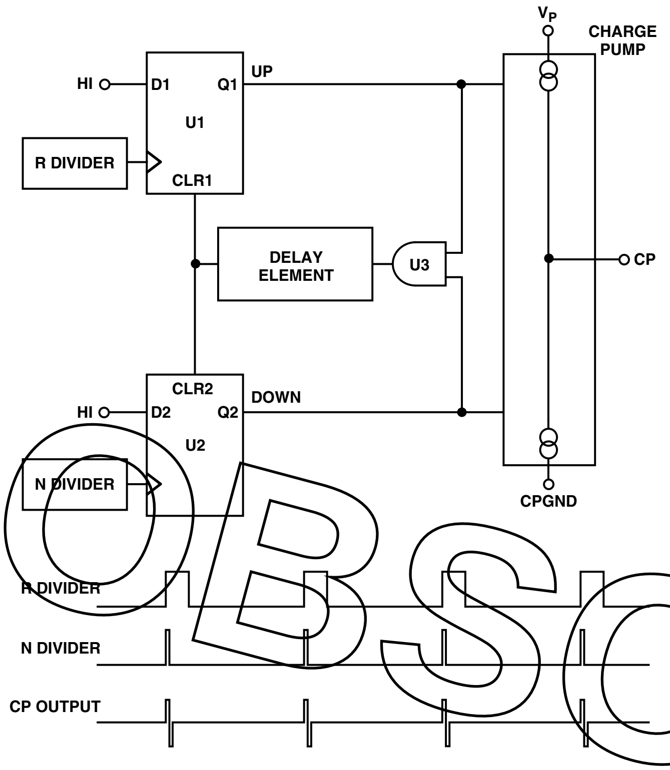


Figure 5. PFD Simplified Schematic and Timing (In Lock)

The PFD includes a delay element which sets the width of the antibacklash phase. The typical value for this is in the ADF4206 family is 3 ns. The pulse ensures that there is no deadzone in the PFD transfer function and minimizes phase noise and reference spurs.

MUXOUT AND LOCK DETECT

The output multiplexer on the ADF4206 family allows the user to access various internal points on the chip. The state of MUXOUT is controlled by P3, P4, P11, and P12. See Tables III and V. Figure 6 shows the MUXOUT section in block diagram form.

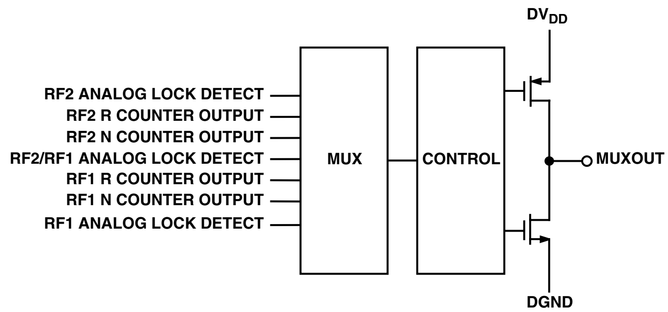


Figure 6. MUXOUT Circuit

Lock Detect

MUXOUT can be programmed for analog lock detect. The N-channel open-drain analog lock detect should be operated with an external pull-up resistor of 10 kΩ nominal. When lock has been detected it is high with narrow low-going pulses.

INPUT SHIFT REGISTER

The functional block diagram for the ADF4206 family is shown on Page 1. The main blocks include a 22-bit input shift register, a 14-bit R counter, and an 17-bit N counter, comprising a 6-bit A counter and an 11-bit B counter. Data is clocked into the 22-bit shift register on each rising edge of CLK. The data is clocked in MSB first. Data is transferred from the shift register to one of four latches on the rising edge of LE. The destination latch is determined by the state of the two control bits (C2, C1) in the shift register. These are the two LSBs DB1, DB0, as shown in the timing diagram of Figure 1. The truth table for these bits is shown in Table I.

Table I. C2, C1 Truth Table

Control Bits C2	C1	Data Latch
0	0	RF2 R Counter
0	1	RF2 AB Counter (and Prescaler Select)
1	0	RF1 R Counter
1	1	RF1 AB Counter (and Prescaler Select)

Table II. ADF4206 Family Latch Summary

RF2 REFERENCE COUNTER LATCH

RF2 F_O	RF2 LOCK DETECT	THREE-STATE CP_{RF2}	RF2 CP GAIN	RF2 PD POLARITY	NOT USED	14-BIT REFERENCE COUNTER, R														CONTROL BITS	
DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P4	P3	P2	P5	P1		R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	C2 (0)	C1 (0)

RF2 AB COUNTER LATCH

RF2 POWER-DOWN	RF2 PRESCALER	11-BIT B COUNTER											NOT USED	6-BIT A COUNTER						CONTROL BITS	
DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P7	P6	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1		A6	A5	A4	A3	A2	A1	C2 (0)	C1 (0)

RF1 REFERENCE COUNTER LATCH

RF1 F_O	RF1 LOCK DETECT	THREE-STATE CP_{RF1}	RF1 CP GAIN	RF1 PD POLARITY	NOT USED	14-BIT REFERENCE COUNTER, R														CONTROL BITS	
DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P12	P11	P10	P13	P9		R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	C2 (1)	C1 (0)

RF1 AB COUNTER LATCH

RF1 POWER-DOWN	RF1 PRESCALER	11-BIT B COUNTER											NOT USED	6-BIT A COUNTER						CONTROL BITS	
DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P16	P14	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1		A6	A5	A4	A3	A2	A1	C2 (1)	C1 (1)

Table III. RF2 Reference Counter Latch Map

RF2 REFERENCE COUNTER LATCH

RF2 F_O	RF2 LOCK DETECT	THREE-STATE CP_{RF2}	RF2 CP GAIN	RF2 PD POLARITY		14-BIT REFERENCE COUNTER, R														CONTROL BITS	
DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P4	P3	P2	P5	P1		R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	C2 (0)	C1 (0)

R14	R13	R12	....	R3	R2	R1	DIVIDE RATIO
0	0	0	....	0	0	1	1
0	0	0	....	0	1	0	2
0	0	0	....	0	1	1	3
0	0	0	....	1	0	0	4
.	.	.	....	.	.	.	.
.	.	.	....	.	.	.	.
.	.	.	....	.	.	.	.
1	1	1	....	1	0	0	16380
1	1	1	....	1	0	1	16381
1	1	1	....	1	1	0	16382
1	1	1	....	1	1	1	16383

P1	PD POLARITY
0	NEGATIVE
1	POSITIVE

P5	I_{CP}
0	1.25 mA
1	4.375 mA

P2	CHARGE PUMP OUTPUT
0	NORMAL
1	THREE-STATE

P12 FROM RF1 R LATCH	P11	P4	P3	MUXOUT
0	0	0	0	LOGIC LOW STATE
0	0	0	1	RF2 ANALOG LOCK DETECT
0	X	1	0	RF2 REFERENCE DIVIDER OUTPUT
0	X	1	1	RF2 N DIVIDER OUTPUT
0	1	0	0	RF1 ANALOG LOCK DETECT
0	1	0	1	RF1/RF2 ANALOG LOCK DETECT
1	X	0	0	RF1 REFERENCE DIVIDER
1	X	0	1	RF1 N DIVIDER
1	0	1	0	FAST LOCK OUTPUT SWITCH ON AND CONNECTED TO MUXOUT
1	0	1	1	RF2 COUNTER RESET
1	1	1	0	RF1 COUNTER RESET
1	1	1	1	RF2 AND RF1 COUNTER RESET

Table IV. RF2 AB Counter Latch Map

RF2 AB COUNTER LATCH

RF2 POWER-DOWN	RF2 PRESCALER	11-BIT B COUNTER												6-BIT A COUNTER						CONTROL BITS	
DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P7	P6	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1		A6	A5	A4	A3	A2	A1	C2 (0)	C1 (1)

A6	A5	A4	A3	A2	A1	A COUNTER DIVIDE RATIO
X	X	0	0	0	0	0
X	X	0	0	0	1	1
X	X	0	0	1	0	2
X	X	0	0	1	1	3
.	.	.	.	.	.	
.	.	.	.	.	.	
.	.	.	.	.	.	
X	X	1	1	1	0	14
X	X	1	1	1	1	15

B11	B10	B9		B3	B2	B1	B COUNTER DIVIDE RATIO
0	0	0	....	0	0	0	NOT ALLOWED
0	0	0	....	0	0	1	NOT ALLOWED
0	0	0	....	0	1	0	NOT ALLOWED
0	0	0	....	0	1	1	3
.	.	.	....	.	.	.	.
.	.	.	....	.	.	.	.
.	.	.	....	.	.	.	.
1	1	1	....	1	0	0	2044
1	1	1	....	1	0	1	2045
1	1	1	....	1	1	0	2046
1	1	1	....	1	1	1	2047

P6	RF2 PRESCALER
0	64/65
1	32/33

P7	RF2 SECTION
0	NORMAL OPERATION
1	POWER-DOWN

N = BP + A, P IS PRESCALER VALUE SET BY P6. B MUST BE GREATER THAN OR EQUAL TO A. TO ENSURE CONTINUOUSLY ADJACENT VALUES OF Nx F_{REF}, N_{MIN} IS $(P^2 - P)$.

Table V. RF1 Reference Counter Latch Map

RF1 REFERENCE COUNTER LATCH

RF1 F_O	RF1 LOCK DETECT	THREE-STATE CP_{RF1}	RF1 CP GAIN	RF1 PD POLARITY		14-BIT REFERENCE COUNTER, R														CONTROL BITS	
DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P12	P11	P10	P13	P9		R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	C2 (1)	C1 (0)

R14	R13	R12	....	R3	R2	R1	DIVIDE RATIO
0	0	0	....	0	0	1	1
0	0	0	....	0	1	0	2
0	0	0	....	0	1	1	3
0	0	0	....	1	0	0	4
.	.	.	....	.	.	.	.
.	.	.	....	.	.	.	.
.	.	.	....	.	.	.	.
1	1	1	....	1	0	0	16380
1	1	1	....	1	0	1	16381
1	1	1	....	1	1	0	16382
1	1	1	....	1	1	1	16383

P9	PD POLARITY
0	NEGATIVE
1	POSITIVE

P13	I_{CP}
0	1.25 mA
1	4.375 mA

P10	CHARGE PUMP OUTPUT
0	NORMAL
1	THREE-STATE

P12	P11	P4 (FROM RF2 R LATCH)	P3 (FROM RF2 R LATCH)	MUXOUT
0	0	0	0	LOGIC LOW STATE
0	0	0	1	RF2 ANALOG LOCK DETECT
0	X	1	0	RF2 REFERENCE DIVIDER OUTPUT
0	X	1	1	RF2 N DIVIDER OUTPUT
0	1	0	0	RF1 ANALOG LOCK DETECT
0	1	0	1	RF1/RF2 ANALOG LOCK DETECT
1	X	0	0	RF1 REFERENCE DIVIDER
1	X	0	1	RF1 N DIVIDER
1	0	1	0	FAST LOCK OUTPUT SWITCH ON AND CONNECTED TO MUXOUT
1	0	1	1	RF2 COUNTER RESET
1	1	1	0	RF1 COUNTER RESET
1	1	1	1	RF2 AND RF1 COUNTER RESET

Table VI. RF1 AB Counter Latch Map

RF1 AB COUNTER LATCH

RF1 POWER-DOWN	RF1 PRESCALER	11-BIT B COUNTER												6-BIT A COUNTER						CONTROL BITS	
DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P16	P14	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1		A6	A5	A4	A3	A2	A1	C2 (1)	C1 (1)

A6	A5	A4	A3	A2	A1	A COUNTER DIVIDE RATIO
0	0	0	0	0	0	0
0	0	0	0	0	1	1
0	0	0	0	1	0	2
0	0	0	0	1	1	3
.	.	.	.	.	.	
.	.	.	.	.	.	
.	.	.	.	.	.	
1	1	1	1	1	0	62
1	1	1	1	1	1	63

B11	B10	B9		B3	B2	B1	B COUNTER DIVIDE RATIO
0	0	0	....	0	0	1	1
0	0	0	....	0	1	0	2
0	0	0	....	0	1	1	3
0	0	0	....	1	0	0	3
.	.	.	....	.	.	.	.
.	.	.	....	.	.	.	.
.	.	.	....	.	.	.	.
1	1	1	....	1	0	0	2044
1	1	1	....	1	0	1	2045
1	1	1	....	1	1	0	2046
1	1	1	....	1	1	1	2047

P14	RF1 PRESCALER
0	64/65
1	32/33

P16	RF1 SECTION
0	NORMAL OPERATION
1	POWER-DOWN

N = BP + A, P IS PRESCALER VALUE SET BY P6. B MUST BE GREATER THAN OR EQUAL TO A. FOR CONTINUOUSLY ADJACENT VALUES OF N, N_{MIN} IS $(P^2 – P)$.

PROGRAM MODES

Table III and Table V show how to set up the Program Modes in the ADF420x family. The following should be noted:

1. RF2 and RF1 Analog Lock Detect indicate when the PLL is in lock. When the loop is locked and either RF2 or RF1 Analog Lock Detect is selected, the MUXOUT pin will show a logic high with narrow low-going pulses. When the RF2/RF1 Analog Lock Detect is chosen, the locked condition is indicated only when both RF2 and RF1 loops are locked.
2. The RF2 Counter Reset mode resets the R and AB counters in the RF2 section and also puts the RF2 charge pump into three-state. The RF1 Counter Reset mode resets the R and AB counters in the RF1 section and also puts the RF1 charge pump into three-state. The RF2 and RF1 Counter Reset mode does both of the above.

   Upon removal of the reset bits, the AB counter resumes counting in close alignment with the R counter (maximum error is one prescaler output cycle).
3. The Fastlock mode uses MUXOUT to switch a second loop filter damping resistor to ground during Fastlock operation. Activation of Fastlock occurs whenever RF1 CP Gain in the RF1 Reference counter is set to one.

POWER-DOWN

It is possible to program the ADF420x family for either synchronous or asynchronous power-down on either the RF2 or RF1 side.

Synchronous RF2 Power-Down

Programming a "1" to P7 of the ADF420x family will initiate a power-down. If P2 of the ADF420x family has been set to "0" (normal operation), a synchronous power-down is conducted. The device will automatically put the charge pump into three-state and then complete the power-down.

Asynchronous RF2 Power-Down

If P2 of the ADF420x family has been set to "1" (three-state the RF2 charge pump), and P7 is subsequently set to "1," an asynchronous power-down is conducted. The device will go into power-down on the rising edge of LE, which latches the "1" to the RF2 power-down bit (P7).

Synchronous RF1 Power-Down

Programming a "1" to P16 of the ADF420x family will initiate a power-down. If P10 of the ADF420x family has been set to "0" (normal operation), a synchronous power-down is conducted. The device will automatically put the charge pump into three-state and then complete the power-down.

Asynchronous RF1 Power-Down

If P10 of the ADF420x family has been set to "1" (three-state the RF1 charge pump), and P16 is subsequently set to "1," an asynchronous power-down is conducted. The device will go into power-down on the rising edge of LE, which latches the "1" to the RF1 power-down bit (P16).

Activation of either synchronous or asynchronous power-down forces the RF2/RF1 loop's R and N dividers to their load state conditions and the RF2/RF1 input section is debiased to a high impedance state.

The reference oscillator circuit is only disabled if both the RF2 and RF1 power-downs are set.

The input register and latches remain active and are capable of loading and latching data during all the power-down modes.

The RF2/RF1 section of the devices will return to normal powered up operation immediately upon LE latching a "0" to the appropriate power-down bit.

IF SECTION (RF2)

Programmable RF2 Reference (R) Counter

If control bits (C2, C1) are (0, 0), the data is transferred from the input shift register to the 14-bit RF2 R counter. Table III shows the input shift register data format for the RF2 R counter and the divide ratios possible.

RF2 Phase Detector Polarity

P1 sets the RF2 Phase Detector Polarity. When the RF2 VCO characteristics are positive, this should be set to "1." When they are negative, it should be set to "0." See Table III.

RF2 Charge Pump Three-State

P2 puts the RF2 charge pump into three-state mode when programmed to a "1." It should be set to "0" for normal operation. See Table III.

RF2 Program Modes

Table III and Table V show how to set up the Program Modes in the ADF420x family.

RF2 Charge Pump Currents

Bit P5 programs the current setting for the RF2 charge pump. See Table III.

Programmable RF2 AB Counter

If control bits (C2, C1) are (0, 1), the data in the input register is used to program the RF2 AB counter. The AB counter consists of a 6-bit swallow counter (A counter) and 11-bit programmable counter (B counter). Table IV shows the input register data format for programming the RF2 AB counter and the divide ratios possible.

RF2 Prescaler Value

P6 in the RF2 AB counter latch sets the RF2 prescaler value. See Table IV.

RF2 Power-Down

P7 in Table IV is the power-down bit for the RF2 side.

RF SECTION (RF1)

Programmable RF1 Reference (R) Counter

If control bits (C2, C1) are (1, 0), the data is transferred from the input shift register to the 14 Bit RF1 R counter. Table V shows the input shift register data format for the RF1 R counter and the divide ratios possible.

RF1 Phase Detector Polarity

P9 sets the RF1 Phase Detector Polarity. When the RF1 VCO characteristics are positive this should be set to "1." When they are negative it should be set to "0." See Table V.

RF1 Charge Pump Three-State

P10 puts the RF1 charge pump into three-state mode when programmed to a "1." It should be set to "0" for normal operation. See Table V.

RF1 Program Modes

Table III and Table V show how to set up the Program Modes in the ADF420x family.

RF1 Charge Pump Currents

Replaced with a P13 programs the current setting for the RF1 charge pump. See Table V.

Programmable RF1 AB Counter

If control bits (C2, C1) are (1, 1), then the data in the input register is used to program the RF1 AB counter. The AB counter consists of a 6-bit swallow counter (A counter) and 11-bit programmable counter (B counter). Table VI shows the input register data format for programming the RF1 AB counter and the divide ratios possible. See Table VI.

RF1 Prescaler Value

P14 in the RF1 A, B counter latch set the RF1 prescaler value. See Table VI.

RF1 Power-Down

Setting P16 in the RF1 AB counter high powers down RF1 side.

RF Fastlock

The fastlock feature can improve the lock time of the PLL. It increases charge pump current to a maximum for a period of time. Fastlock of the ADF420x family is activated by setting P13 in the reference counter high and setting the fastlock switch on using MUXOUT. Switching in an external resistor using MUXOUT compensates the loop dynamics for the effect of increasing charge pump current. Setting P13 low removes the PLL from fastlock mode.

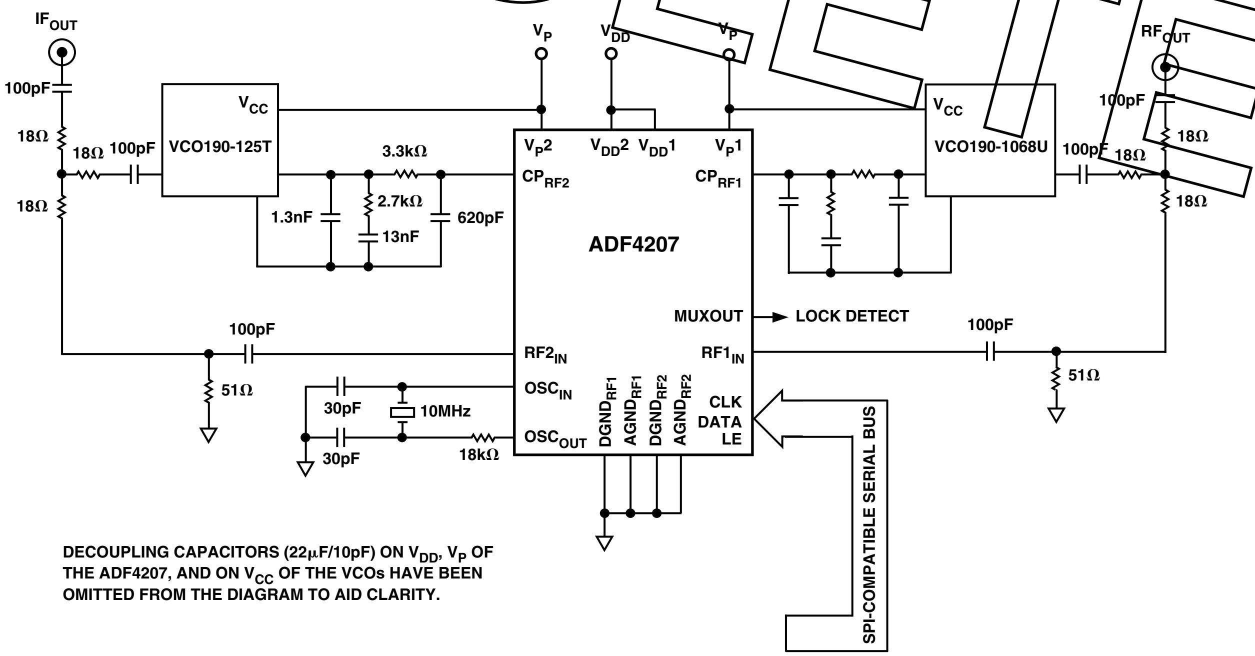


Figure 7. GSM Handset Receiver Local Oscillator Using the ADF4207

APPLICATIONS SECTION

Local Oscillator for GSM Handset Receiver

Figure 7 shows the ADF4207 being used in a classic superheterodyne receiver to provide the required LOs (Local Oscillators).

In this circuit, the reference input signal is applied to the circuit at OSC_{IN} and is being generated by a 10 MHz Crystal Oscillator. This is a low-cost solution and for better performance over temperature, a TCXO (Temperature Controlled Crystal Oscillator) may be used instead.

In order to have a channel spacing of 200 kHz (the GSM standard), the reference input must be divided by 50, using the on-chip reference counter.

The RF output frequency range is 1050 MHz to 1086 MHz. Loop filter component values are chosen so that the loop bandwidth is 20 kHz. The synthesizer is set up for a charge pump current of 4.375 mA and the VCO sensitivity is 15.6 MHz/V.

The IF output is fixed at 125 MHz. The IF loop bandwidth is chosen to be 20 kHz with a channel spacing of 200 kHz. Loop filter component values are chosen accordingly.

Local Oscillator for WCDMA Receiver

Figure 8 shows the ADF4208 being used to generate the local oscillator frequencies for a Wideband CDMA (WCDMA) system.

The RF output range needed is 1720 MHz to 1780 MHz. The VCO190–1750T will accomplish this. Channel spacing is 200 kHz with a 20 kHz loop bandwidth. VCO sensitivity is 32 MHz/V. Charge pump current of 4.375 mA is used and the desired phase margin for the loop is 45°.

The IF output is fixed at 200 MHz. The VCO190–200T is used. It has a sensitivity of 10 MHz/V. Channel spacing and loop bandwidth is chosen to be the same as the RF side.

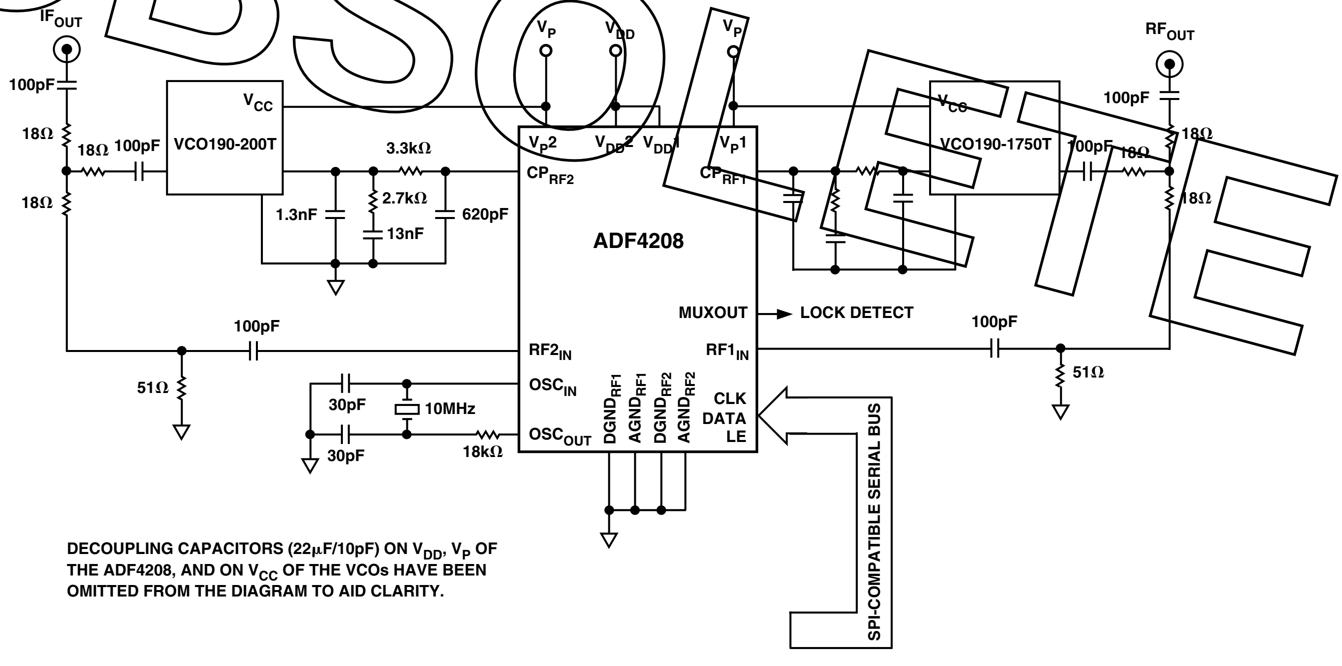


Figure 8. Local Oscillator for WCDMA Receiver Using the ADF4208

INTERFACING

The ADF4206/ADF4207/ADF4208 family has a simple SPI-compatible serial interface for writing to the device. SCLK, SDATA, and LE (Latch Enable) control the data transfer. When LE goes high, the 22 bits that have been clocked into the input register on each rising edge of SCLK will be transferred to the appropriate latch. See Figure 1 for the Timing Diagram and Table I for the Latch Truth Table.

The maximum allowable serial clock rate is 20 MHz. This means that the maximum update rate possible for the device is 909 kHz or one update every 1.1 ms. This is certainly more than adequate for systems that will have typical lock times in hundreds of microseconds.

ADuC812 Interface

Figure 10 shows the interface between the ADF420x family and the ADuC812 microconverter. Since the ADuC812 is based on an 8051 core, this interface can be used with any 8051-based microcontroller. The microconverter is set up for SPI Master Mode with CPHA = 0. To initiate the operation, the I/O port driving LE is brought low. Each latch of the ADF420x family needs a 22-bit word. This is accomplished by writing three 8-bit bytes from the microconverter to the device. When the third byte has been written, the LE input should be brought high to complete the transfer.

On first applying power to the ADF420x family, it requires four writes (one each to the R counter latch and the AB counter latch for both RF1 and RF2 side) for the output to become active.

When operating in the mode described, the maximum SCLOCK rate of the ADuC812 is 4 MHz. This means that the maximum rate at which the output frequency can be changed will be about 180 kHz.

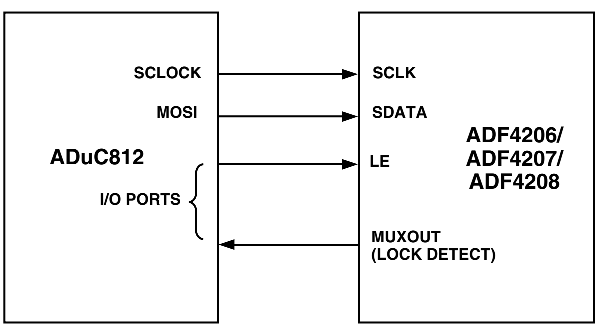


Figure 9. ADuC812 to ADF420x Family Interface

ADSP-2181 Interface

Figure 10 shows the interface between the ADF420x family and the ADSP-21xx Digital Signal Processor. As previously noted, the ADF420x family needs a 22-bit serial word for each latch write. The easiest way to accomplish this using the ADSP21-xx family is to use the Autobuffered Transmit Mode of operation with Alternate Framing. This provides a means for transmitting an entire block of serial data before an interrupt is generated. Set up the word length for eight bits and use three memory locations for each 22-bit word. To program each 22-bit latch, store the three 8-bit bytes, enable the Autobuffered mode and then write to the transmit register of the DSP. This last operation initiates the autobuffer transfer.

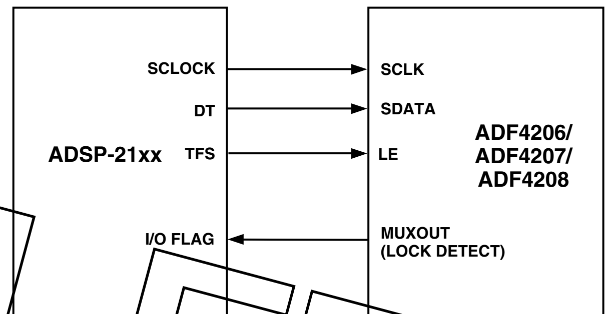
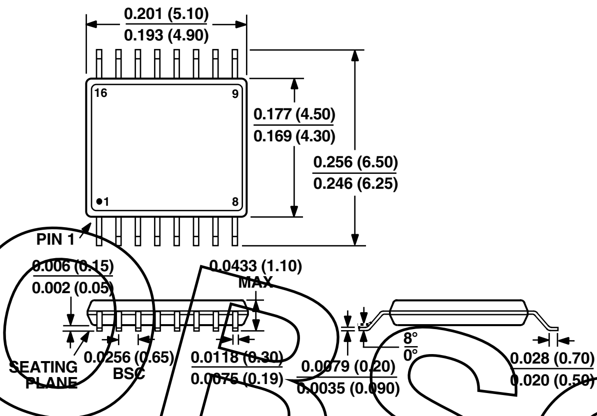


Figure 10. ADSP-21xx to ADF420x Family Interface

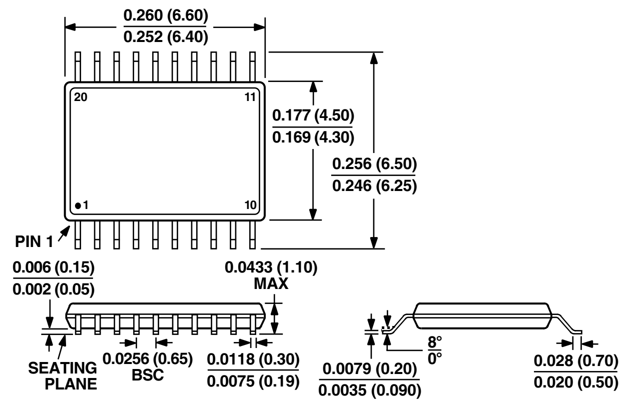
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

Thin Shrink Small Outline Package (TSSOP) (RU-16)



Thin Shrink Small Outline Package (TSSOP) (RU-20)



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