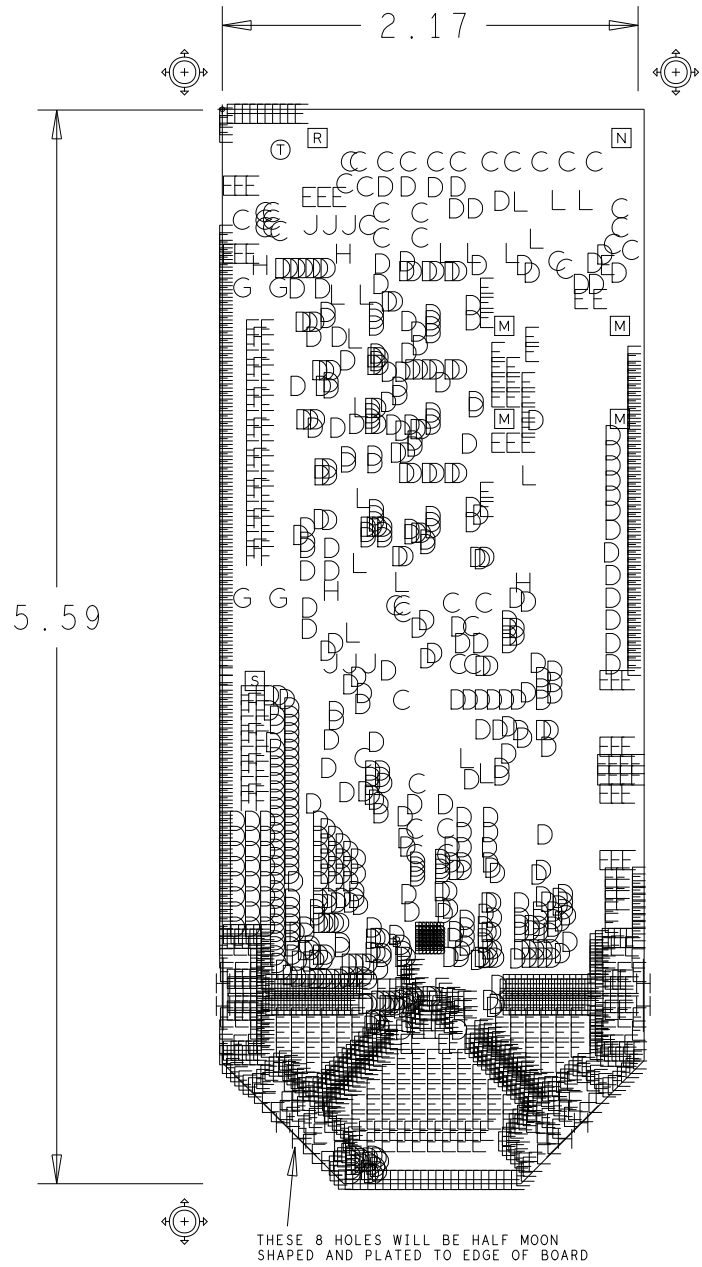


PLATED: +/- .003
HOLE TOLERANCE
UNLESS SPECIFIED
NON PLATED: +/- .001



DRILL CHART: TOP to BOTTOM			
ALL UNITS ARE IN MILLIMETERS			
FIGURE	SIZE	PLATED	QTY
B	0.2032	PLATED	51
C	0.254	PLATED	47
D	0.254	PLATED	561
E	0.4064	PLATED	950
F	0.7874	PLATED	60
G	0.889	PLATED	4
H	0.9906	PLATED	12
J	1.016	PLATED	6
L	1.6002	PLATED	18
M	1.905	PLATED	4
	2.1082	PLATED	8
N	0.7112	NON-PLATED	1
R	1.0922	NON-PLATED	1
S	1.1938	NON-PLATED	1
T	3.175	NON-PLATED	1

4 LAYER STACKUP

	PRIMARY SILKSCREEN
	PRIMARY SOLDER MASK
Cu-Cu THICKNESS 0.058" +/- .003"	LYR 1 - SIG 50ohm(TOP)- [Start Cu=17um, After Plating=53um or 1.5oz]
	8mil ROGERS 4003 LYR 2 - GND Plane - [Cu = 17um]
	CORE FR4 LYR 3 - PWR Plane - [Cu = 17um]
	8mil ROGERS 4003 LYR 4 - SIG (BOT)- [Start Cu=17um, After Plating=53um]
	SECONDARY SOLDER MASK
	SECONDARY SILKSCREEN

CHARACTERISTIC IMPEDANCE ON LAYER 1 :
A.--> 50 OHM SINGLE
ENDED CO-PLANAR WAVEGUIDE (+/-5%).
LINE WIDTH = 0.380 mm
GAP TO GROUND PLANE ON LAYER 1 = 0.2mm EITHER SIDE
OF THE TRACE

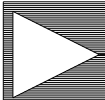
GROUND REFERENCE PLANE ON LAYER 2.

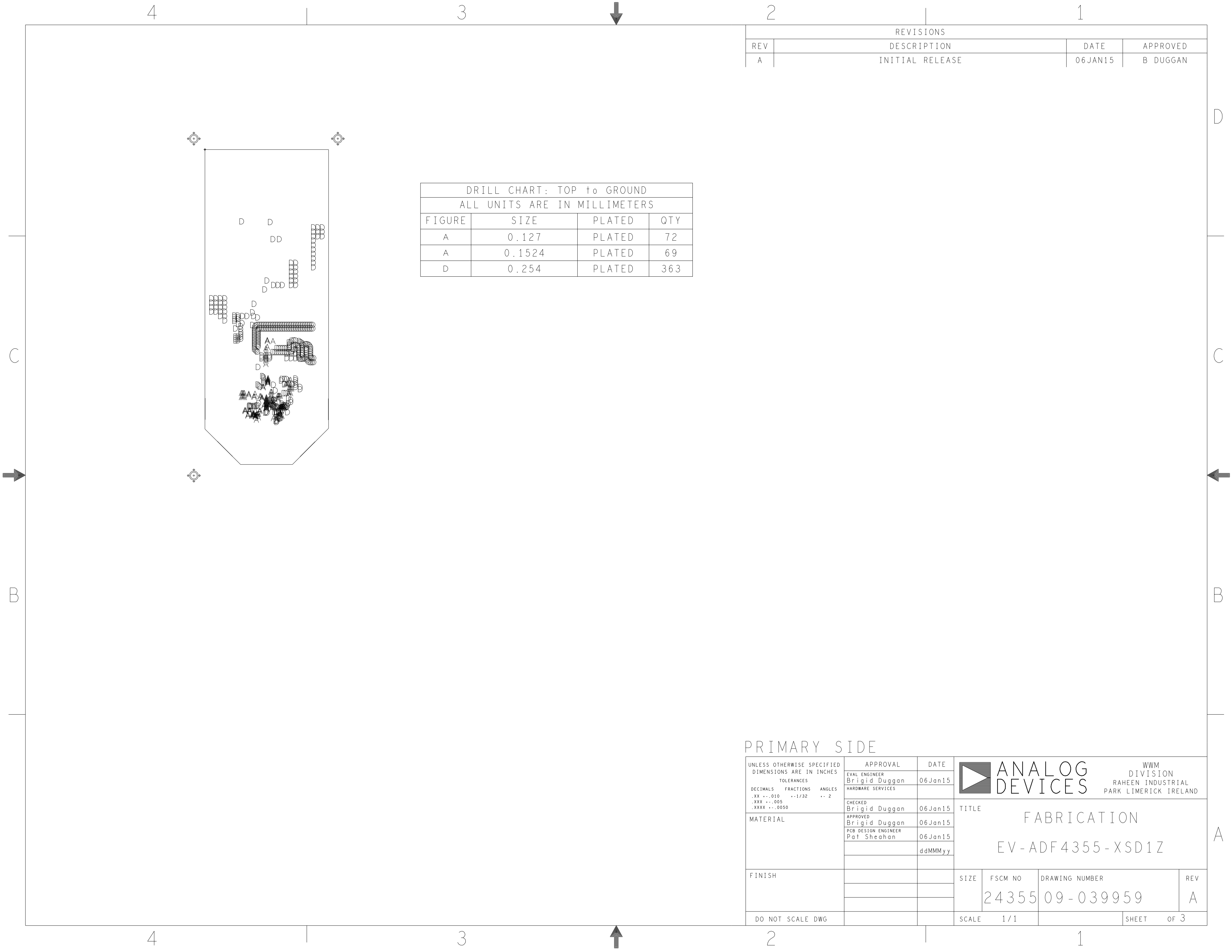
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	INITIAL RELEASE	06JAN15	B DUGGAN

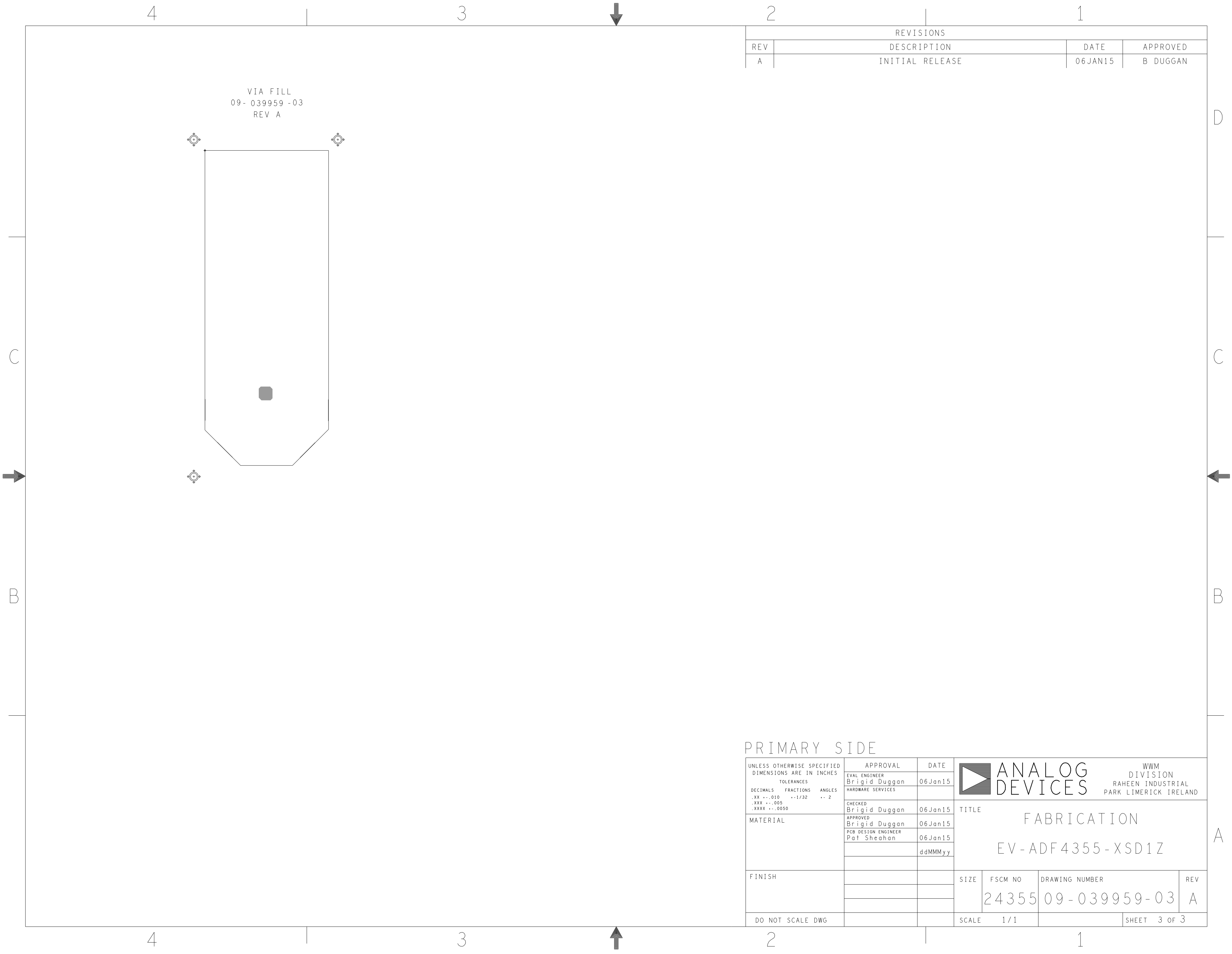
- NOTES:
- ACCEPTABILITY; PER ANALOG DEVICES, INC. SPECIFICATION TST00115 LATEST REVISION.
 - MATERIALS; ROGERS 4003(8 MILS) AND RF4 COMPOSITE FOR RF BUILD. SEE LAYER STACK-UP FOR MORE DETAIL.
 - BONDING AGENT; PREIMPREGNATED B STAGE EPOXY GLASS CLOTH IN ACCORDANCE WITH IPC-L-109 (LATEST REV.).
 - CLADDING; EXTERNAL LAYERS 1/2 OZ. AFTER PLATING 53UM TOTAL. INTERNAL SIGNAL LAYERS 0.5 OZ COPPER. INTERNAL PLANE LAYERS 0.5 OZ COPPER.
 - SOLDER MASK; SHALL BE LIQUID PHOTOIMAGABLE (LPI) APPLIED ON BOTH SIDES OVER BARE COPPER AND SHALL MEET IPC-SM-840 (LATEST REV.) CLASS 3.
 - SILK SCREEN; SHALL BE PERMANENT NON-CONDUCTIVE EPOXY INK, COLOR WHITE.
 - U.L. RATING; 94VO MINIMUM.

- FABRICATION:
- REFER TO IPC-6010 SERIES (LATEST REV.), CLASS 2 FOR FABRICATION UNLESS OTHERWISE SPECIFIED.
 - UNDIMENSIONED HOLES TO BE LOCATED WITHIN +/- .005 OF THEIR TRUE POSITION WITH RESPECT TO ARTWORK.
 - PLATED HOLE WALL THICKNESS SHALL NOT BE LESS THAN .001 INCH MINIMUM AVERAGE, WITH NO READING LESS THAN .0008 BY CROSS SECTION.
 - HOLE DIAMETERS APPLY AFTER PLATING.
 - FINISHED CONDUCTOR WIDTHS SHALL NOT BE REDUCED FROM THE NOMINAL, INDICATED ON THE MASTER PATTERN, BY MORE THAN THE CONDUCTOR THICKNESS.
 - MINIMUM DESIGN LINE WIDTH IS .008 INCH.
 - MINIMUM DESIGN SPACING IS .008 INCH.
 - BOARD/PANEL MUST MEET IPC-A-600 (LATEST REV.) CLASS 2 FOR FLATNESS.
 - MFGR. TO LEGIBLY ETCH OR STAMP/SCREEN WITH PERMANENT NON-CONDUCTIVE INK ON SECONDARY SIDE IN A CLEAR AREA UNLESS OTHERWISE INDICATED;
A. U.L. CODE D. MFGR. LOGO - DESIGNATED AREA,
B. DATE CODE (STAMP) E. SUCCESSFUL ELECTRICAL BOARD TEST.
C. FLAMMABILITY RATING F. LOT NUMBER - DESIGNATED AREA.
 - NON-FUNCTIONAL PADS MAY BE REMOVED FROM INNER SIGNAL LAYERS AT MFGR. DISCRETION.
 - IF PAD SIZES PROVIDED ARE NOT LARGE ENOUGH TO MAINTAIN ANNULAR RING REQUIREMENT, MFGR. MAY TEAR DROP PADS TO MAINTAIN ANNULAR RING AT PAD TO CIRCUIT INTERFACE ONLY AND MUST INSURE ELECTRICAL INTEGRITY. REPAIRS PER IPC-R-700 ARE ALLOWED.
 - MODIFICATIONS TO THE ARTWORK, OTHER THAN THOSE DESCRIBED ON THE FABRICATION DRAWING, ARE NOT ALLOWED WITHOUT WRITTEN AUTHORIZATION.
 - SURFACE FINISH TOP AND BOTTOM IS ENIG.
 - FINISHED BOARD MUST BE ROHS & REACH COMPLIANT.
 - THE VIAS IN THE VIA FILL AREA MUST BE FILLED WITH NON-CONDUCTIVE EPOXY, SANDED FLUSH AND PLATED OVER. THE FINISHED PADS MUST BE FLAT AND CO-PLANAR. THIS INCLUDES THE BLIND AND THRU VIAS - REALLY IMPORTANT.
 - THE BLIND VIAS GO FROM LAYER 1 TO LAYER 2.
 - NOTE THE 8 HOLES AT THE EDGE OF THE BOARD THAT WILL BE A HALF MOON AND PLATED.

PRIMARY SIDE

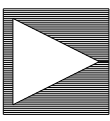
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES DECIMALS FRACTIONS ANGLES .XX --.010 --1/32 -- 2 .XXX --.005 .XXXX --.0050	APPROVAL	DATE	<div></div> <div>ANALOG DEVICES</div> <div>WWM DIVISION RAHEEN INDUSTRIAL PARK LIMERICK IRELAND</div>				
	EVAL ENGINEER Brigid Duggan	06Jan15					
	HARDWARE SERVICES		TITLE FABRICATION EV - ADF4355 - XSD1Z				
	CHECKED Brigid Duggan	06Jan15					
	APPROVED Brigid Duggan	06Jan15					
PCB DESIGN ENGINEER Pat Sheahan	06Jan15						
MATERIAL		ddMMMyy	SIZE 24355				
FINISH			DRAWING NUMBER 09 - 039959				
DO NOT SCALE DWG			SCALE	1/1	SHEET 1 OF 3		REV A





REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	INITIAL RELEASE	06 JAN15	B DUGGAN

PRIMARY SIDE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES DECIMALS FRACTIONS ANGLES .XX -.010 --1/32 -- 2 .XXX -.005 .XXXX -.0050	APPROVAL		DATE	<div>ANALOG DEVICES</div> <div>WWM DIVISION RAHEEN INDUSTRIAL PARK LIMERICK IRELAND</div>			
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FINISH				SIZE	FSCM NO	DRAWING NUMBER	REV
					24355	09 - 039959 - 03	A
DO NOT SCALE DWG				SCALE	1 / 1		SHEET 3 OF 3