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Evaluating the ADF5610 Wideband Microwave Synthesizer with Integrated VCO

FEATURES

- Self contained board, including ADF5610 frequency synthesizer with integrated VCO, single-ended, 50 MHz VCXO, PLL jitter clean up circuit, loop filter (4 kHz), USB interface, and voltage regulators
- Windows-based software allows control of synthesizer functions from a PC
- Externally powered by a single 6 V supply

EVALUATION KIT CONTENTS

- EV-ADF5610SD1Z evaluation board

EQUIPMENT NEEDED

- Windows-based PC with USB port for evaluation software
- System demonstration platform, SDP-S
- EVAL-SDP-CS1Z controller board
- Micro USB cable
- Power supply (6 V)
- 50 Ω terminations
- Signal source analyzer

ONLINE RESOURCES

- ADF5610 data sheet
- ADF5610 software, Version 0.1.3 or higher

GENERAL DESCRIPTION

The EV-ADF5610SD1Z evaluates the performance of the ADF5610 frequency synthesizer with integrated VCO for phase-locked loops (PLLs). A photograph of the evaluation board is shown in Figure 1. The evaluation board contains the ADF5610 synthesizer with integrated voltage controlled oscillator (VCO), a low noise, single-ended, 50 MHz voltage controlled crystal oscillator (VCXO) reference, the HMC1031 Integer N PLL, a switch, a jumper, a loop filter, a USB interface, and subminiature Version A (SMA) connectors.

For easy programming of the synthesizer, download the Windows®-based software from the ADF5610 page at ftp://ADF5610_ftp:ZagrJ6Fx@ftp.analog.com. The file transfer program (FTP) user name and password are printed on the label inside the lid of the evaluation board box. The user manual and evaluation printed circuit board (PCB) schematic can also be found on the FTP site.

The EV-ADF5610SD1Z evaluation board requires a SDP-S controller board (see Figure 3), which is not included with the kit. The SDP-S allows software programming of the ADF5610 device through a USB interface.

Full specifications for the ADF5610 wideband microwave synthesizer are available in the ADF5610 data sheet, which must be consulted in conjunction with this user guide when working with the evaluation board.

EV-ADF5610SD1Z EVALUATION BOARD PHOTOGRAPH

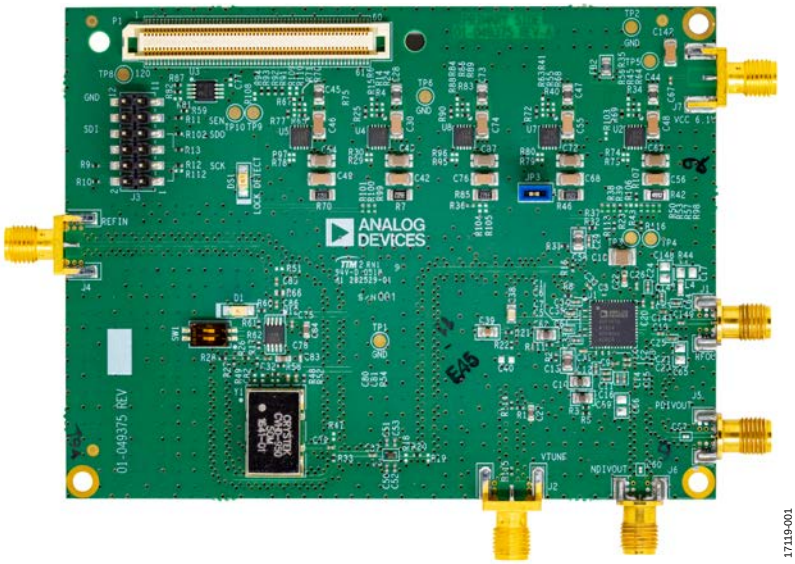

Figure 1.

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REVISION HISTORY

3/2019—Revision 0: Initial Version

GETTING STARTED

SOFTWARE INSTALLATION PROCEDURES

Download the EV-ADF5610SD1Z control software from ftp://ADF5610_ftp:ZagrJ6Fx@ftp.analog.com, the ADF5610 FTP page. The FTP user name and password are printed on a label inside the evaluation kit box. For the software installation procedure, see the PLL Software Installation Guide.

EVALUATION BOARD SETUP PROCEDURES

To run the software, perform the following steps:

1. After installation, double click the **ADF5610** icon on the desktop or select **Analog Devices > ADF5610** from the **Start** menu.
2. In the **Connection** tab, select **ADF5610** and **SDP-S Board**. Click **Connect** (see Figure 2).
3. Approximately 5 sec to 10 sec after the SDP-S establishes communications between the EV-ADF5610SD1Z and the PC, the connection status in the bottom left corner changes from **No device connected** to **Connected**.

Under **File**, the current settings can be saved to or loaded from a text file.

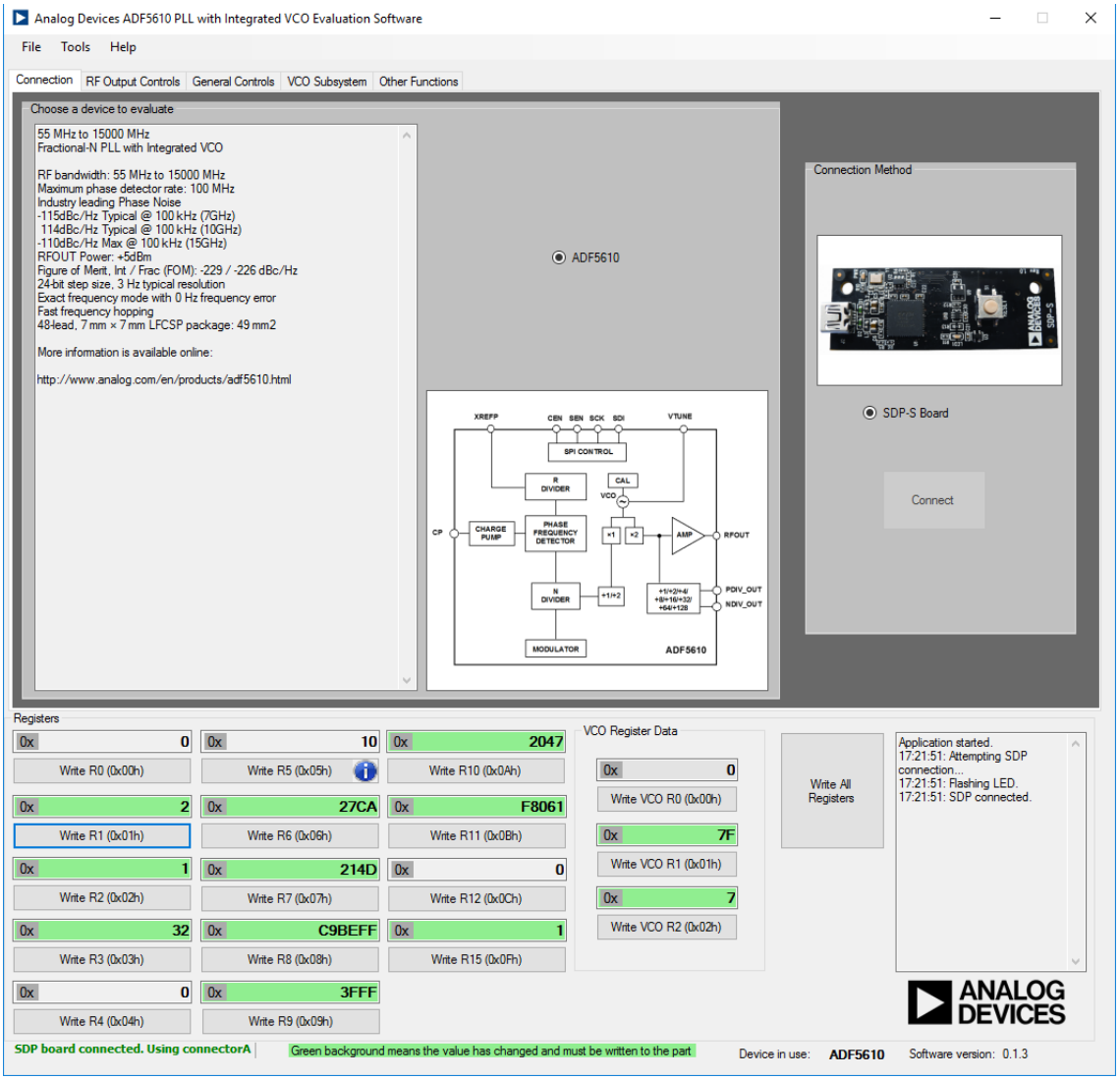

*Figure 2. Software Front Panel Display, **Connection** Tab*

EVALUATION BOARD HARDWARE

The EV-ADF5610SD1Z requires the SDP-S platform that uses the EVAL-SDP-CS1Z. Use of the SDP-B is not currently supported.

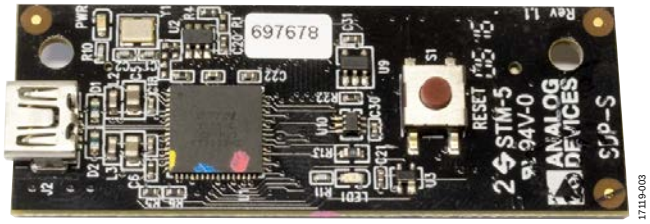

Figure 3. SDP-S USB Interface

The evaluation boards schematics, assembly, silkscreen and bill of materials are available in the Evaluation Board Schematics and Artwork section and the Ordering Information section.

POWER SUPPLIES

The EV-ADF5610SD1Z evaluation board is powered by a 6 V (600 mA) power supply connected to the SMA connector labeled VCC 6.1 V (J7).

The EV-ADF5610SD1Z evaluation board uses five low dropout (LDO) regulators: one LT3045, and four LT3042 devices. Three of these LDO regulators provide the biasing for the ADF5610.

Using fewer LDO regulators increases the risk of spur contaminated dc feeds, but provides a more cost efficient design. Combining bias circuitry requires careful selection to minimize the chance of increasing spurious content or levels at the RF outputs.

RF OUTPUT

The EV-ADF5610SD1Z has a total of three RF outputs.

RFOUT (J1) is a single-ended RF output that operates from 7.3 GHz to 14.6 GHz.

The two PDIVOUT (J5) and NDIVOUT (J6) outputs operate as a 100 Ω differential pair and as such are sensitive to impedance mismatch. If both of these RF outputs are to be used, ensure they are connected to equal load impedances. If only one port of the differential pair is to be used, terminate the complementary port with a 50 Ω termination. These outputs operate from 7.3 GHz to 14.6 GHz with the divider set to bypass mode (divide by 1). Additional divide ratios from 2 through 128 allow operation as low as 57 MHz.

If only RFOUT is used, NDIVOUT and PDIVOUT can be powered down. If NDIVOUT and PDIVOUT are to remain on but unused, terminate both SMA connectors with a 50 Ω termination to minimize unwanted propagation of RF signals.

Control of the RF output power, divider output power, and the ability to power down the output divider is available through VCO Register 0x01.

VCO Register 0x02 allows the divide ratio to be selected and power down of the VCO itself if desired.

VOLTAGE CONTROLLED OSCILLATOR (VCO)

The ADF5610 includes dual VCO cores with enough overlap between the cores such that continuous frequency coverage from 57 MHz to 14.6 GHz over temperature and supply variation is possible. Each VCO core is subdivided into 128 bands for a total of 256 bands. This topology allows broadband frequency coverage with more consistent tuning sensitivity across the band. Each band has an allowable tune voltage that is applied to Pin 37 (VT), of 0 V dc to 3.3 V dc. To maintain optimal charge pump linearity, minimize spurious levels, and to ensure autocalibration remains operational, the recommended tune voltage range is 0.5 V dc to 2.8 V dc. By default, autocalibration is enabled. Autocalibration utilizes an internally generated, temperature compensated voltage that is applied to the tune port of the VCO as each band is searched. Using autocalibration also ensures that, regardless of the ambient temperature during autocalibration, the synthesizer remains locked in the chosen band over the specified operating temperature range of −40°C to +85°C. At −40°C, this voltage is approximately 0.85 V, and at +85°C, the voltage is about 1.75 V. This preset voltage can be measured at the VPRST pin. The nominal tuning sensitivity is approximately 150 MHz.

LOOP FILTER

The reduced tuning voltage requirements of the ADF5610 PLL synthesizer architecture allows a simple passive loop filter to be used rather than an active loop filter.

A portion of loop filter component placements is shown in Figure 4. For lowest noise at 100 kHz offset, use the default components values included on the EV-ADF5610SD1Z. The values are as follows (C26, C27, and R1 are not shown in Figure 4):

- C38 = 0.18 µF, C39 = 3.9 µF, C40 = do not install (DNI), C27 = 68 nF, C26 = 100 pF
- R21 = 18 Ω, R22 = 0 Ω, R1 = 39 Ω

This loop filter is based on a 50 MHz phase frequency detector (PFD) frequency and a 2.54 mA charge pump current and has a loop bandwidth (BW) of approximately 4 kHz, with 47° of phase margin.

C26, C27, and R1 are located near the VT input (Pin 37) to provide additional filtering due to the extended loop filter path. The VTUNE port (J2) provides a means to verify the voltage at VT or to manually tune the VCO within its band in open-loop mode.

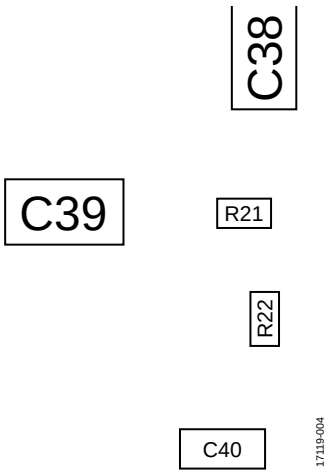

Figure 4. Loop Filter Placement

REFERENCE SOURCE

The evaluation board contains a low noise, 50 MHz, VCXO from Crystek Corporation (CVHD-950).

The EV-ADF5610SD1Z evaluation board is configured by default to use the on-board 50 MHz VCXO reference.

The EV-ADF5610SD1Z evaluation board also includes a feature to allow synchronization of the on-board VCXO to RF or microwave test equipment such as a spectrum analyzer or signal source analyzer, which in turn improves correlation between the programmed and displayed frequency. This feature is achieved by the PLL jitter cleanup circuit consisting of the D0 and D1 pins of the HMC1031 PLL (U12) and a dual, single-pole, single-throw (SPST) switch (SW1).

The EV-ADF5610SD1Z evaluation board is set up by default to allow the use of the jitter cleanup circuit. To use this feature, connect a 50 Ω, double shielded RF cable from REFIN (J4) to the 10 MHz input/output (I/O) synchronization port typically located on the rear of most modern test equipment. Use Table 1 to configure SW1 for the default setup. For example, if a 10 MHz I/O port is to be used with a 50 MHz VCXO, set SW1 to divide by 5 to divide the VCXO down to match the frequency of the I/O port.

Table 1. SW1 Divider Control Settings Using the HMC1031

Configuration	D1 Pin	D0 Pin
Power Down	0	0
Divide by 1	0	1
Divide by 5	1	0
Divide by 10	1	1

To use an external reference instead of the internal reference, modify the EV-ADF5610SD1Z evaluation board as follows:

1. Power down the HMC1031 PLL jitter cleanup circuit by setting D1 and D0 via SW1, as shown in Table 1, or by removing R100.
2. Power down the on-board VCXO by removing R99.
3. Remove C50, C51, R52, C53 from the jitter cleanup circuit to prevent loading and perturbation of the clock signal.
4. Replace L3 and C36 with a 0 Ω resistor. It may be necessary to adjust the value of C37 to maintain between 1 Ω and 3 Ω of reactance.
5. Verify that the drive level (swing and power range) is acceptable for the waveform being used. Consult the ADF5610 data sheet for the recommended operating regions for different reference frequencies using a square input vs. sinusoidal input.
6. If possible, connect the 10 MHz synchronization port on the external reference to the spectrum or signal source analyzer 10 MHz I/O.
7. Connect the external reference to the SMA connector labeled REFIN (J4).

DEFAULT CONFIGURATION

All components necessary for local oscillator generation are inserted on the EV-ADF5610SD1Z evaluation board. The EV-ADF5610SD1Z evaluation board is shipped with the ADF5610 synthesizer with an integrated VCO, a single-ended 50 MHz reference VCXO, a PLL jitter cleanup circuit, a 4 kHz loop filter (assuming charge pump current (I_{CP}) = 2.54 mA), and high performance, low noise voltage regulators.

EVALUATION BOARD SOFTWARE

MAIN CONTROLS

The **RF Output Controls** tab (see Figure 5) selects the RF settings for the output frequency. Consult the register descriptions of the ADF5610 data sheet for details.

Ensure that the value in the **External Reference Frequency** box equals the applied reference signal. The **External Reference Frequency** is set to 50 MHz by default, which matches the frequency of the VCXO that the EV-ADF5610SD1Z evaluation board is shipped with. The PFD frequency is calculated from the reference frequency, the R counter, the reference doubler, and the reference divide by 2. Ensure that the value in the **f_PFD (MHz)** box matches the value specified in the loop filter design.

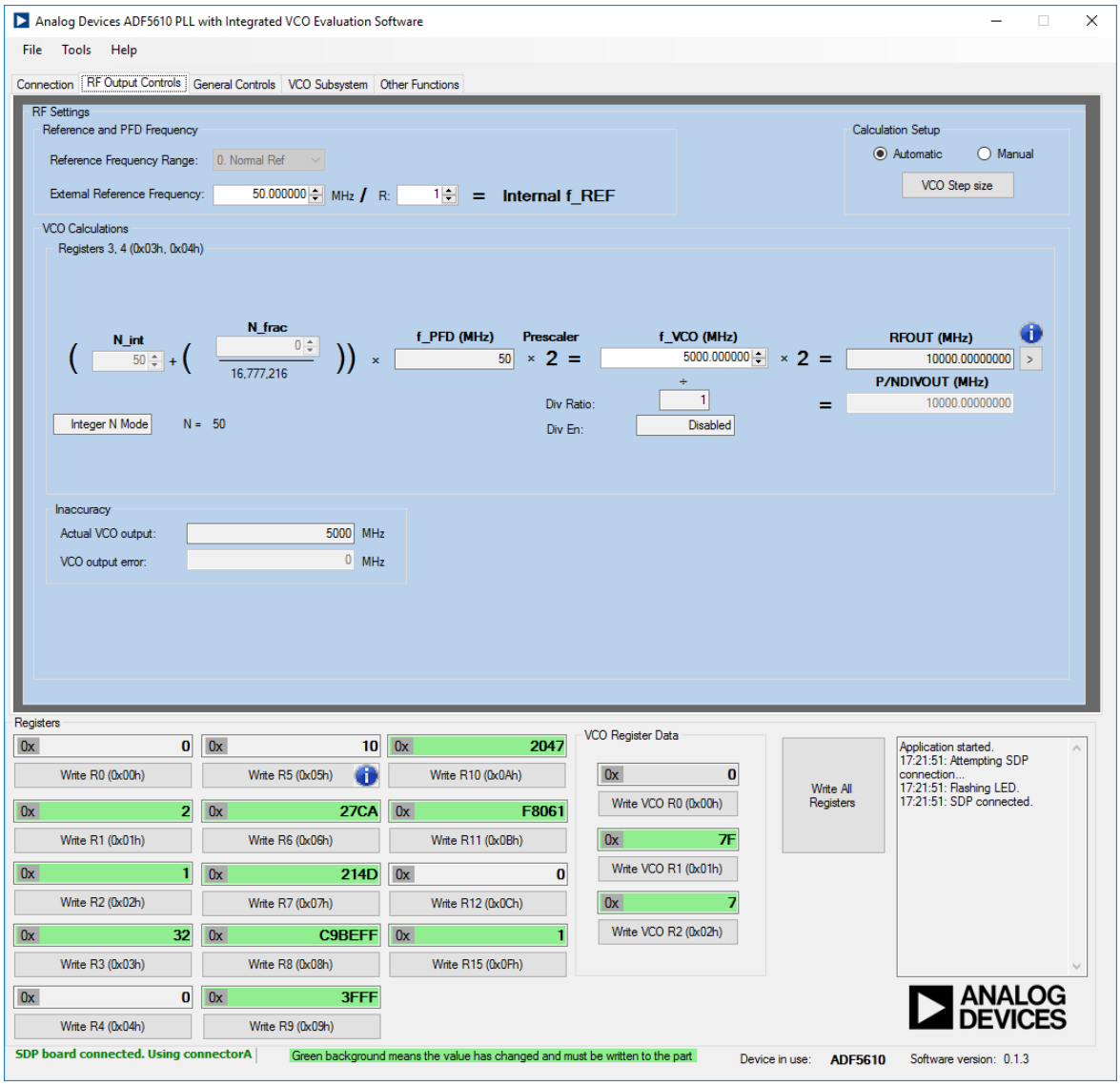

*Figure 5. Software Panel Display, **RF Output Controls** Tab*

The **General Controls** tab (see Figure 6) contains the rest of the settings, as described in the ADF5610 data sheet. In the **Charge Pump Control** section, enter the values in the **Charge-Pump Up Gain** and **Charge-Pump Dn Gain** boxes that match the values used for the loop filter design.

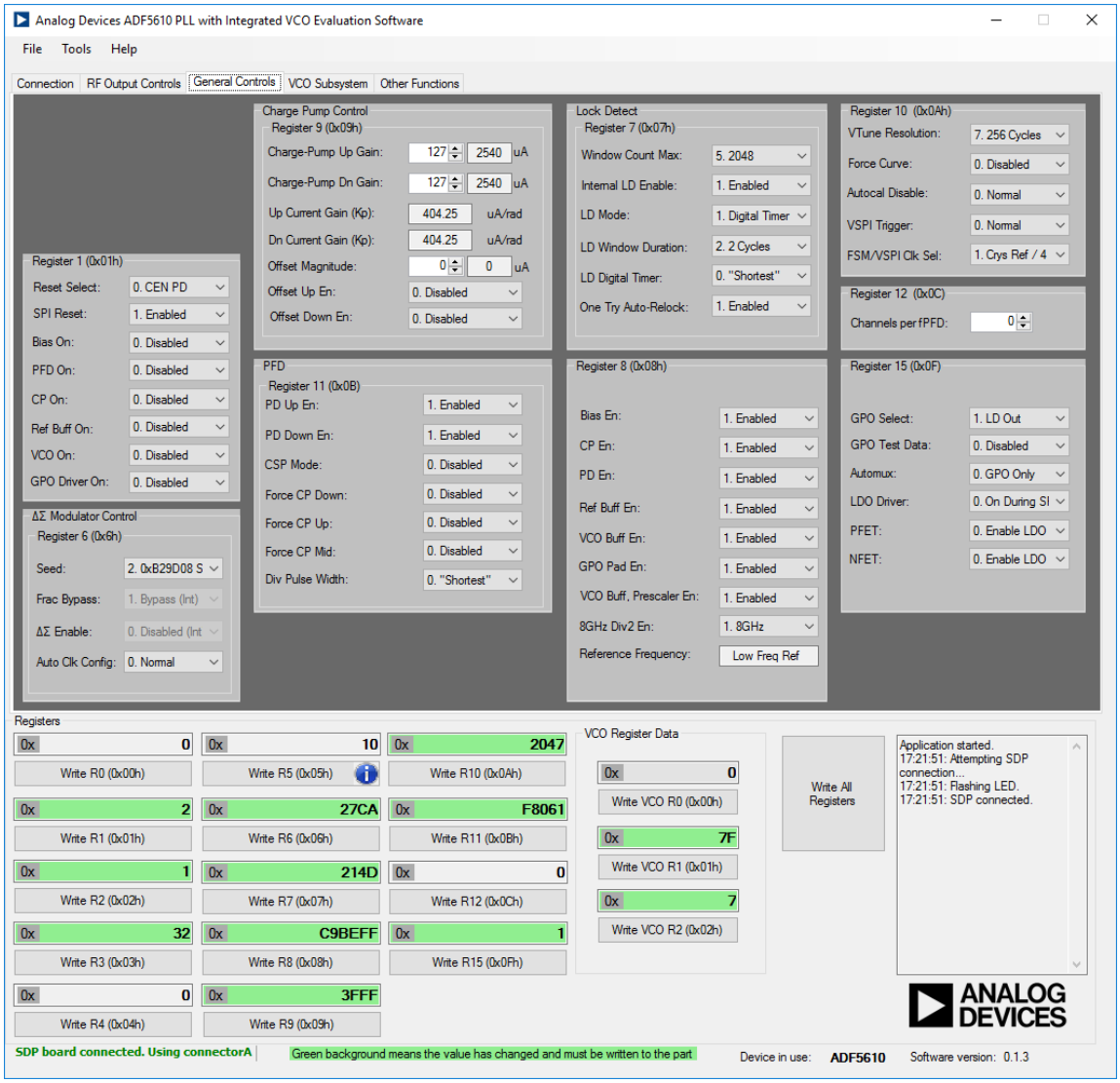

*Figure 6. Software Panel Display, **General Controls** Tab*

EVALUATION AND TEST

To evaluate and test the performance of the EV-ADF5610SD1Z use the following procedure. To ensure the software is able to program the device correctly, follow Step 3 to Step 10 exactly as they appear in this procedure every time the board is powered up.

1. Install the ADF5610 software (see the PLL Software Installation Guide).
2. If using a PC with Windows XP, follow the hardware driver installation procedure.
3. Connect the evaluation board to the SDP-S board.
4. Connect the 6 V power supply to the VCC 6.1V SMA (J7) connector, but ensure the power supply is turned off.
5. Connect the USB cable from the SDP-S board to the PC.
6. Run the ADF5610 software.
7. Select **ADF5610** and **SDP-S board** in the **Connection** tab and click **Connect** (see Figure 2).
8. Remove the micro USB cable from the SDP-S board.
9. Power on the 6 V power supply.
10. Connect the micro USB cable back into the SDP-S board.
11. Click **Write All Registers** in the **Registers** section of the software panel display.
12. Connect the spectrum analyzer to SMA Connector RFOUT (J1).
13. Measure the output spectrum and single sideband phase noise.

Figure 7 shows a phase noise plot at 7 GHz on RFOUT (J1).

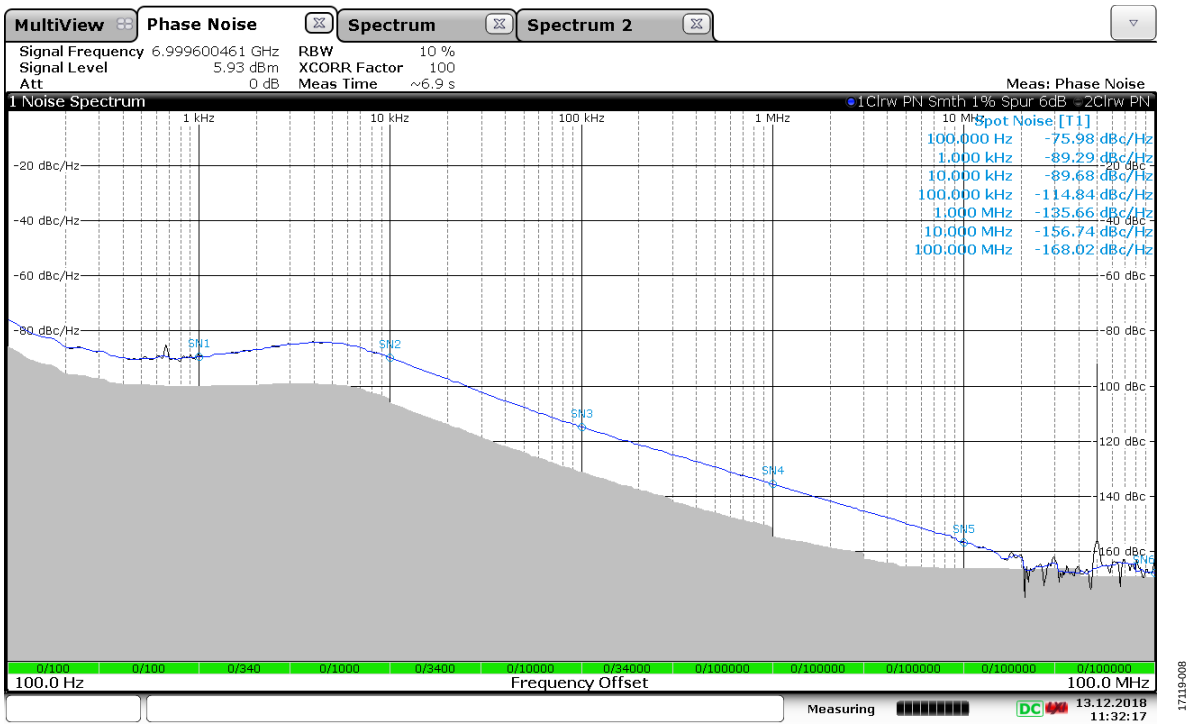

Figure 7. Phase Noise at RFOUT, 7 GHz, Jitter Cleanup Circuit Not Used

EVALUATION BOARD SCHEMATICS AND ARTWORK

EV-ADF5610SD1Z BOARD SCHEMATICS

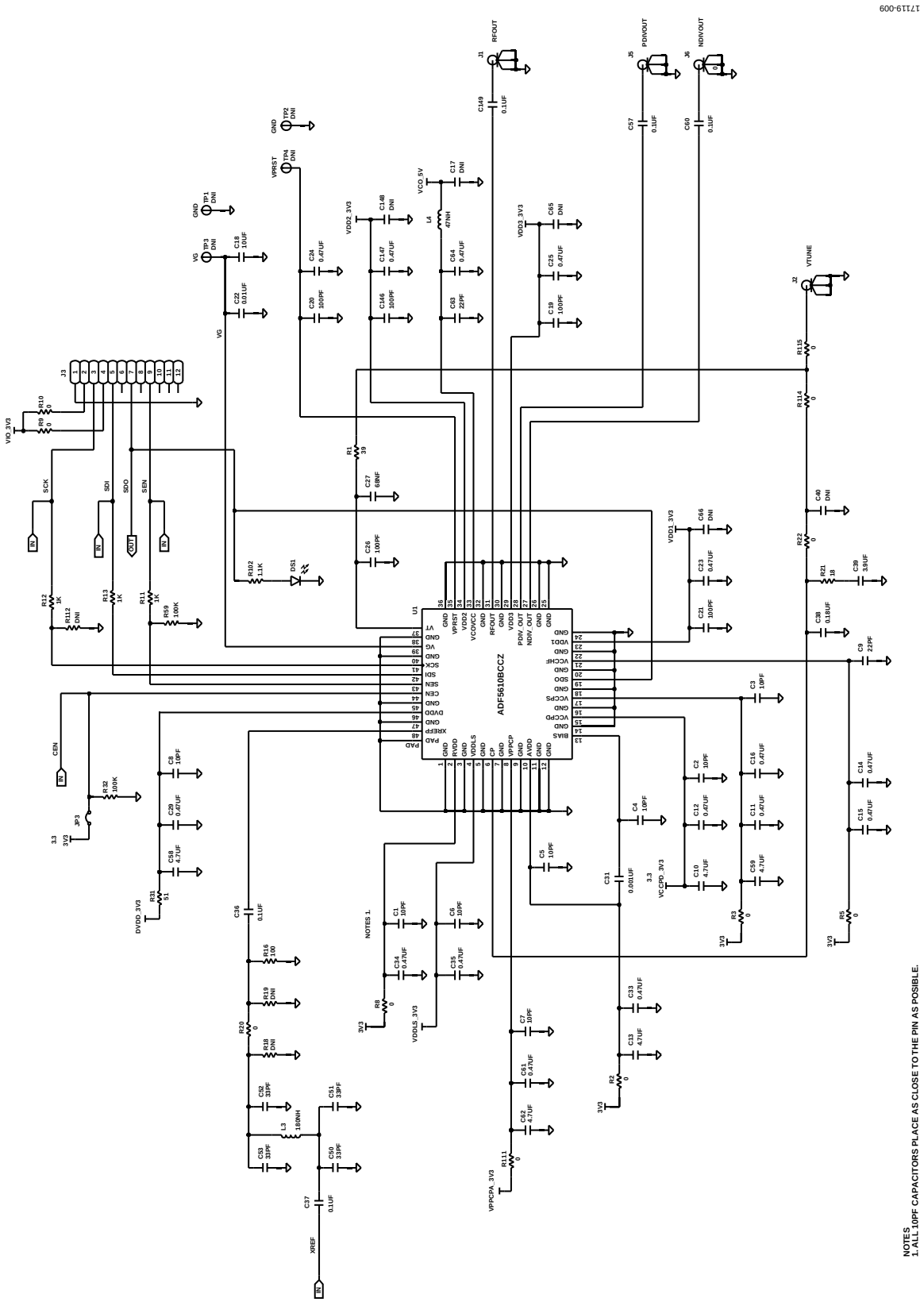

Figure 8. EV-ADF5610SD1Z Schematic, ADF5610

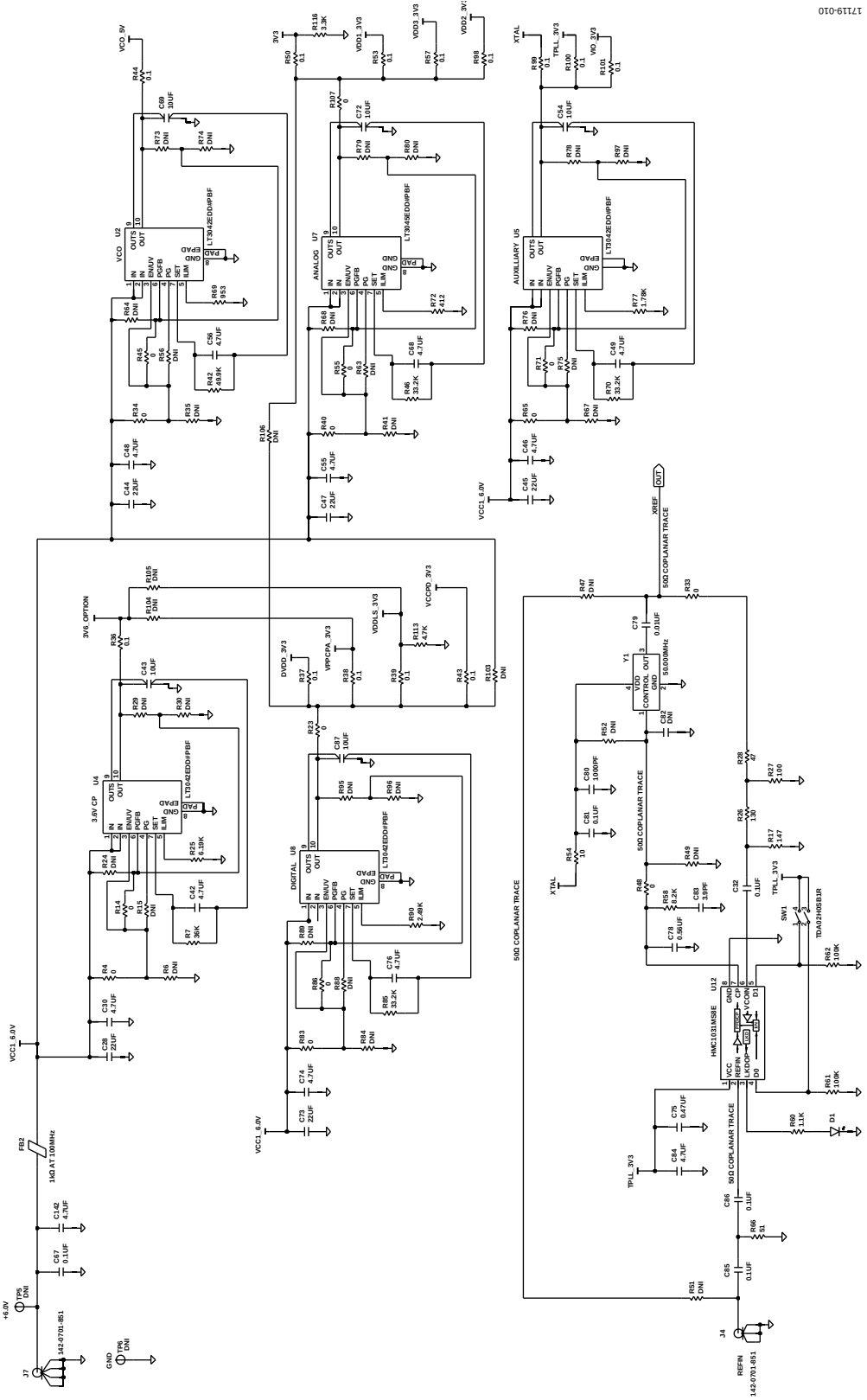

Figure 9. EV-ADF5610SD1Z Schematic, Power

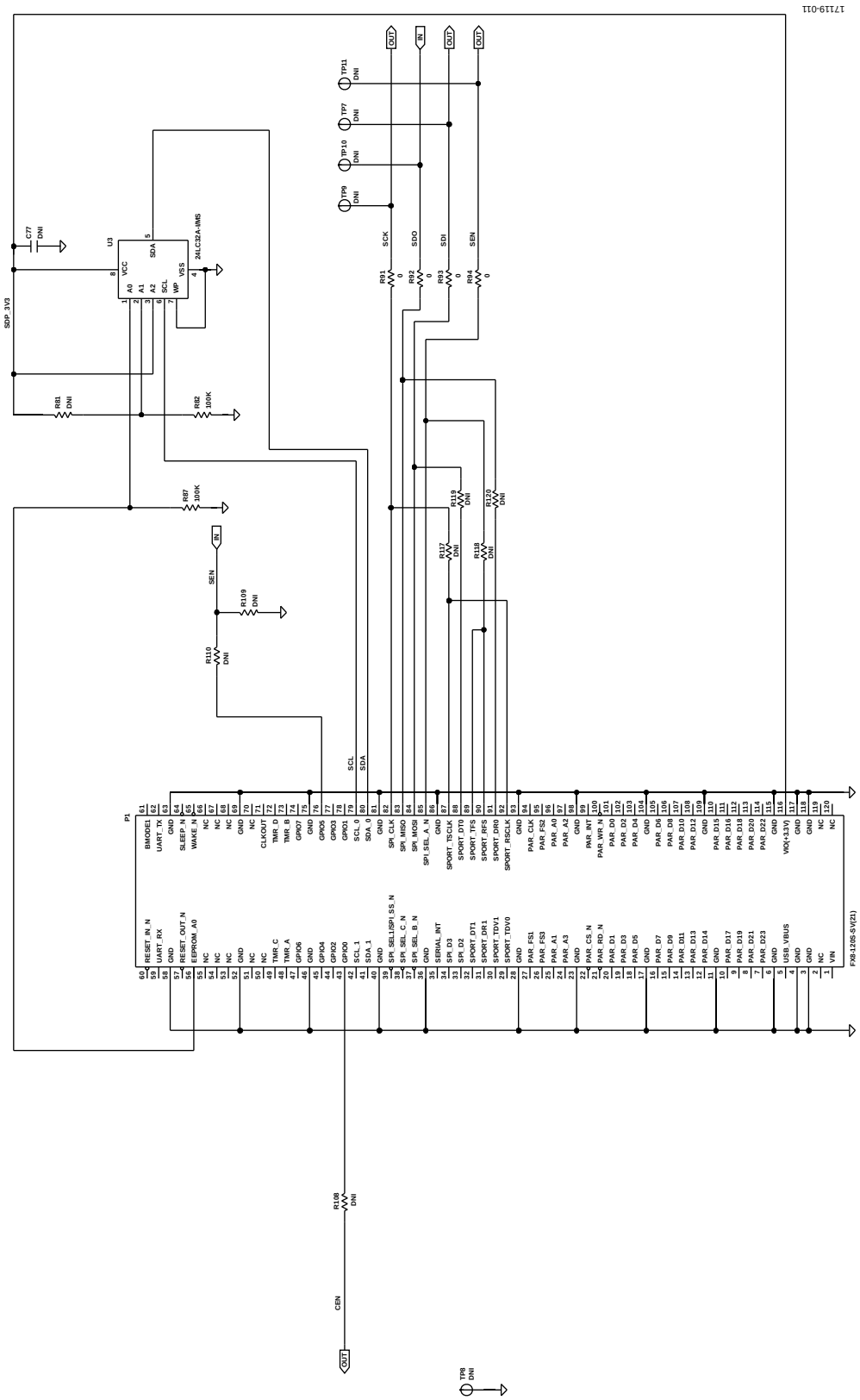

Figure 10. EV-ADF5610SD1Z Schematic, System Demonstration Platform (SDP) Connector

SILKSCREEN LAYERS

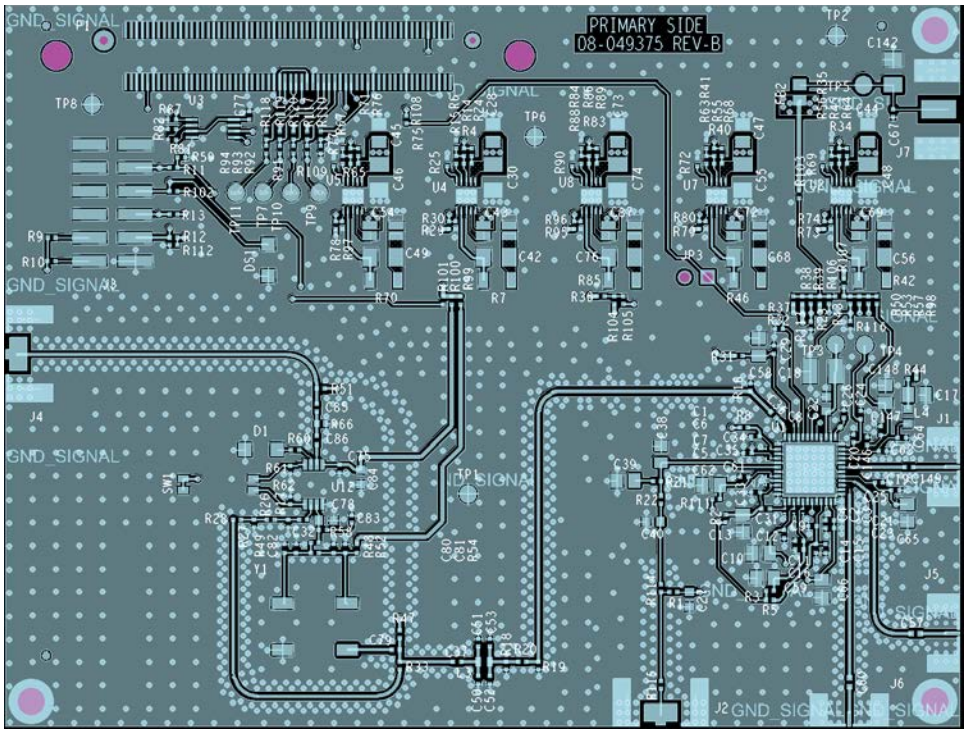

Figure 11. EV-ADF5610SD1Z Silk Screen and Metal 1, Top Side

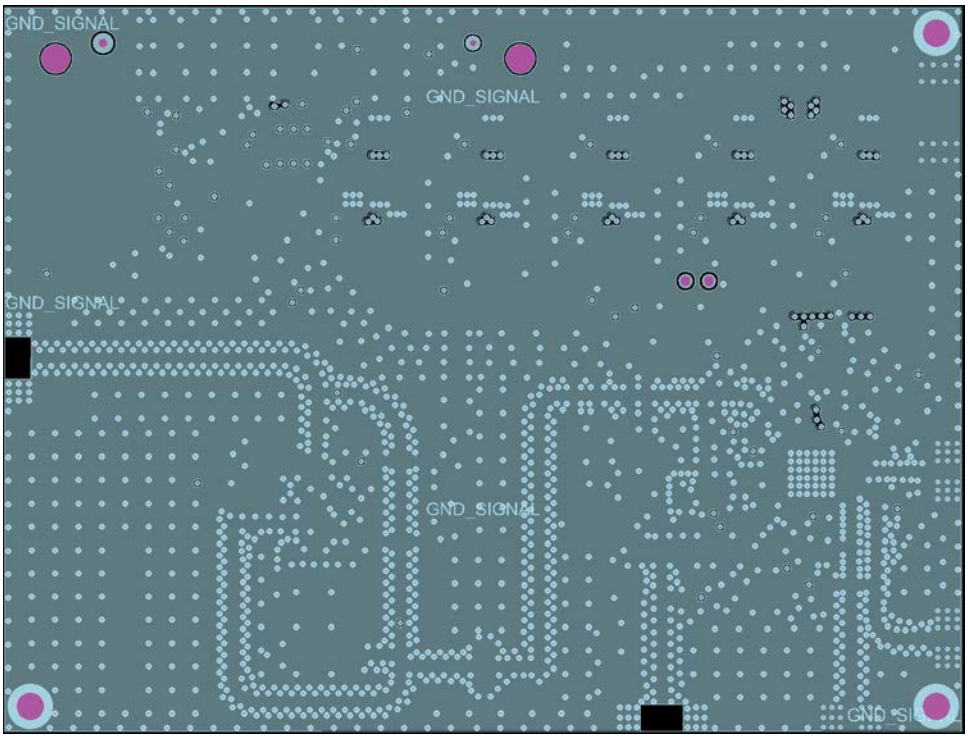

Figure 12. EV-ADF5610SD1Z Metal 2, Ground

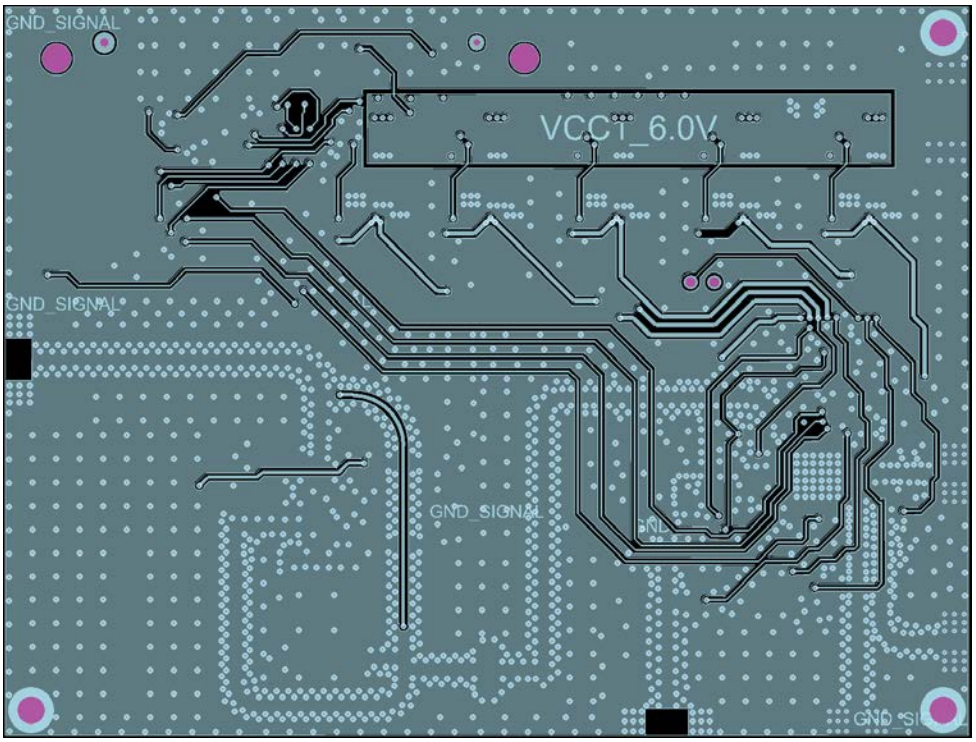

Figure 13. EV-ADF5610SD1Z Metal 3, RF and DC

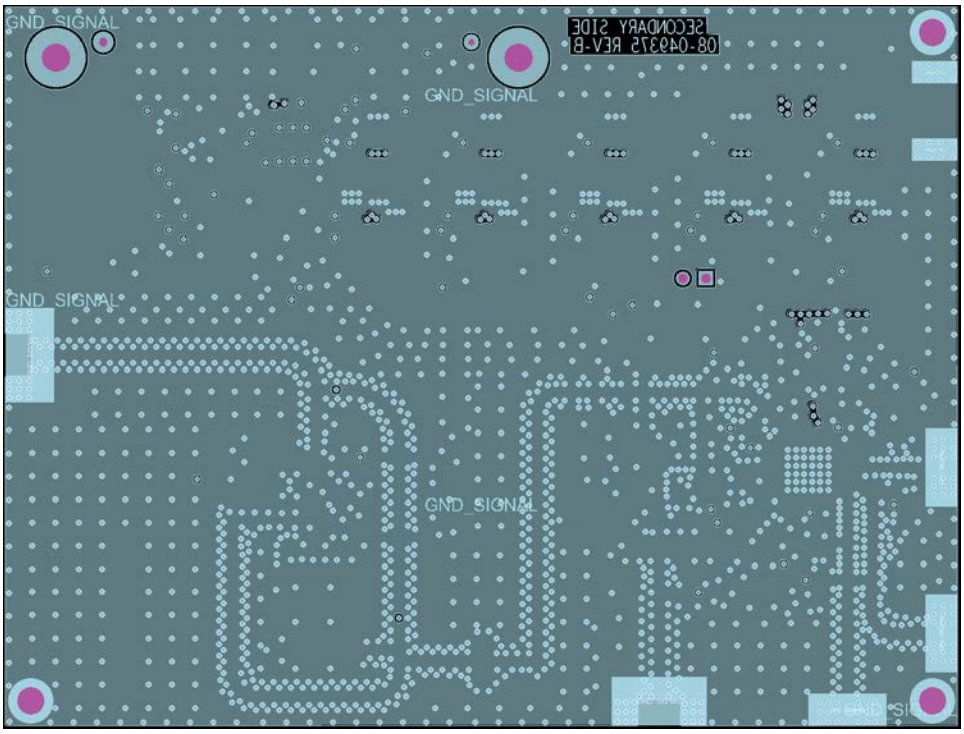

Figure 14. EV-ADF5610SD1Z Metal 4, Backside

ORDERING INFORMATION

BILL OF MATERIALS

Table 2.

Reference Designator	Description	Value	Manufacturer	Part Number
Not applicable	PCB, evaluation	Not applicable	Analog Devices, Inc.	600-01780-00
C1 to C8	Capacitor, ceramic, C0G (NP0), general-purpose	10 pF	Murata	GRM0335C1E100JA01D
C10, C13, C58, C59, C62	Capacitor, multilayer, ceramic, X7R, automotive grade	4.7 µF	Kemet	C0805X475J4RACAUTO
C11, C12, C14 to C16, C23 to C25, C29, C33 to C35, C61, C64, C147	Capacitor, multilayer, ceramic, X7R	0.47 µF	Taiyo Yuden	JMK105B7474KVHF
C30, C42, C46, C48 ,C49, C55, C56, C68, C74, C76, C142	Capacitor, ceramic, X7R	4.7 µF	Kemet	C1206C475K3RACTU
C19 to C21, C26, C146	Capacitor multilayer, ceramic, NP0, high temp	100 pF	TDK	C1005NP01H101J050BA
C57, C60, C149	Capacitor, ultrabroadband	0.1 µF	American Technical Ceramics	ATC550L104KT
C18	Capacitor, ceramic, X7R, general-purpose	10 µF	Murata	GRM32ER71H106KA12L
C22	Capacitor, ceramic, X7R	0.01 µF	Yageo	CC0603KRX7R9BB103
C27	Capacitor, ceramic, X7R, automotive grade	68 nF	Samsung	CL10B683KC8WPNC
C28, C44, C45, C47, C73	Capacitor, ceramic, X5R	22 µF	Murata	GRT21BR61E226ME13L
C31	Capacitor, ceramic, chip	0.001 µF	Kemet	C0402C102J3GACTU
C32	Capacitor, ceramic, X7R	0.1 µF	Kemet	C0402C104K4RACTU
C36, C37, C67, C81, C85, C86	Capacitor, ceramic, X5R	0.1 µF	Taiyo Yuden	LMK105BJ104KV-F
C38	Capacitor, ceramic, X7R	0.18 µF	AVX	08053C184KAT2A
C39	Capacitor, ceramic, X5R, commercial grade	3.9 µF	Kemet	C0805C395K8PACTU
C43, C54, C69, C72, C87	Capacitor, ceramic, X7R, 4-pin footprint	10 µF	Taiyo yuden	GMK316AB7106KL-TR
C50 to C53	Capacitor, ceramic, NP0 (C0G), high freq, high-Q	33 pF	Murata	GJM1555C1H330JB01
C9, C63	Capacitor, ceramic, NP0	22 pF	Yageo	CC0402JRNPO9BN220
C75	Capacitor, ceramic, X5R, 0402	0.47 µF	Taiyo yuden	LMK105BJ474KV-F
C78	Capacitor, ceramic, X5R, general-purpose	0.56 µF	Murata	C0603C564K8PACTU
C79	Capacitor, ceramic, chip X8R	0.01 µF	Tdk	C1005X8R1E103K
C80	Capacitor, ceramic, C0G (NP0), general-purpose	1000 pF	Murata	GRM1555C1H102JA01
C83	Capacitor, ceramic,	3.9 pF	Samsung	CL05C3R9CBNC
C84	Capacitor, ceramic, X6S, general-purpose	4.7 µF	Murata	GRM188C81C475KE11D
D1, DS1	LED, aluminum, indium, gallium, and phosphorous (AlInGaP), 560 nm, green	597-3311-407NF	Dialight	597-3311-407NF
FB2	Inductor chip ferrite bead multilayer, 0.5 A, 0.280 Ω maximum dc resistance	1 kΩ at 100 MHz	Murata	BLM21AG102SN1D
J1, J5, J6	Connector, K jack, 40 GHz, 0.062 in. thick board	25-146-1000-92	SRI Connector Gage, Co.	25-146-1000-92
J2, J4	Connector, PCB, jack assembly, end launch, SMA, 62 mil board thickness,	142-0701-851	Cinch	142-0701-851

Reference Designator	Description	Value	Manufacturer	Part Number
J3	Connector, PCB, surface-mount technology (SMT) square post	TSM-106-01-T-DV	Samtec	TSM-106-01-T-DV
J7	Connector, PCB, SMA, 50 Ω end launch jack receptacle	142-0701-851	Cinch	142-0701-851
JP3	Connector, PCB, 2-position, unshrouded 0.635 mm square post header, 5.84 mm post height, 2.54 mm solder tail, 2.54 mm pitch	HTSW-102-07-T-S	Samtec, INC.	HTSW-102-07-T-S
L3	Inductor, chip 0.15 Ω, dc resistance, 1.3 A	180 nH	Coilcraft, Inc.	0603LS-181XJLB
L4	Inductor, RF ceramic chip, 0.9 Ω, dc resistance, 0.3 A	47 nH	Johanson Technology	L-14C47NJV4T
P1	Connector PCB vertical type receptacle for SDP breakout board	FX8-120S-SV(21)	HRS	FX8-120S-SV(21)
R1	Resistor, thick film, surface-mount device (SMD), 0402	39 Ω	Panasonic	ERJ-2GEJ390X
R2 to R5, R8 to R10, R14, R20, R22, R23, R33, R34, R40, R45, R48, R55, R65, R71, R83, R86, R91 to R94, R107, R111, R114, R115	Resistor, chip, SMD, jumper	0 Ω	Panasonic	ERJ-2GE0R00X
R36 to R39, R43, R44, R50, R53, R57, R98 to R101	Resistor, thick film	0.1 Ω	Panasonic	ERJ-2BSFR10X
R60, R102	Resistor, thick film, SMD, 0402	1.1 kΩ	Panasonic	ERJ-2GEJ112X
R11 to R13	Resistor, precision thick film chip	1 kΩ	Panasonic	ERJ-2RKF1001X
R113	Resistor, precision thick film chip	4.7 kΩ	Panasonic	ERJ-2RKF4701X
R116	Resistor, precision thick film chip	3.3 kΩ	Panasonic	ERJ-2RKF3301X
R16	Resistor, thick film chip, automotive grade	100 Ω	Panasonic	ERJ-2GEJ101X
R17	Resistor, precision thick film chip, for automotive	147 Ω	Panasonic	ERJ-2RKF1470X
R21	Resistor, precision film chip thick	18 Ω	Yageo	RC0402JR-0718RL
R25	Resistor, precision thick film chip	6.19 kΩ	Panasonic	ERJ-2RKF6191X
R26	Resistor, precision thick film chip	130 Ω	Panasonic	ERJ-2RKF1300X
R27	Resistor, precision thick film chip	100 Ω	Panasonic	ERJ-2RKF1000X
R28	Resistor, thick film chip	47 Ω	Panasonic	ERJ-2GEJ470X
R31, R66	Resistor, thick film, SMD, 0402	51 Ω	Panasonic	ERJ-2GEJ510X
R32, R59, R61, R62, R82, R87	Resistor, thick film chip	100 kΩ	Panasonic	ERJ-2GEJ104X
R42	Resistor, precision thick film chip, R1206	49.9 kΩ	Panasonic	ERJ-8ENF4992V
R46, R70, R85	Resistor, precision thick film chip, R1206	33.2 kΩ	Panasonic	ERJ-8ENF3322V
R54	Resistor, precision thick film chip	10 Ω	Panasonic	ERJ-2RKF10R0X
R58	Resistor, thick film, SMD, 0402	8.2 kΩ	Panasonic	ERJ-2GEJ822X
R69	Resistor, thick film chip	953	Vishay	CRCW0402953RFKED
R7	Resistor, thick film, SMD, 1206	36 kΩ	Welwyn	36K WCR 1206
R72	Resistor, precision thick film chip	412 Ω	Panasonic	ERJ-2RKF4120X
R77	Resistor, precision thick film chip	1.78 kΩ	Panasonic	ERJ-2RKF1781X
R90	Resistor, precision thick film chip	2.49 kΩ	Panasonic	ERJ-2RKF2491X
SW1	Switch dual inline package (DIP) off/on dual single-pole, single-throw (SPST), 0.025 A	TDA02H0SB1R	C&K	TDA02H0SB1R
U1	IC, Analog Devices microwave wideband synthesizer with integrated VCO	ADF5610BCCZ	Analog Devices	ADF5610BCCZ

Reference Designator	Description	Value	Manufacturer	Part Number
U12	IC, Analog Devices clock generator with Integer-N PLL, 0.1 MHz to 500 MHz	HMC1031MS8E	Analog Devices	HMC1031MS8E
U2, U4, U5, U8	IC, linear, 20 V, 200 mA, ultralow noise, ultrahigh PSRR RF linear regulator	LT3042EDD#PBF	Analog Devices	LT3042EDD#PBF
U3	IC, 32 kb, serial EEPROM	24LC32A-I/MS	Microchip Technology	24LC32A-I/MS
U7	IC, linear, 20 V, 500 mA, ultralow noise, ultrahigh, PSRR linear regulator	LT3045EDD#PBF	Analog Devices	LT3045EDD#PBF
Y1	IC VCXO ultralow phase noise oscillator	50.000 MHz	Crystek Corporation	CVHD-950-50.000
C17, C65, C66, C148	Do not install	4.7 µF	Kemet	C0805X475J4RACAUTO
C17	Do not install	1500 pF	Kemet	C0603C152J5GACTU
C77	Do not install	0.1 µF	Kemet	C0402C104K4RACTU
C82	Do not install	0.01 µF	TDK	C1005X8R1E103K
R103 to R105	Do not install	0.1 Ω	Panasonic	7005414
R6, R15, R18, R19, R24, R29, R30, R35, R41, R47, R49, R51, R52, R56, R63, R64, R67,R68, R73 to R76, R78 to R80, R84, R88, R89, R95 to R97,R106,R108 to R110, R117 to R120	Do not install	0 Ω	Panasonic	7000282
R81, R112	Do not install	100k Ω	Panasonic	7005773
TP1 to TP11	Do not install	SMOX/060/B1/R2K GOLD	Oxley	SMOX/060/B1/R2K GOLD

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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